VHDL Based Simulation of a Sigma-Delta A/D Converter

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About the MixED Method

- MixED = Mixed-signal Event Driven
- Network of controlled sources
- Source voltages and output impedances are user-definable functions
- Implicite backward Euler integration of DEQ for capacitive and inductive loads
- Output of a controlled source is triggered not before input data is stable

Academic Aspects

- Individual time stepping of each node
- Single kernel solver
- Iterations occur for nonlinear devices (e.g. CMOS inverter) and networks with more than 1 analog nodes between sources
- Convergence behavior for such networks of individually acting sources is subject to research

Practical Aspects

- A/D and D/A converters
- PLL‘s (spec. if they have digital ports only)
- Fits in standard environments (DRC, Synthesizer)
- Models can be given as „black boxes“ to customers that have digital VHDL only
- No need to buy nor learn VHDL-AMS

Problems / Features

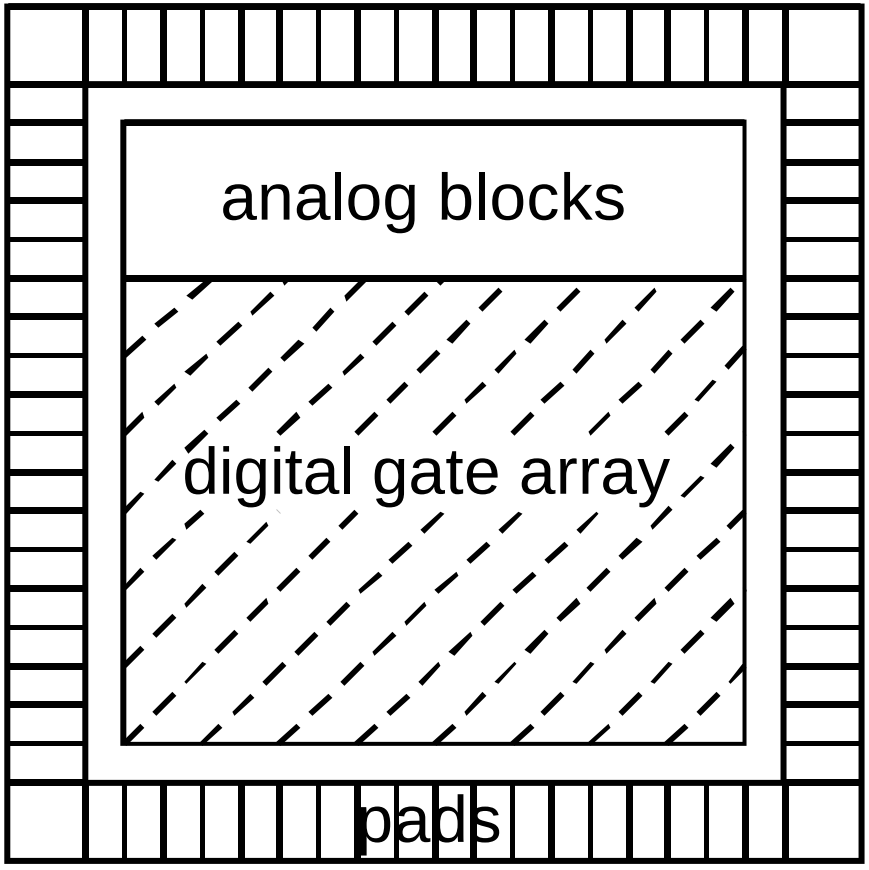
- Numerical stability depends on models
- Moderate nonlinearities only (e.g. CMOS digital gates)
- Range of applications:
  academically problably <1% of VHDL-AMS
  practically many relevant mixed-signal circuits: ΣΔ–modul., PLL, CMOS gates, OpAmp, SC, ...

Goal here: Verification of the VHDL Based MixED Simulation Module

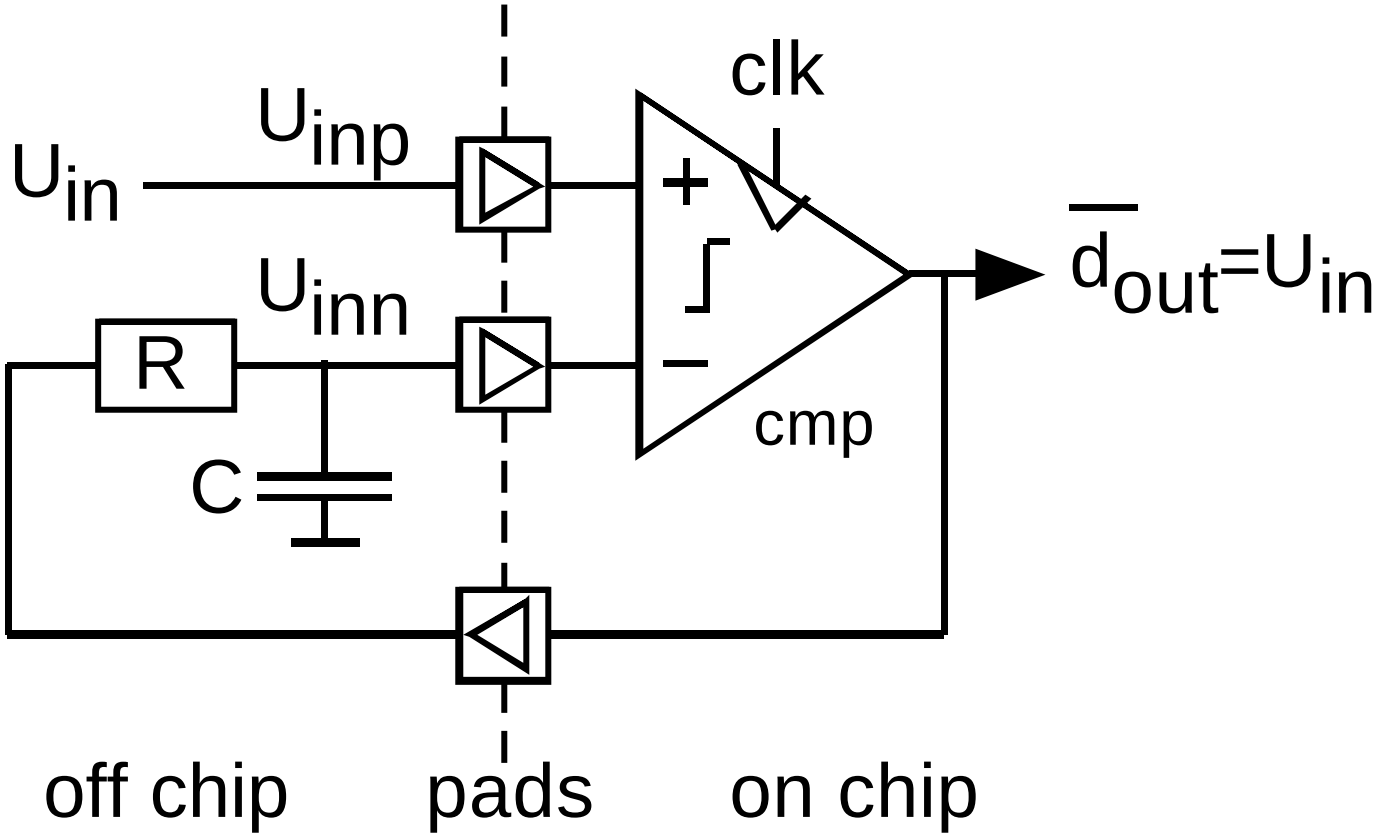
- By comparison to simulated data
- By comparision to experimental data

Suitable Applications

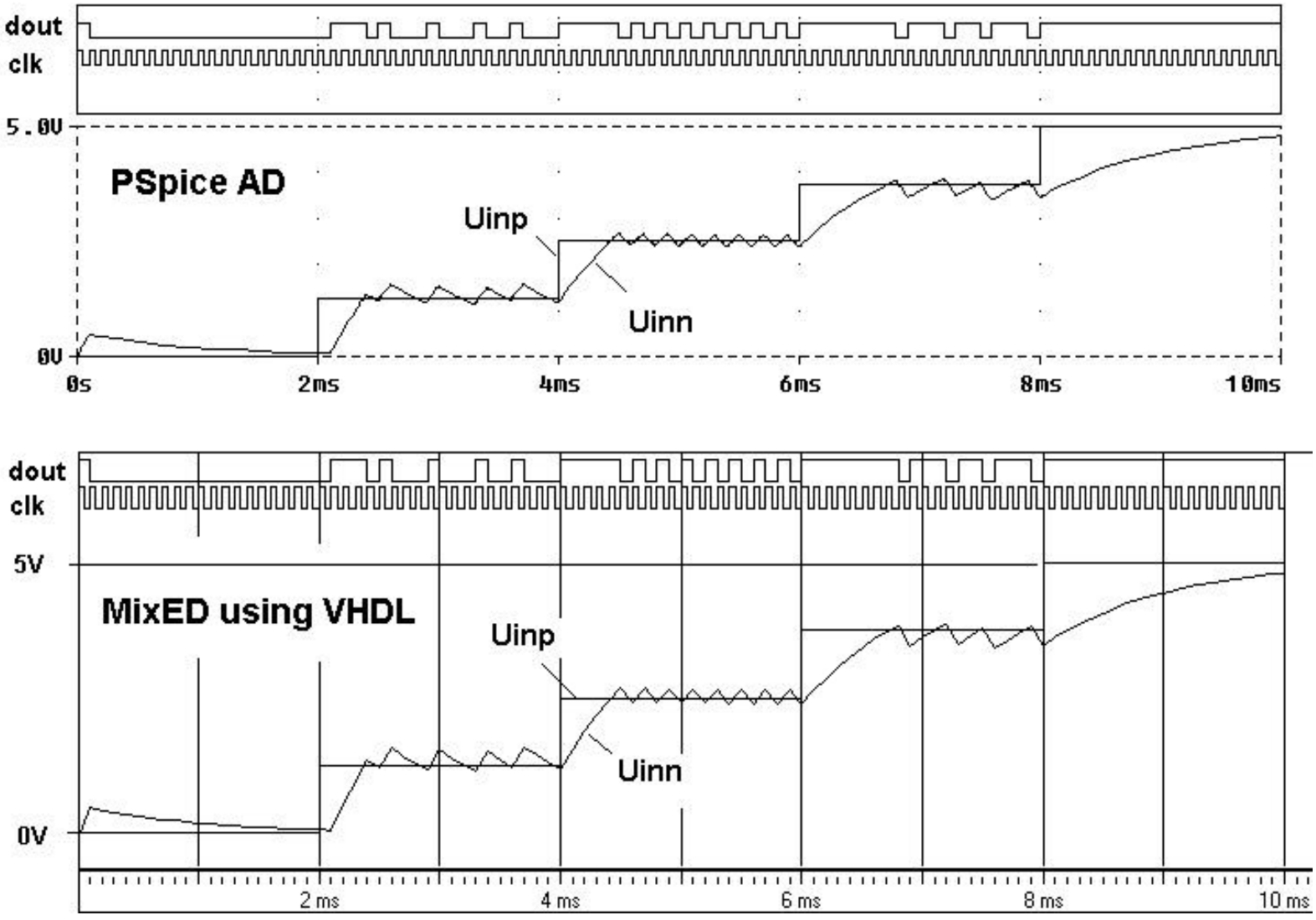
Mostly digital circuits with some simple analog fuctions, as offered e.g. by the Institute for Microelec-tronics Stuttgart (IMS) [8].



Application: Sigma-Delta Modulator for A/D Conversion



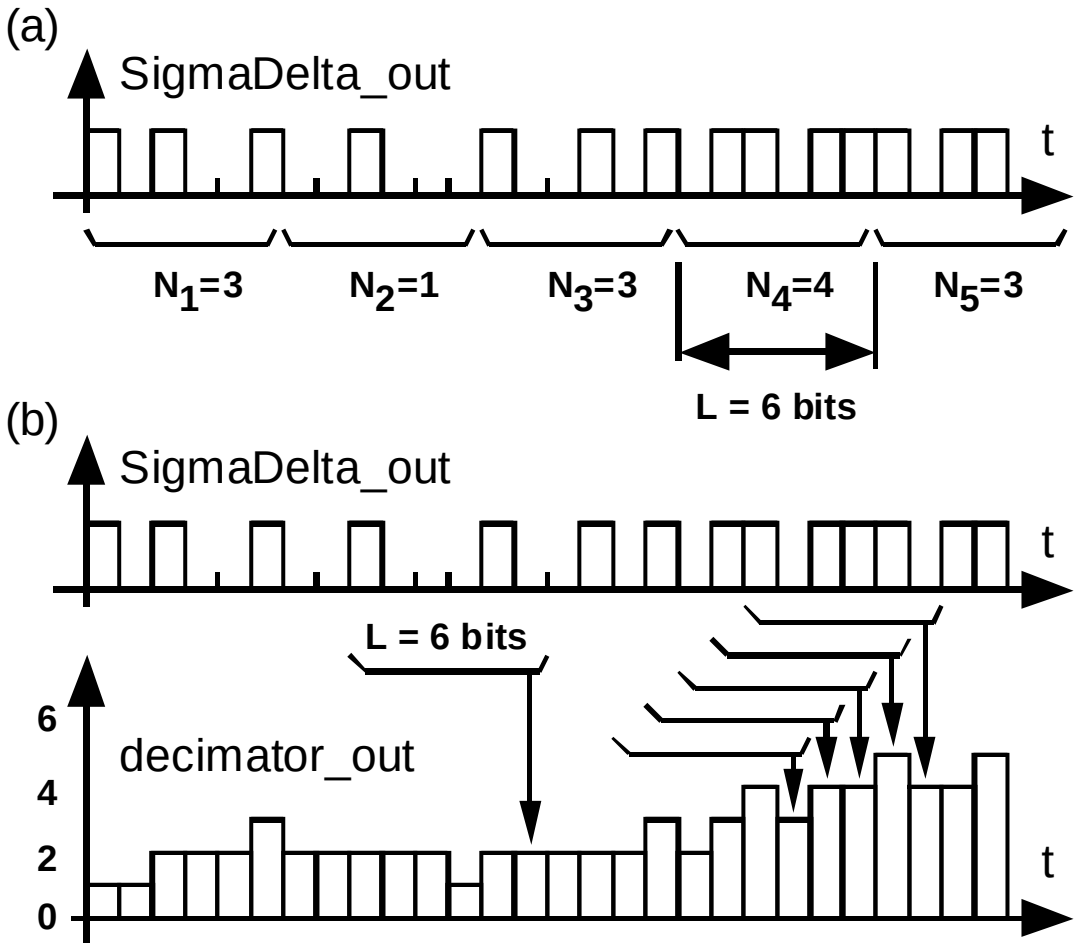
MixED vs. Pspice-AD Simulation



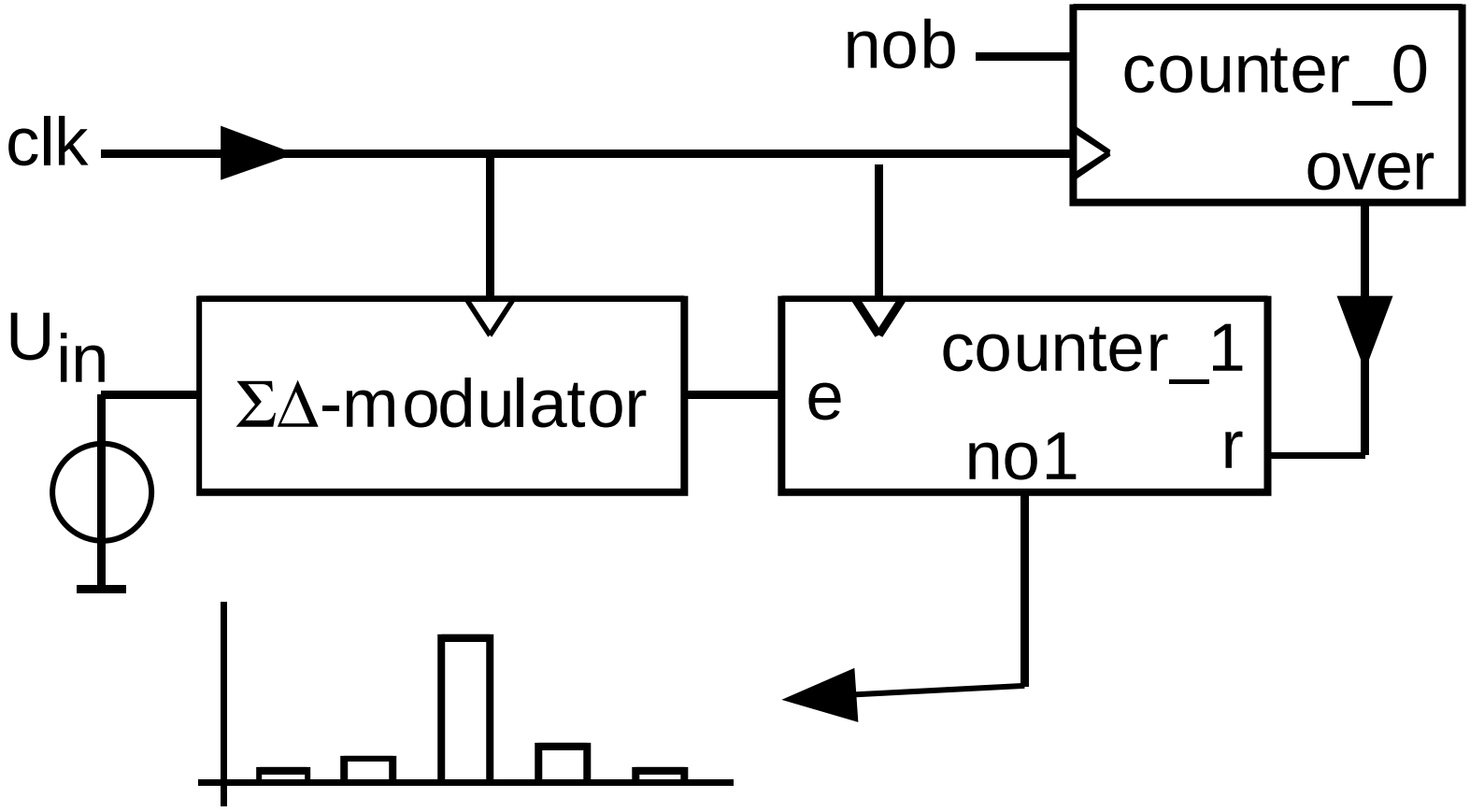
Computing the average of the Pseudo-Random Bit Stream

- Average of d_{out}: $\bar{d}_{out} = N / L$
- Corresp. Voltage: $U_{out} = a \cdot \bar{d}_{out} + b$
- Filter: $decimator\_out(n) = \sum_{i=0}^{L-1} d_{out}(n-i)$

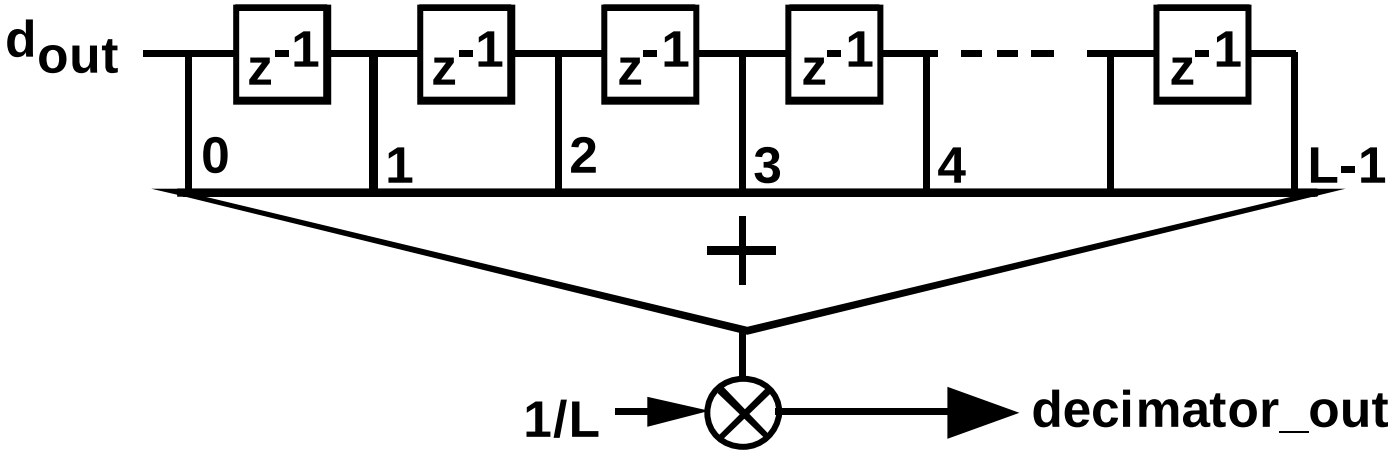
Measurement Setups



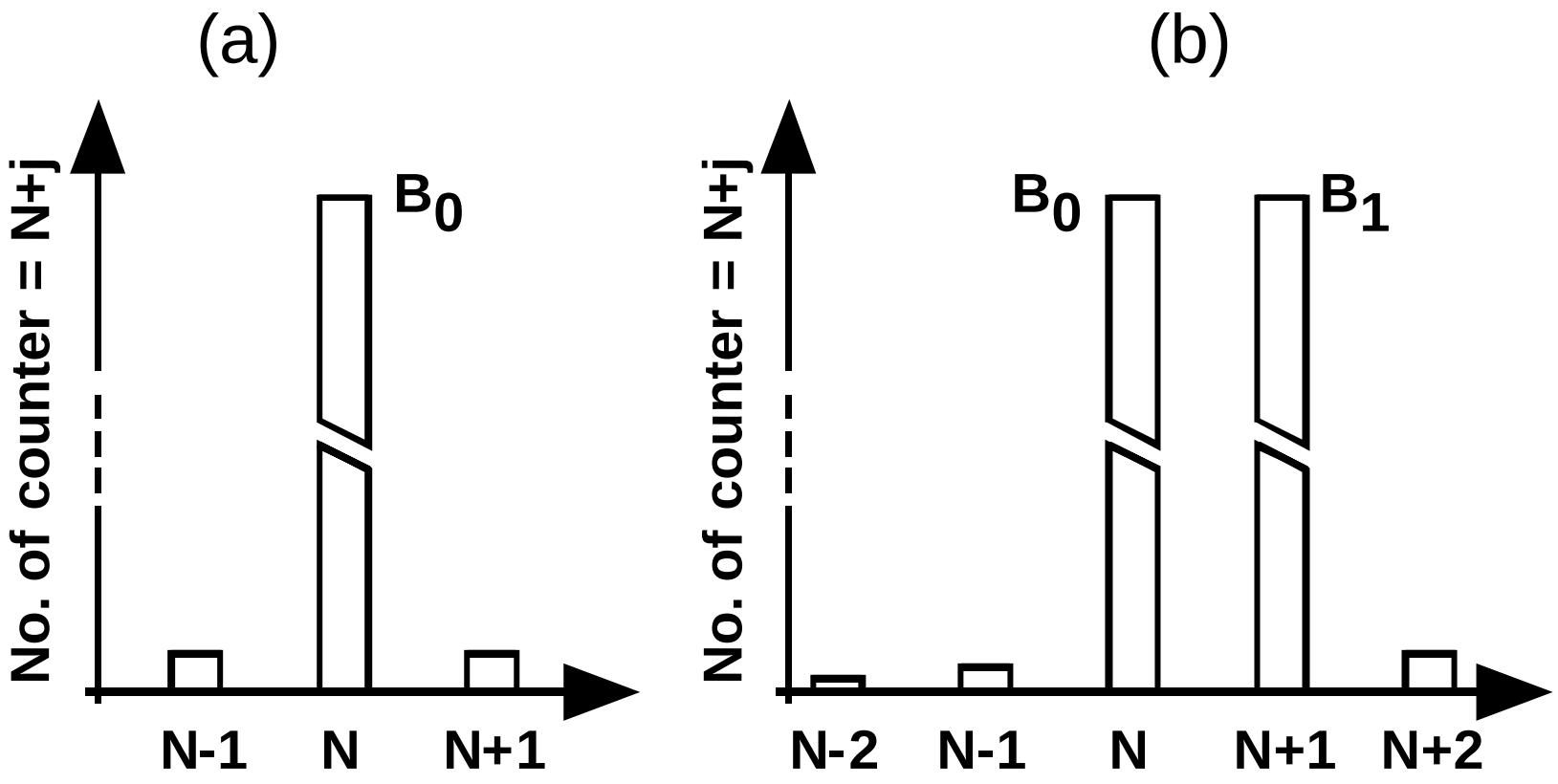
Experimental Setup: Counters Used for Decimation



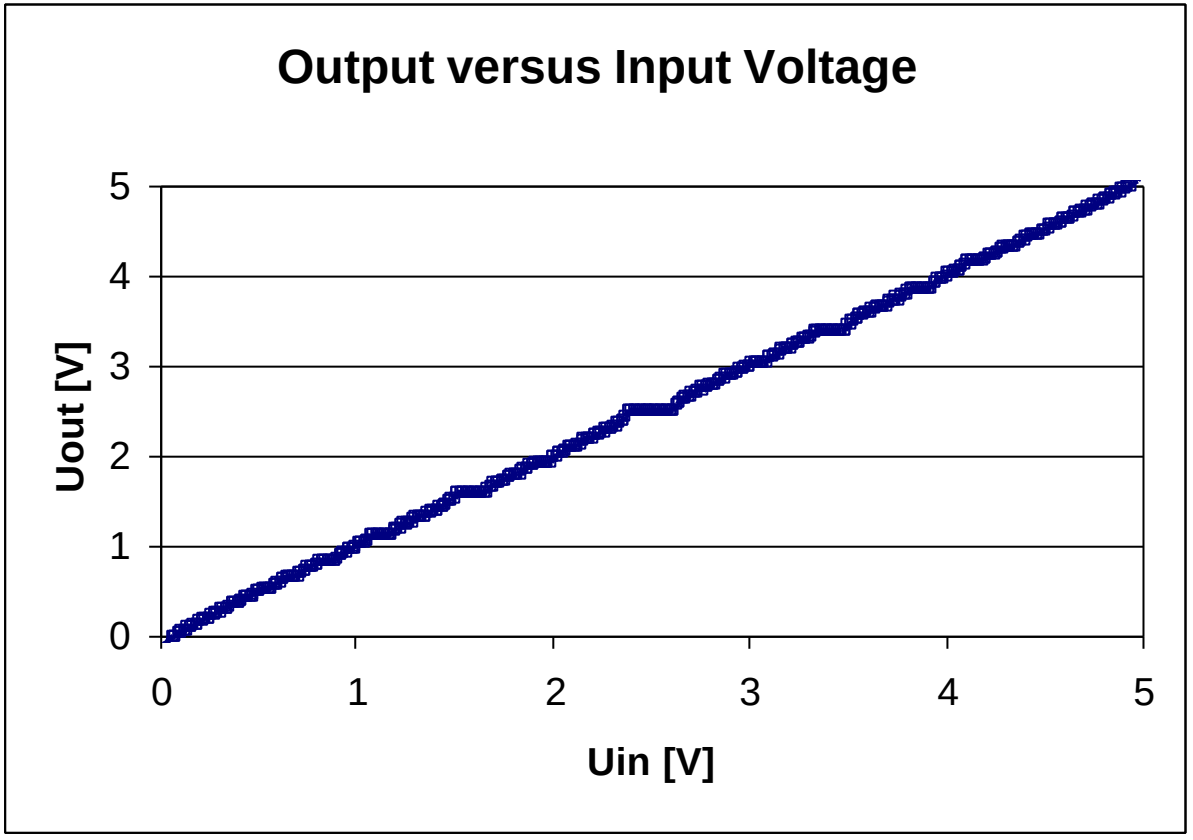
Simulated Setup: Moving Averager Used for Decimation



Experimental statistics

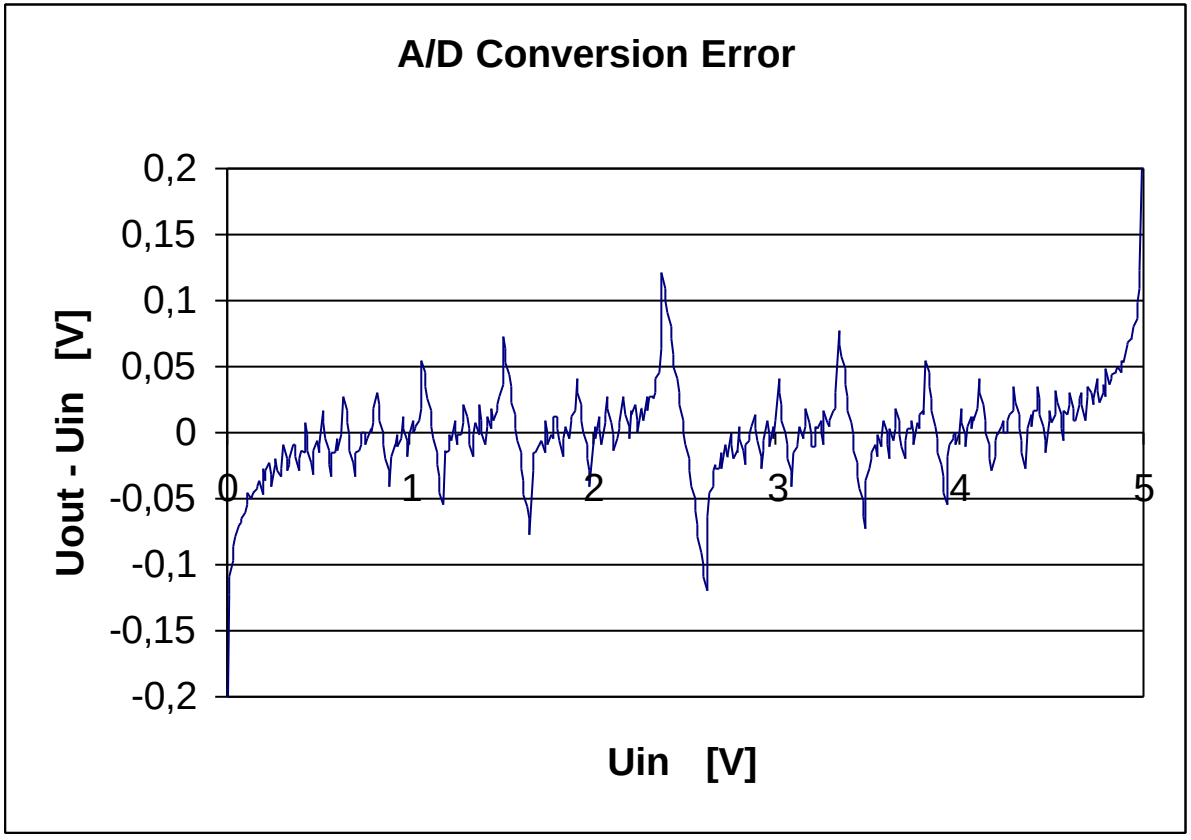


Simulated y_{out}/u_{in} Charateristics



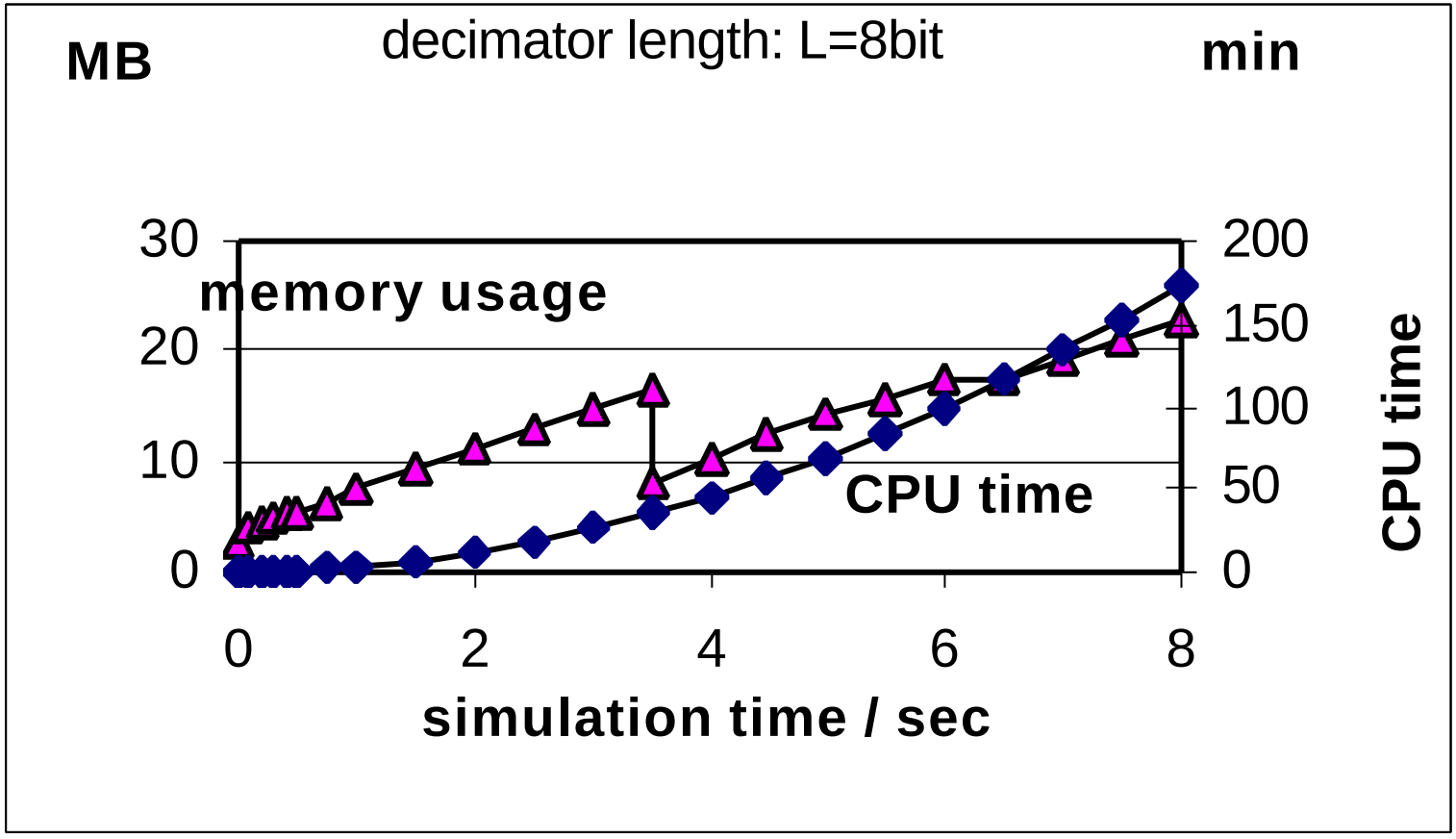
Horizontal niveaus are due to the dead zone problem [11]

Err: Output Voltage - Input Voltage



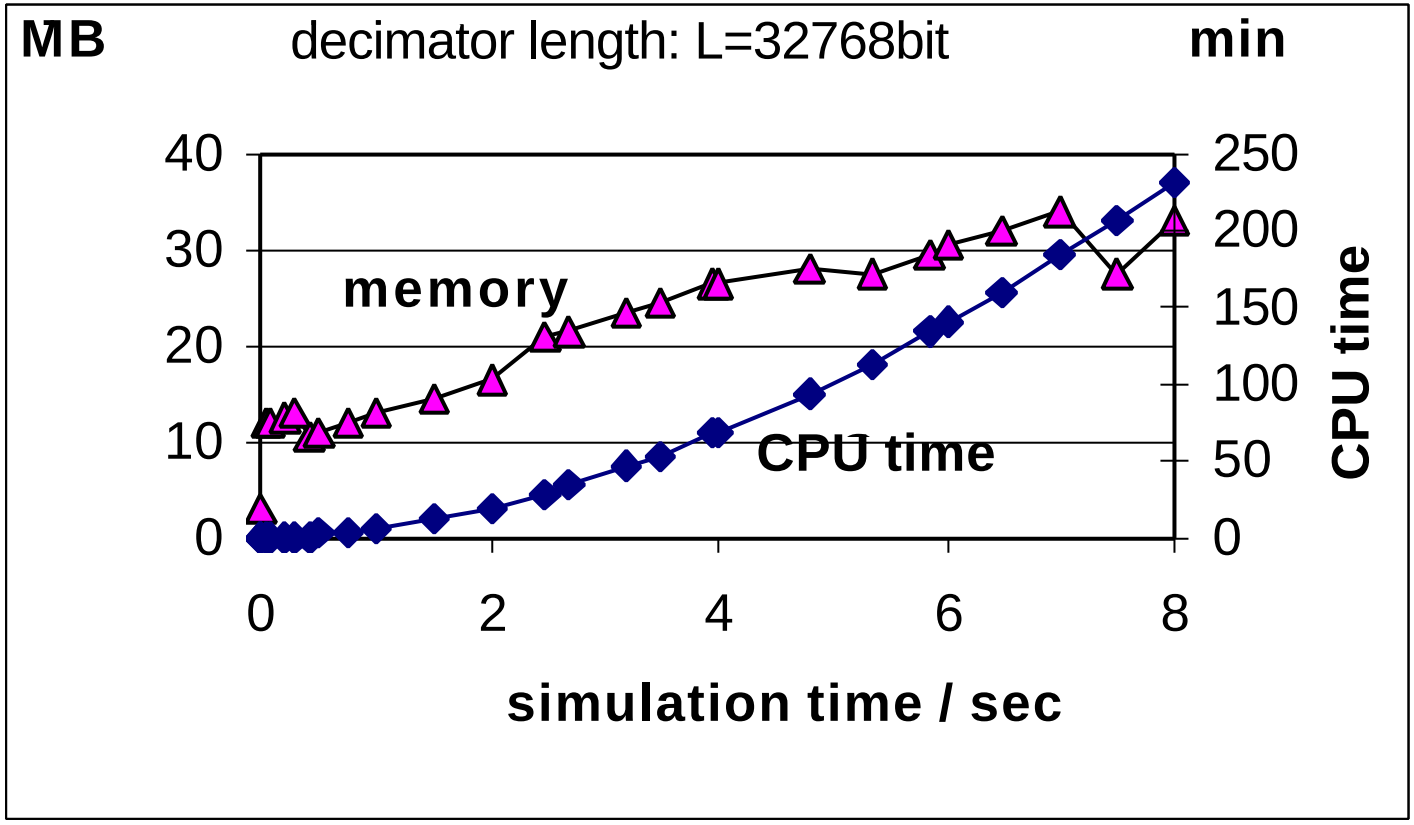
The maxima around Uin=2.5V illustrate the dead zone problem

CPU Power Consumed with 8 Bit Averager at f_{clk}=20KHz



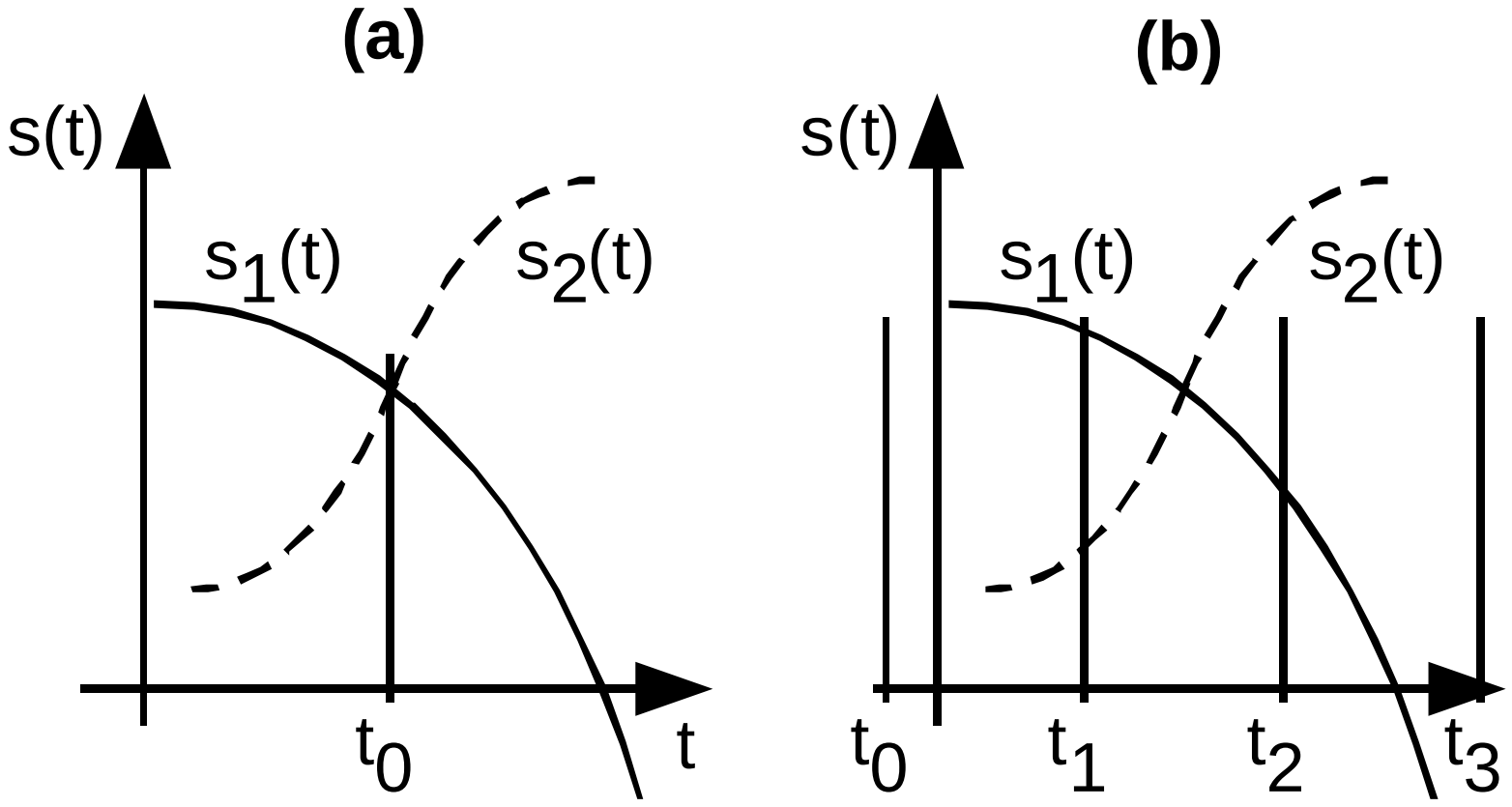
733MHz Intel Pentium III Processor und Windows NT 4.0

CPU Power Consumed at with 2^{15} = 32768 Bit Averager at f_{clk}=20KHz



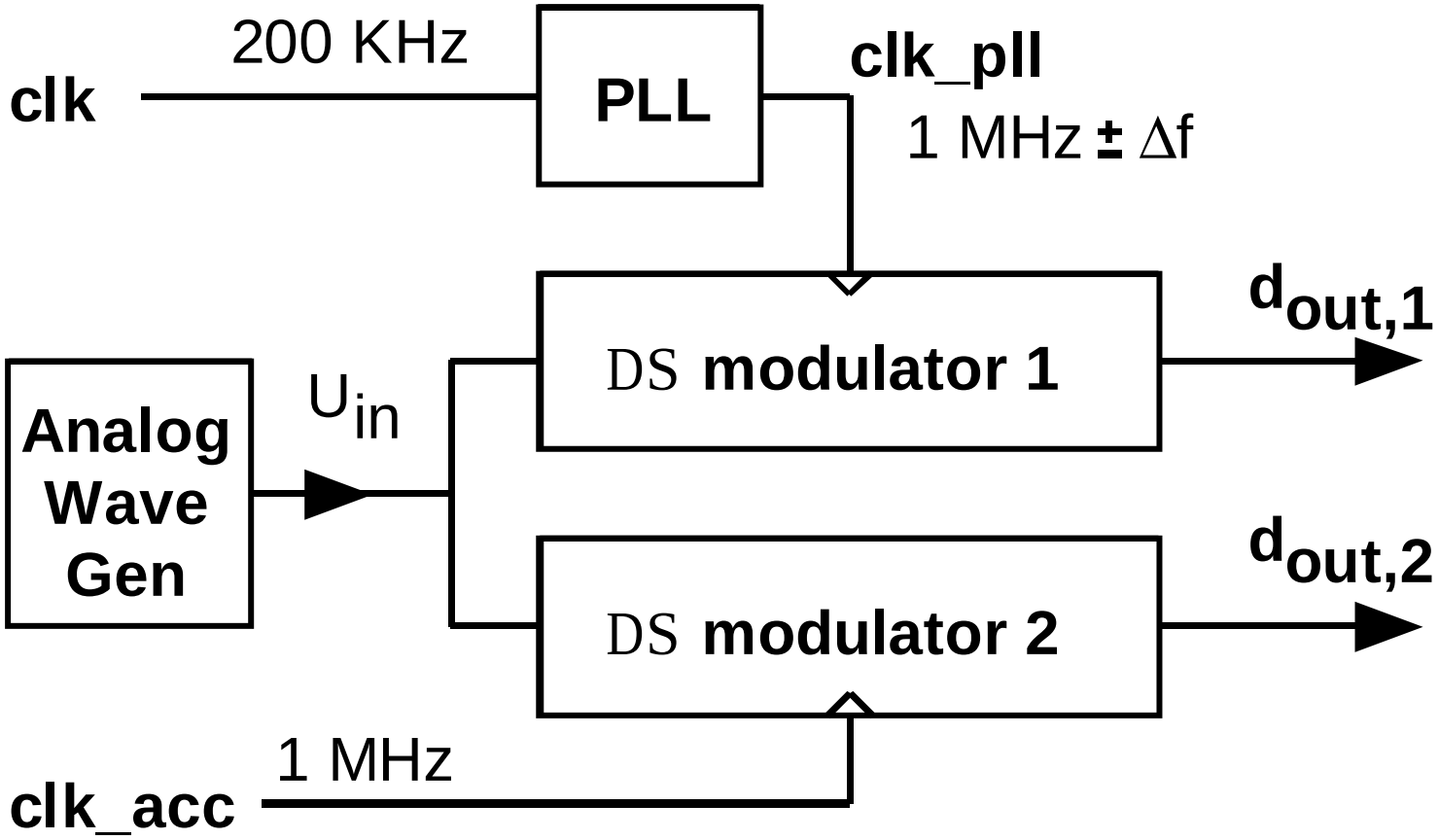
733MHz Intel Pentium III Processor und Windows NT 4.0

New Device: Clocked Comparator



(a) Asynchronous Comparator, (b) Clocked Comparator

Progress: System Composed of PLL and ΣΔ Already Simulated



Employed Phase-Locked Loop [7]