Modeling and Simulation of a Σ - Δ DAC using VHLD-AMS

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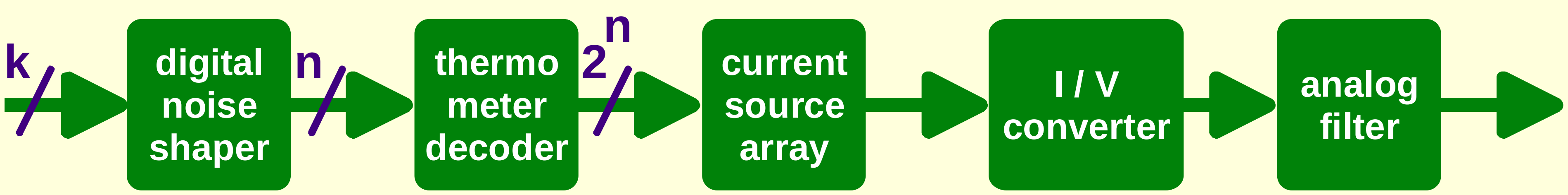
Introduction

- ADC
  - Σ - Δ ADC very popular for mid-range performance (typ. 16 bit, 2 MHz)
  - flash, SAR for high-frequency or high-accuracy
- DAC
  - flash most common
  - Σ - Δ DAC has advantage of low area

Overview

- DAC structure
  - noise shaper
  - thermo decoder
  - current cell array
- Nonidealities
- Evaluation Environment
- Illustration
- Conclusion

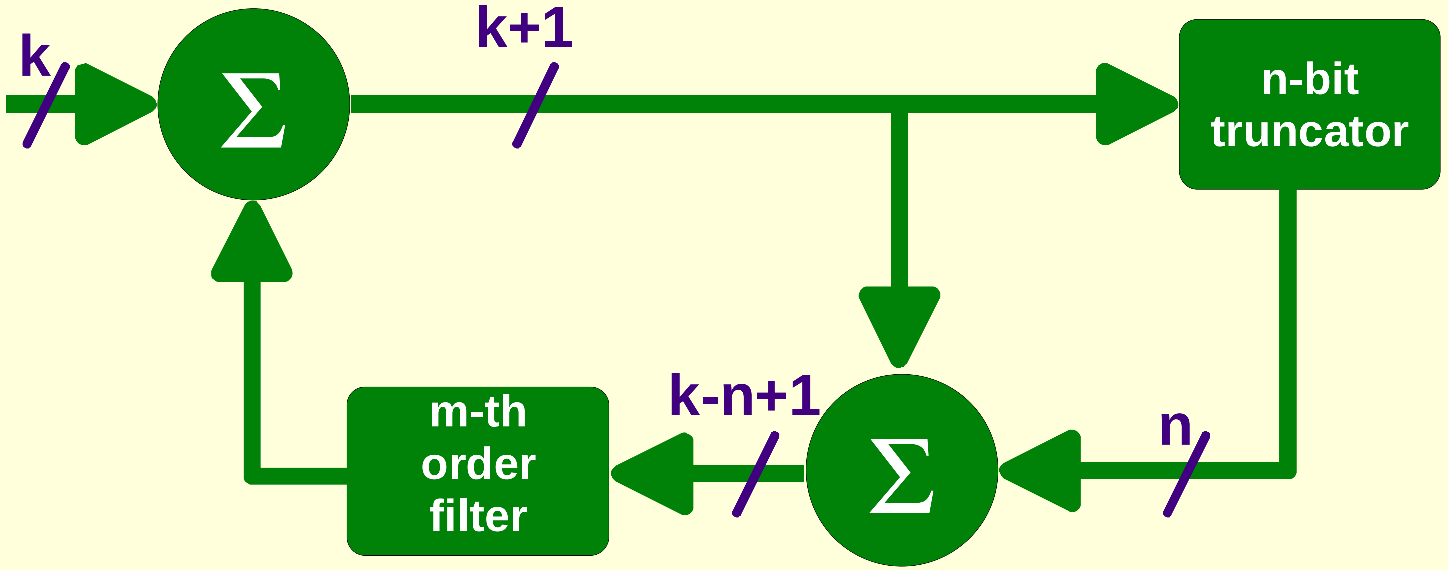
Structure of a Σ - Δ DAC



- Truncation (k>n) :

  ⇒ relatively small area for current source array
- Σ - Δ loop shapes quantization noise

The digital noise shaper

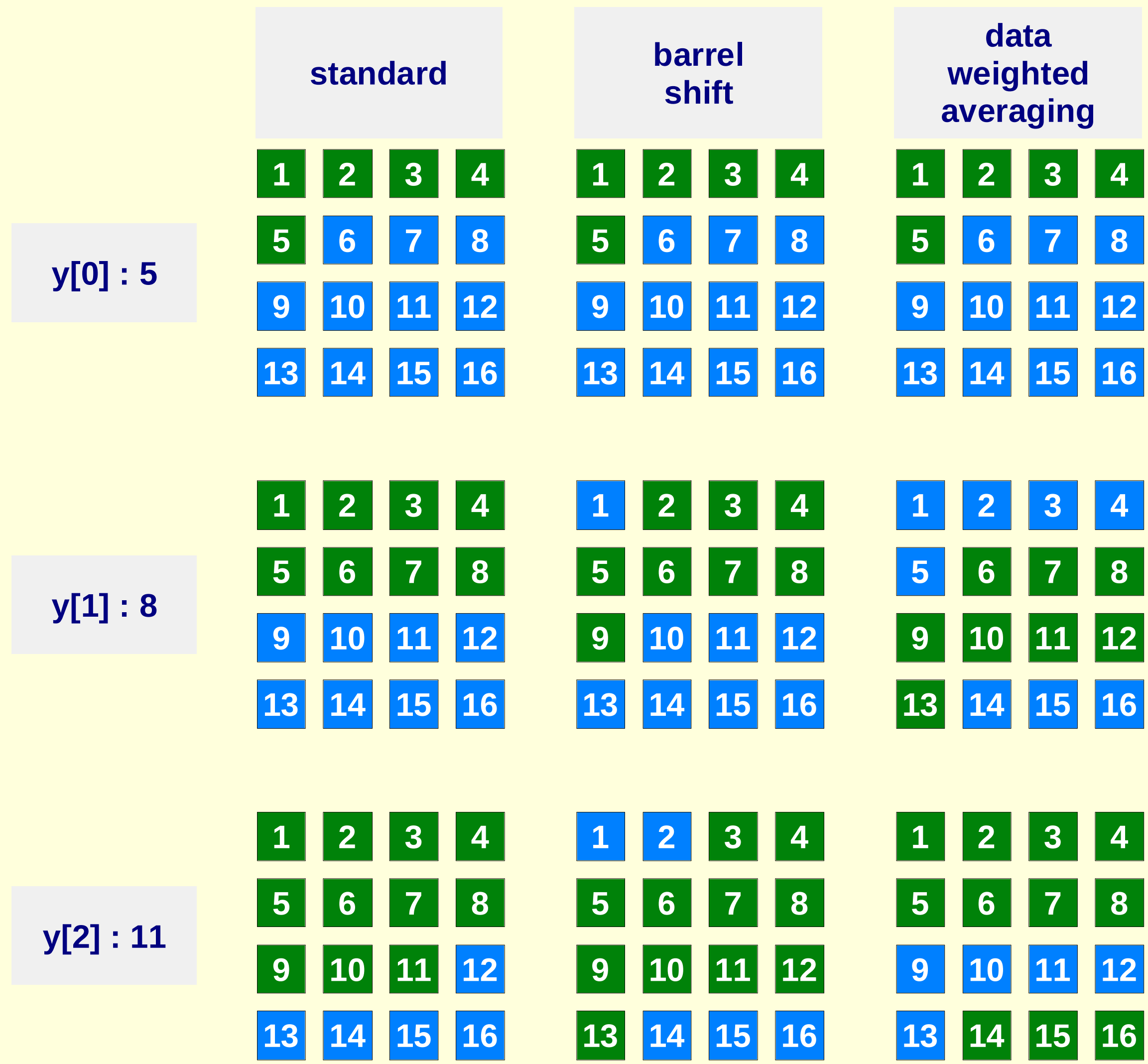


$$Y(z) = X(z) + \left(1 - z^{-1}\right)^m E(z)$$

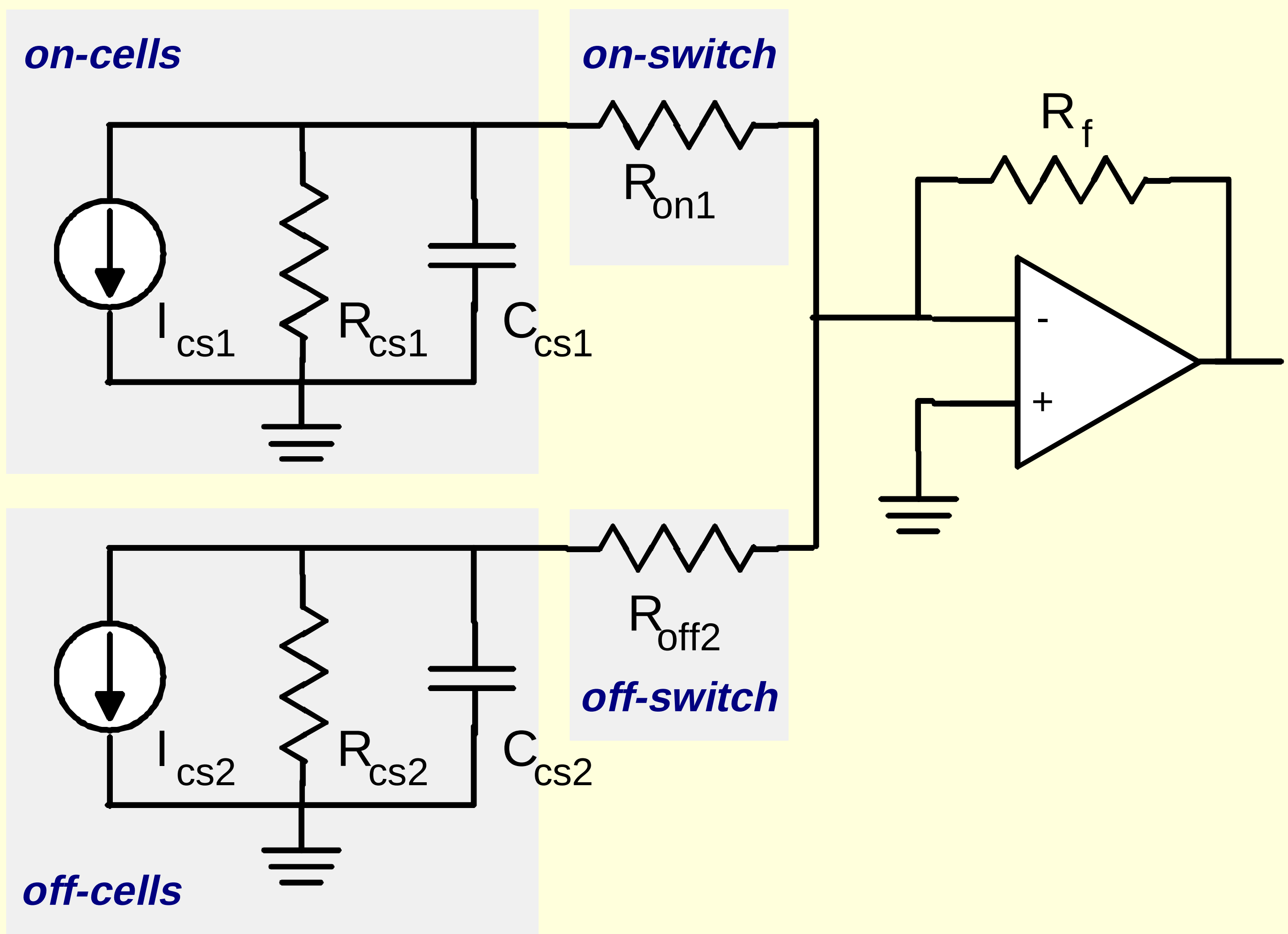
- Limiter prevents overload in filter
- Digital word vs. integer
- Delay in feed-back loop (asynchronous digital logic)

The thermometer decoder

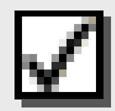
- Fast conversion from analog to digital
- Performance limited by mismatch
- Switching scheme important



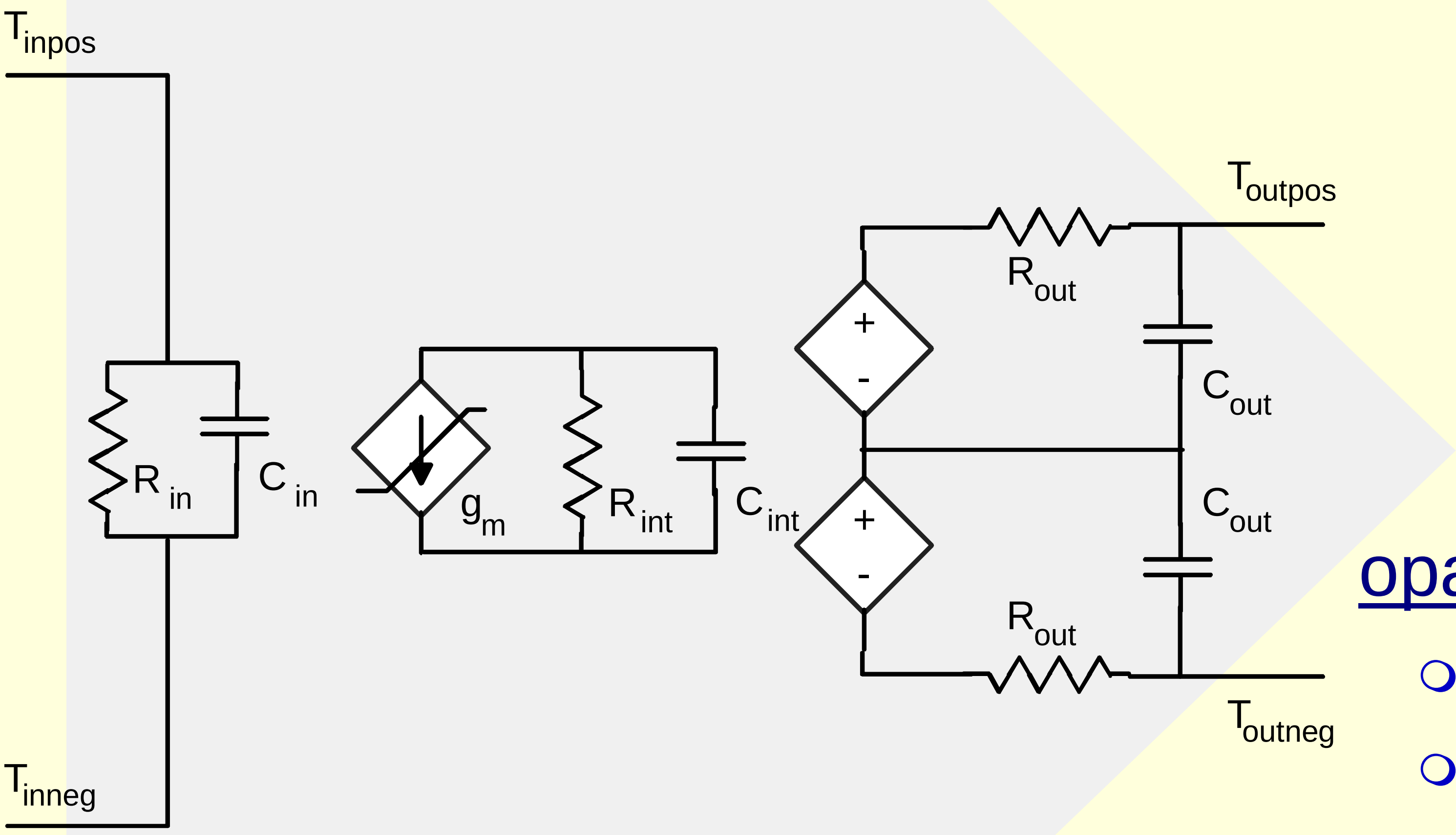
The current cell array



The current cell array (cntd.)

	Lumped model	Distributed model
Evaluation time	Fast	Slow
Accuracy	Moderate	Good
DEM evaluation		

Opamp model



opamp specs

- A_0
- GBW
- SR
- first pole

Overview

- DAC structure
- Nonidealities
  - current cell mismatch
  - settling
  - opamp slew rate
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Current cell mismatch

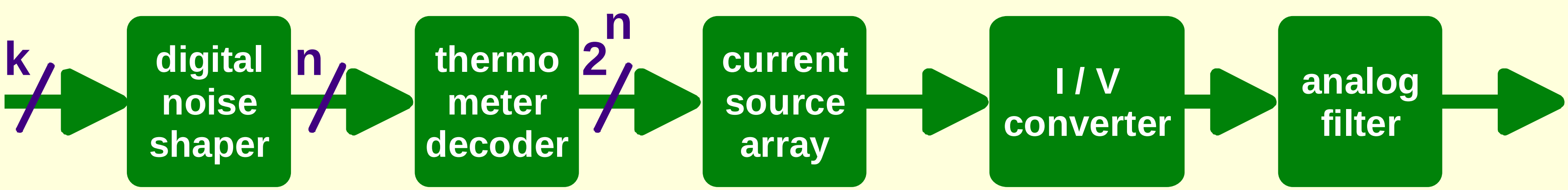
- mismatch consists of systematic and random part

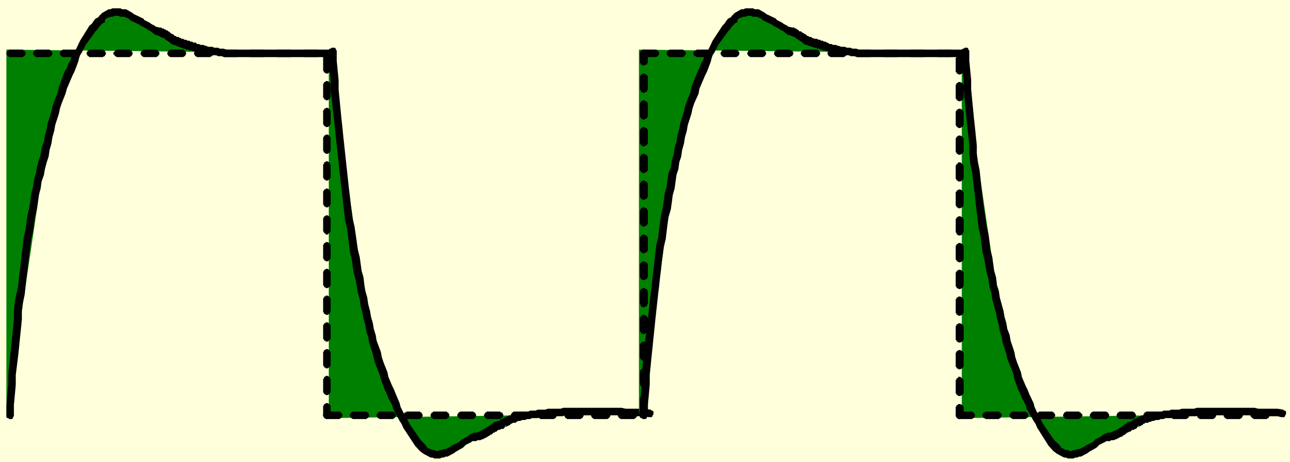
systematic mismatch	linear or quadratic gradient model
random mismatch	use random number generator

- use carefull layout techniques to reduce systematic mismatch
- random mismatch modeled using random number generators

$$\sigma\left(\frac{\Delta I_{out}}{I_{\max - out}}\right) = \frac{1}{2\sqrt{NoLevels}} . \sigma\left(\frac{\Delta I_{cell}}{I_{cell}}\right) . \sqrt{K}$$

Settling of the current cells





Settling of the current cells

- linear analysis
  - transfer from switching current cell to output voltage (simplified)

$$\frac{V_{out}}{I_{cell}} = H_b(s) = \frac{A_f}{s^2 + 2.s.\omega_n.\zeta + \omega_n^2}$$

  - error due to settling :

$$e_{\max} = \frac{1}{2.NoLevels} \int_0^{\frac{1}{f_s}} \left(h_b(t).u(t) - \frac{1}{NoLevels} \right) dt$$

  - this results in a noise power that equals :

$$e_{rms}^2 = \frac{1}{e_{\max}} . \int_0^{e_{\max}} e^2.de = \frac{e_{\max}^2}{3}$$

- nonlinear analysis
  - momentary values for different components depend on the input signal

$\Rightarrow$ transient analysis

Opamp's slew rate

- opamp's slewing modeled by limiting the internal maximal current

- slew rate affects the settling behavior

  $\Rightarrow$ similar calculation method

- linear analysis results in ($SR_n = SR_p$) :

$$e_{\max} = \frac{f_s}{2.NoLevels} \cdot \frac{1}{SR} \cdot \frac{1}{NoLevels}$$

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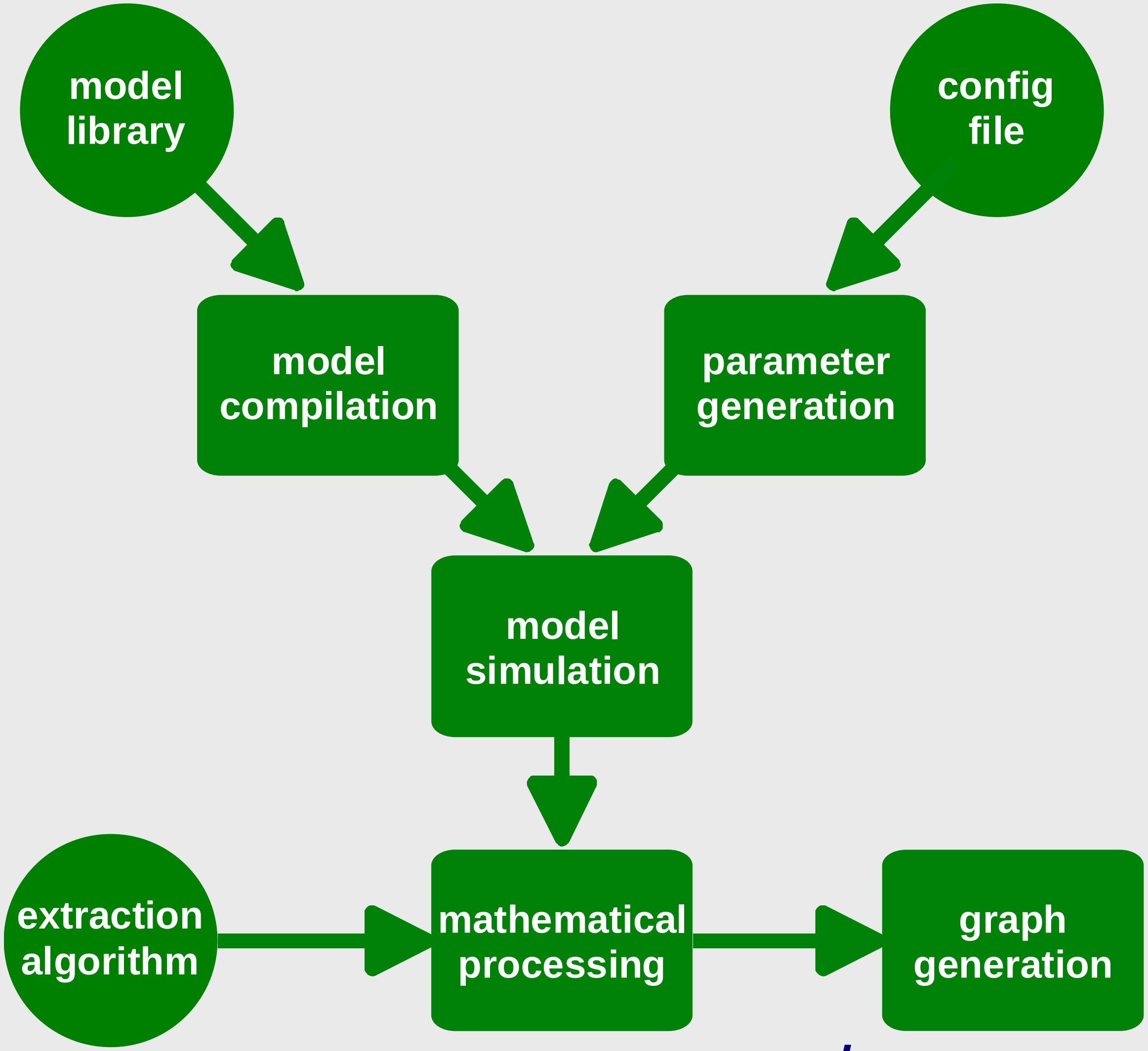
Requirements for evaluation environment

- easy to plug-in specific models for different blocks
- automate simulation and post-processing
- flexibility towards the user to modify post-processing algorithms
- clearly log and track the ongoing evaluation process (also as documentation for later)

Evaluation environment



glue : vamsSweep

Evaluation environment : example

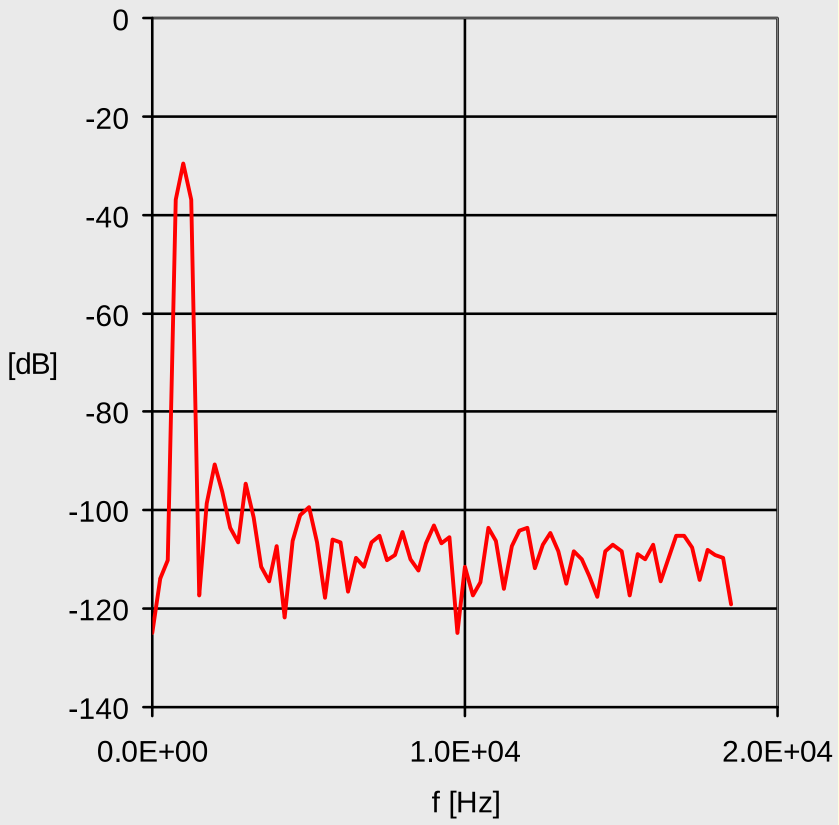
config file

```
% vamsSweep      v1.0.2   configuration file
entityName                TBdac
architectureName          testbench
fixedVariableNames        {amp, freq, rf }
fixedVariableValues       {0.25e0, 1.0e3, 5.0e3}
sweepVariableNames        {pcin}
sweepType                 log
sweepNoP                  10
sweepStart                1.0e-12
sweepStop                 1.0e-11
```

evaluation results

```
1.000000e-12      5.3894127e+01
1.322376e-12      5.4098707e+01
1.748679e-12      5.4182483e+01
2.312411e-12      5.4822368e+01
3.057877e-12      5.5453887e+01
4.043663e-12      5.5488050e+01
```

intermediate result



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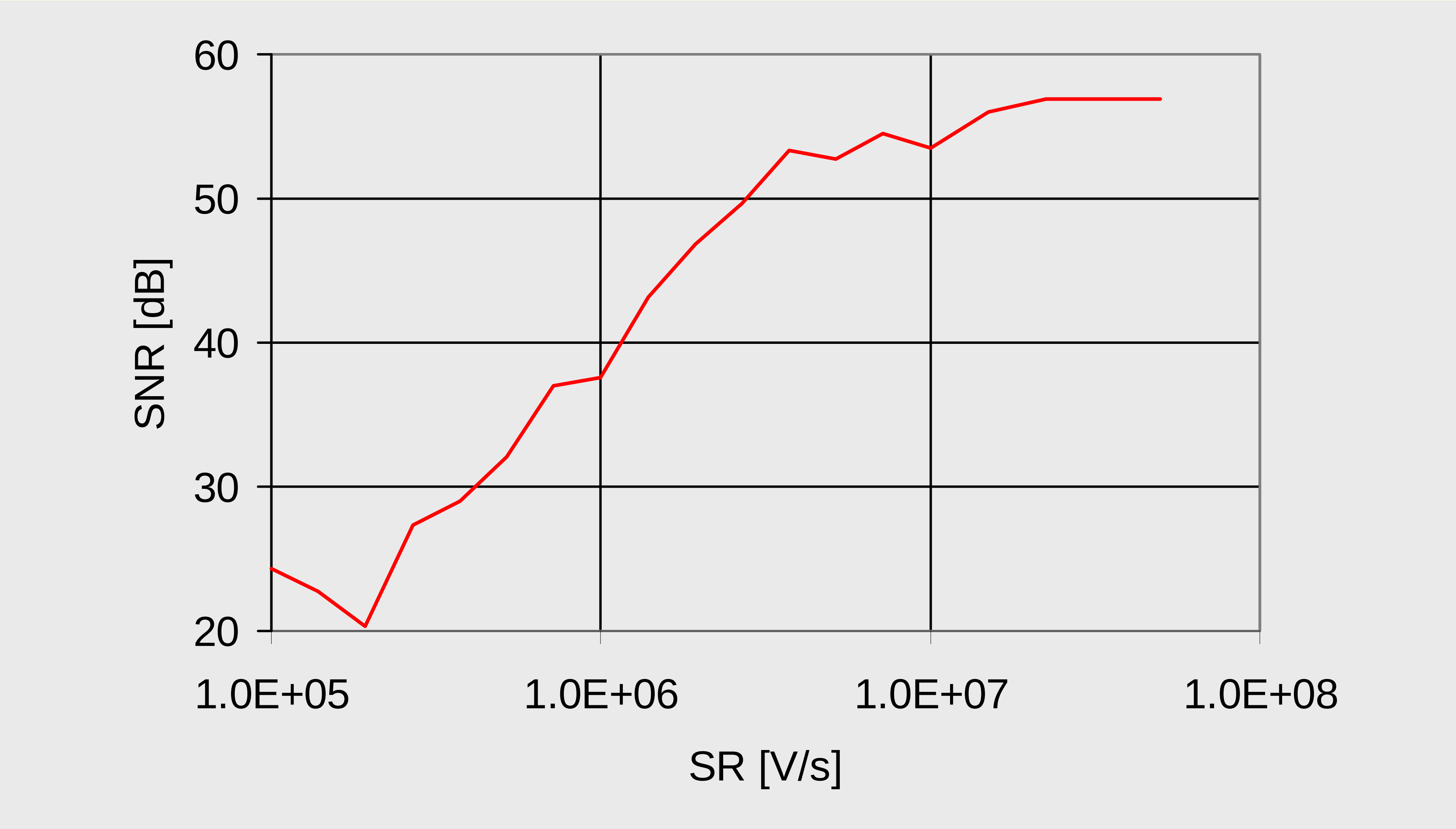
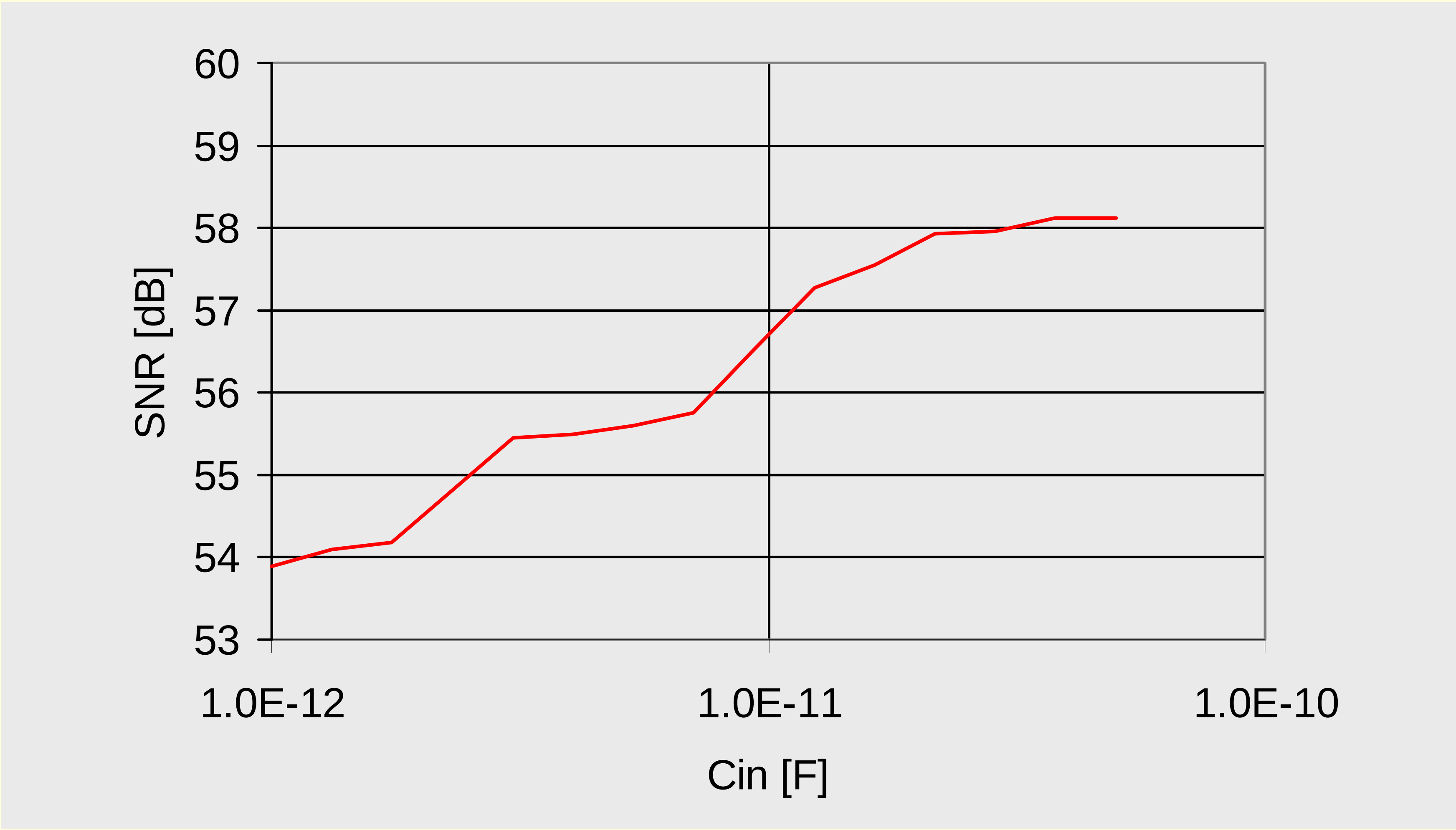
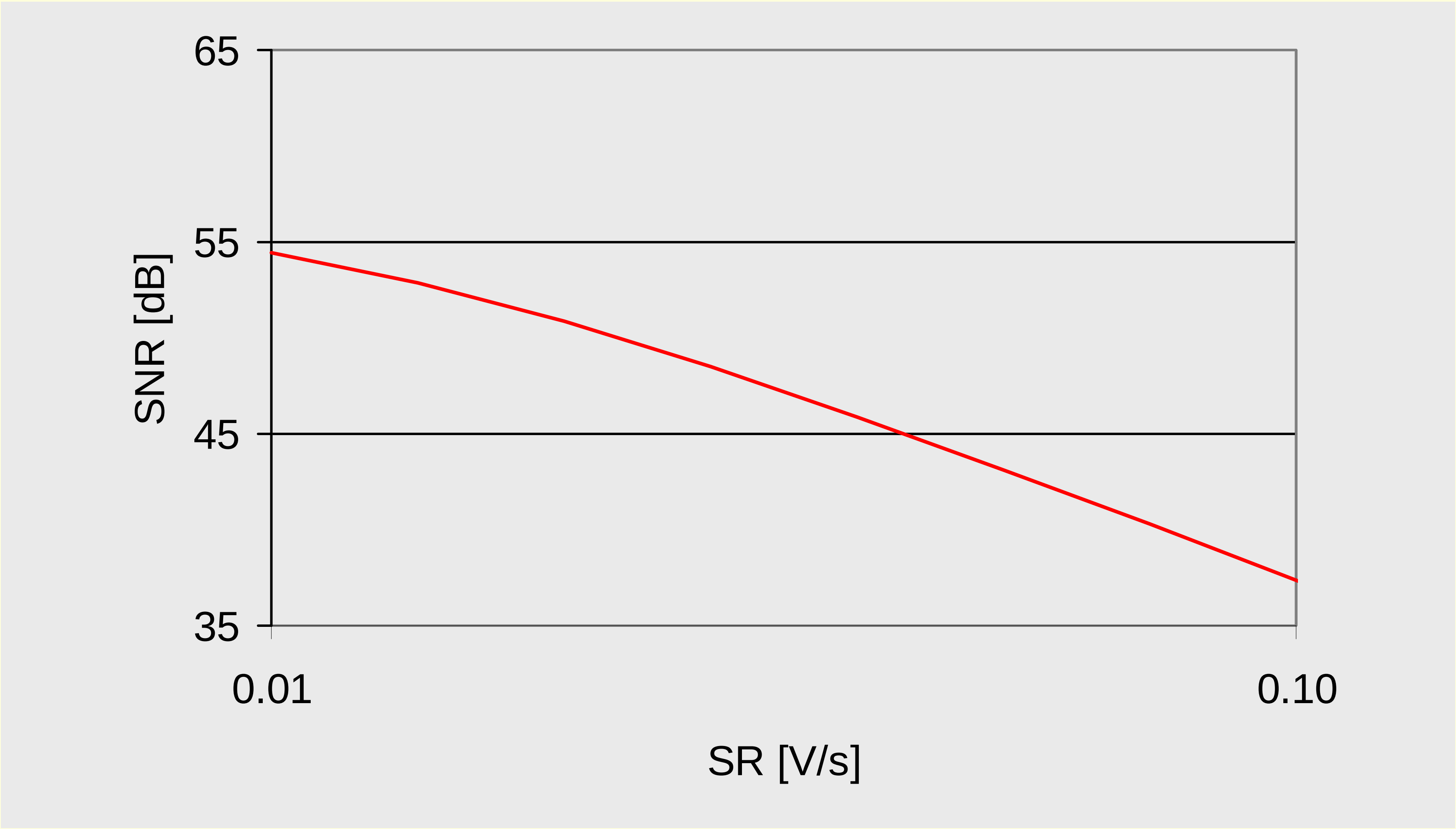
Slew Rate Simulated



Input Capacitance Variation Simulated



Current Cell Mismatch Simulated



Conclusions

- Generation of a library for Σ - Δ DAC building blocks
- Identification and evaluation of the influence of the dominant DAC imperfections on SNR
- Setup of a flexible evaluation environment