UNDERSTANDING THE EFFECT OF CIRCUIT NON-IDEALITIES ON SIGMA-DELTA MODULATOR

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ABSTRACT

The main objective of this paper is to demonstrate and to understand the effect of each common non-idealities in switched-capacitor circuits on sigma-delta modulators. Since quantization process is non-linear in nature, a sigma-delta loop is then inherently non-linear. Therefore, analyzing its non-ideal behaviors would be difficult. A better understanding of these effects can be achieved if each of these non-idealities is studied separately. This paper is an extension and improvement effort of sigma-delta modulator modeling to the one proposed in [1] using MATLAB® and SIMULINK® [2].
Keyword – sigma-delta modulator modeling, circuit non-idealities, over-sampling, noise shaping.

1. INTRODUCTION

Since a sigma-delta modulator loop is non-linear and complex to analyze, the behavioral study of the system and its effect of circuit non-idealities can be done using SIMULINK® and MATLAB® model simulation. This paper starts with a general overview of the second order sigma-delta modulator. Each of the common circuit non-ideality models such as the input sampling clock jitter, switched-capacitor kT/C noise, system dynamic range, integrator gain capacitor mismatch, and operational amplifier parameters such as the finite DC gain, thermal noise, finite bandwidth, and slew-rate will be described in the section follows. The effect of each of these non-idealities is demonstrated using a second-order sigma-delta modulator with 3-bit quantizer at 40MHz clock and with 32 times over sampling ratio (OSR).

2. SECOND ORDER SIGMA-DELTA MODELING

A sigma-delta modulator can be represented as a linear system if the quantization error is assumed to be additive white noise by fulfilling these four assumptions [3]:

(1) All quantization levels are exercised with equal probability.
(2) The quantization steps are uniform.
(3) The quantization error is not correlated with the input signal.
(4) A large number of quantization levels are used.

Referring to (Figure 2.1), the output of the modulator as a function of input signal, X, quantization error as well as other errors at node 3, E_3, other possible errors at node 1, E_1, and node 2, E_2, and the integrator transfer functions, H_1 and H_2, is given by equation (2.1).

$$Y = \frac{X \cdot H_1 \cdot H_2}{1 + H_1 \cdot H_2 + H_2} + \frac{E_1 \cdot H_1 \cdot H_2}{1 + H_1 \cdot H_2 + H_2} + \frac{E_2 \cdot H_2}{1 + H_1 \cdot H_2 + H_2} + \frac{E3}{1 + H_1 \cdot H_2 + H_2} - \frac{E_4 \cdot (H_1 \cdot H_2 + H_2)}{1 + H_1 \cdot H_2 + H_2} \tag{2.1}$$

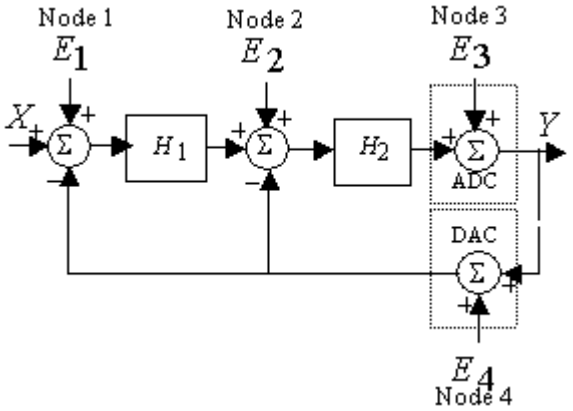

Figure (2.1) Second order sigma-delta modulator model.

The ideal integrators' z-domain transfer function including the necessary closed loop gain are given by,

$$H_1(Z) = 0.5 \cdot \frac{Z^{-1}}{1 - Z^{-1}} \tag{2.2}$$

$$H_2(Z) = 2 \cdot \frac{Z^{-1}}{1 - Z^{-1}} \tag{2.3}$$

Thus, the ideal signal transfer function is given by,

$$STF(Z) = \frac{H_1 \cdot H_2}{1 + H_1 \cdot H_2 + H_2} = Z^{-2} \tag{2.4}$$

Whereas, the noise transfer functions at each node are found to be,

$$NTF_1(Z) = \frac{H_1 \cdot H_2}{1 + H_1 \cdot H_2 + H_2} = Z^{-2} \tag{2.5}$$

$$NTF_2(Z) = \frac{H_2}{1 + H_1 \cdot H_2 + H_2} = 2 \cdot Z^{-1} \cdot \left(1 - Z^{-1}\right) \tag{2.6}$$

$$NTF_3(Z) = \frac{1}{1 + H_1 \cdot H_2 + H_2} = \left(1 - Z^{-1}\right)^2 \tag{2.7}$$

$$NTF_4(Z) = -\frac{H_1 \cdot H_2 + H_2}{1 + H_1 \cdot H_2 + H_2} = -Z^{-1} \cdot \left(2 - Z^{-1}\right) \tag{2.8}$$

Thus, noise at different nodes has different noise shaping functions. However, for any ADC, the ultimate limitation is the quantization noise, when everything else is ideal. As a function of quantization step size, Δ, and over-sampling-ratio, OSR, the quantization noise power for a second-order modulator is given by,

$$P_{Q\varepsilon} = \left(\frac{\Delta^2}{12}\right) \cdot \left(\frac{6}{OSR} - \frac{8 \cdot \sin\left(\frac{\pi}{OSR}\right)}{\pi} + \frac{\sin\left(\frac{2 \cdot \pi}{OSR}\right)}{\pi} \right) \tag{2.9}$$

Assuming the input is a sinusoidal wave and N is the quantizer resolution, the maximum full-scale input signal power is found to be,

$$Ps = \frac{\left(\frac{\Delta \cdot 2^N}{2}\right)^2}{2} = \frac{\Delta^2 \cdot 2^{2 \cdot N}}{8} \tag{2.10}$$

The maximum signal-to-noise ratio of a second order sigma-delta modulator is,

$$SNR_{MAX} = 10 \cdot \log_{10} \left(\frac{\frac{3}{2} \cdot 2^{2 \cdot N}}{\left(\frac{6}{OSR} - \frac{8 \cdot \sin\left(\frac{\pi}{OSR}\right)}{\pi} + \frac{\sin\left(\frac{2 \cdot \pi}{OSR}\right)}{\pi} \right)} \right) \tag{2.11}$$

Figure (2.2) shows the effect of quantizer resolution; for an increment of 12 dB in SNR, quantizer resolution needs to increase by 2-bits. In addition, SNR increases with increasing OSR as shown in figure (2.3).

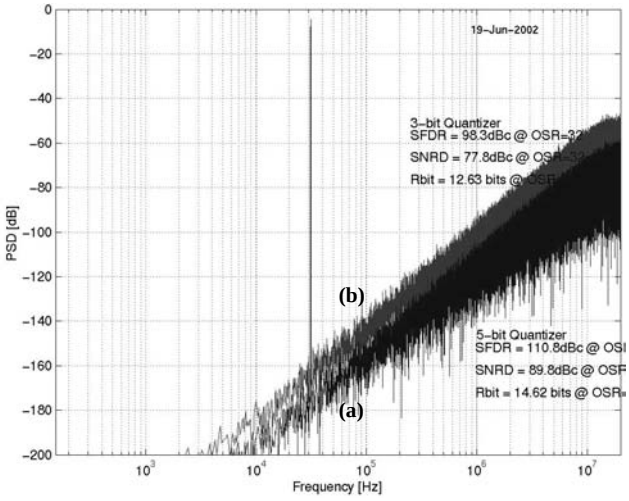

Figure (2.2) Ideal Second Order Sigma-Delta Modulator with OSR = 32: PSD Plot (a) with 3-bit Quantizer, (b) with 5-bit Quantizer.

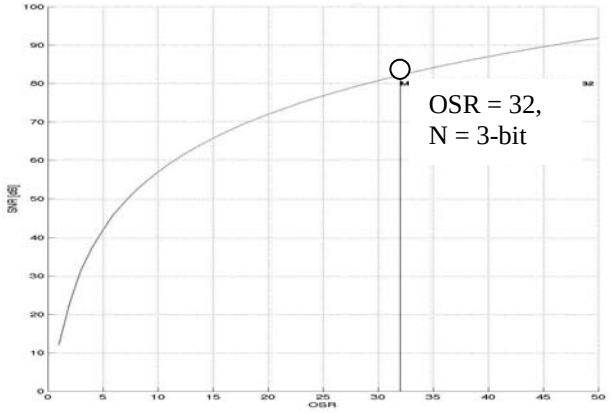

Figure (2.3) Ideal Second Order Sigma-Delta Modulator with 3-bit quantizer: SNR (dB) vs. OSR.

3. ANALOG CIRCUIT NON-IDEALITIES MODELING

Figure (3.1) shows the model of the second order sigma-delta modulator including the analog circuit non-idealities.

3.1 Switched-Capacitor kT/C Noise Model

Since the switched-capacitor kT/C noise is random in nature, this noise can be modeled as a Gaussian random process with unity gain standard deviation and magnitude of,

$$Vn_{SC}(rms) = \sqrt{\frac{kT}{C}} \tag{3.1}$$

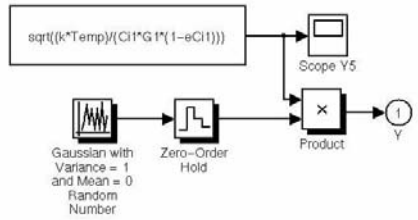

Figure (3.2) Switched-Capacitor kT/C Noise.

3.2 Input Sampling Clock Jitter Model

Input sampling clock jitter cause non-uniform sampling and increases the total noise power in the system.

$$\delta Vin = \delta T \cdot \frac{dVin}{dt} \tag{3.2}$$

Assuming the sampling clock jitter, δT, to be a Gaussian random process with standard deviation, ΔT, and is white, the sampling clock jitter model is given by equation (3.2).

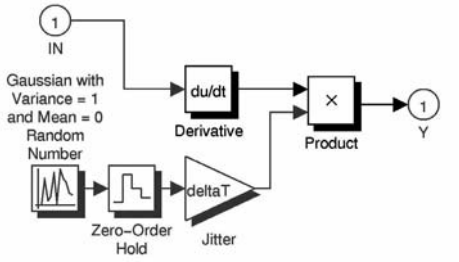

Figure (3.3) Input Sampling Clock Jitter.

3.3 Amplifier Thermal Noise Model

Assuming that the amplifier thermal noise dominates the other amplifier noise such as 1/f noise, this noise can be modeled as a Gaussian random noise with amplitude, *Vni* or *Vno*, depending if it is input referred or output referred, which can be obtained from measurement, circuit simulation or calculation. The 1/f noise is detailed in [8].

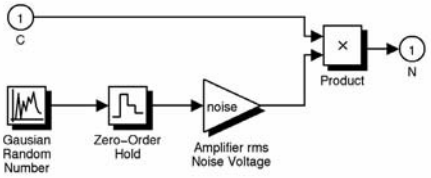

Figure (3.4) Amplifier Thermal Noise.

3.4 Amplifier Slew - Rate and Finite Bandwidth Model

Amplifier slew-rate, SR, dictates the non-linear settling section, *tsl*, of figure (3.5), whereas, the linear settling section, *texp*, is determined by the amplifier finite bandwidth, BW, or time constant, τ. These two regions can be characterized in a piecewise function as described by equation (3.3) [4].

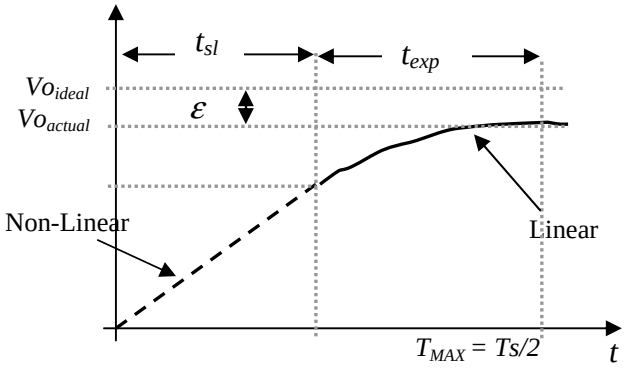

Figure (3.5) Integrator Output Step Response.

$$|\varepsilon| = \begin{cases} |Vin| - SR \cdot T\max & if \quad tsl \geq T\max \\ (|Vin| - SR \cdot tsl) \cdot e^{\frac{-t_{\exp}}{\tau}} & if \quad tsl < T\max \end{cases} \quad if \quad \left|\frac{dVin}{dt}\right|_{t=0} > SR$$

$$|\varepsilon| = |Vin| \cdot e^{\frac{-t_{\exp}}{\tau}} \quad if \quad \left|\frac{dVin}{dt}\right|_{t=0} \leq SR \tag{3.3}$$

3.5 Amplifier Finite DC Gain Model

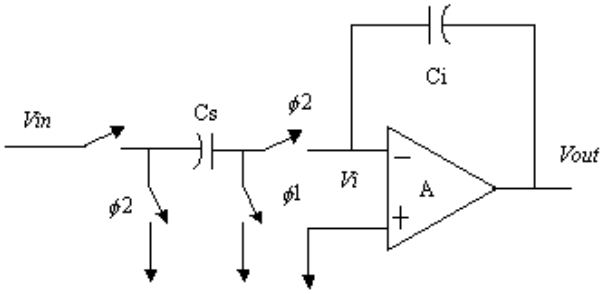

Figure (3.6) Switched-Capacitor Delay Integrator [5].

A commonly implemented switched-capacitor delay integrator, similar to figure (3.6) has the transfer function described in equation (3.4), given as a function of sampling capacitor, Cs, integrating capacitor, Ci, and amplifier finite DC gain, A.

$$\frac{Vout}{Vin} = \frac{\frac{\frac{Cs}{Ci}}{1+\frac{Ci+Cs}{Ci \cdot A}} \cdot Z^{-1}}{1-\left(\frac{\frac{1}{A}+1}{1+\frac{Ci+Cs}{Ci \cdot A}}\right) \cdot Z^{-1}} \tag{3.4}$$

3.6 Gain Capacitor Mismatch, Cs/Ci, Model

If there is a mismatch between the gain capacitors due to layout and silicon fabrication, the ratio of sampling capacitor, Cs and integrating capacitor, Ci, can be given as a function of the ideal gain, G, unit capacitor of the integrating capacitor, C_{Ci}, unit capacitor of the sampling capacitor, C_{Cs}, to be matched with C_{Ci}, and the mismatch error, ε_{Ci}.

$$\frac{Cs}{Ci} = G \cdot \left(\frac{C_{Ci} - (C_{Ci} - C_{Cs})}{C_{Ci}} \right) = G \cdot (1 - \varepsilon_{Ci}) \qquad (3.5)$$

Therefore, substituting equation (3.5) in equation (3.4),

$$\frac{Vout}{Vin} = \frac{\dfrac{G \cdot (1-\varepsilon_{Ci})}{1 + \dfrac{1 + G \cdot (1-\varepsilon_{Ci})}{A}} \cdot Z^{-1}}{1 - \dfrac{\left(1 + \dfrac{1}{A}\right)}{1 + \dfrac{1 + G \cdot (1-\varepsilon_{Ci})}{A}} \cdot Z^{-1}}, \qquad (3.6)$$

or can be rewritten as a gain error, α, and a pole error, β.

$$\frac{Vout}{Vin} = \frac{G \cdot \alpha \cdot Z^{-1}}{1 - \beta \cdot Z^{-1}}, \qquad (3.7)$$

3.7 Non-Ideal Second Order Sigma-delta Modulator

Due to the amplifier finite DC gain and gain capacitor mismatch, the signal transfer function and quantization noise transfer function are found to be (the subscript for G, α, and β indicates that it is in the 1st or 2nd integrator),

$$STF = \frac{G_1 \cdot \alpha_1 \cdot G_2 \cdot \alpha_2 \cdot Z^{-2}}{1 - (\beta_1 + \beta_2 - G_2 \cdot \alpha_2) \cdot Z^{-1} + (\beta_1 \cdot \beta_2 + G_1 \cdot \alpha_1 \cdot G_2 \cdot \alpha_2 - G_2 \cdot \alpha_2 \cdot \beta_1) \cdot Z^{-2}} \qquad (3.8)$$

$$NTF_3 = \frac{1 - (\beta_1 + \beta_2) \cdot Z^{-1} + \beta_1 \cdot \beta_2 \cdot Z^{-2}}{1 - (\beta_1 + \beta_2 - G_2 \cdot \alpha_2) \cdot Z^{-1} + (\beta_1 \cdot \beta_2 + G_1 \cdot \alpha_1 \cdot G_2 \cdot \alpha_2 - \beta_1 \cdot G_2 \cdot \alpha_2) \cdot Z^{-2}} \qquad (3.9)$$

3.8 System Dynamic Range Model

Every single block in the modulator has its own dynamic range. The dynamic range for the amplifier, switch, and quantizer is modeled as a linear transfer function with output saturation or clipping at both positive and negative input ends.

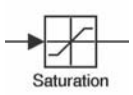

Figure (3.7) Dynamic Range.

4. EFFECT OF ANALOG CIRCUIT NON-IDEALITIES

4.1 Switched-Capacitor kT/C Noise Effect

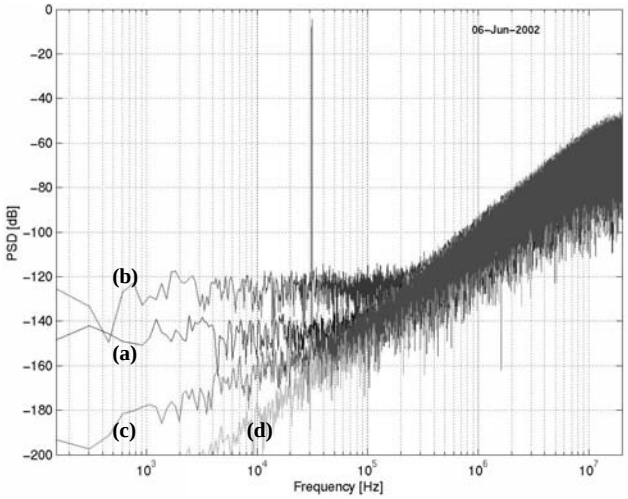

Figure (4.1) Effect of kT/C Noise on PSD.

The PSD of the ideal case shown in figure (4.1.d) with slope of 40dB/decade indicates that the quantization noise has a second order noise shaping over a wide band of frequency only if no other noise dominates. Figure (4.1.a) and (4.1.b) shows that the switched-capacitor kT/C noise from the input sampling switch starts to dominate the noise floor at lower in-band frequency. The kT/C noise increases as the sampling capacitor value is decreased from 6pF to 60fF. Since it is a white noise introduced at the input, it will not be noise shaped. If the kT/C noise at the input of the second integrator is dominating, it is noise shaped to the first order with 20dB/decade slope as shown in Figure (4.1.c) with a sampling capacitor of 4pF. The noise floor increases as the capacitor value decreases. Figure (4.2) shows this effect on SNRD. Since kT/C noise is white, it does not introduce harmonics or tones.

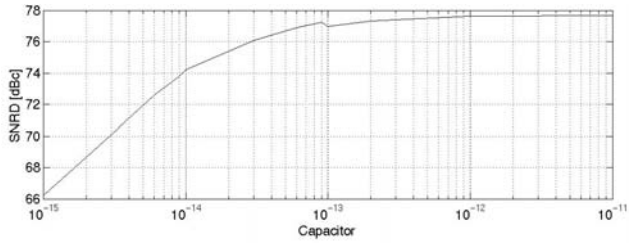

Figure (4.2) Effect of Sampling kT/C Noise on SNRD.

4.2 Input Sampling Clock Jitter Effect

Since it is modeled as white noise, input sampling clock jitter has the same effect as the kT/C noise. Since input sampling jitter only happens at the input, this noise will

not be noise shaped. The noise floor increases as the jitter increases; it starts to affect SNR when its in-band noise power is on the order of the in-band quantization error. Shown in Figure (4.3.a) with 1ns jitter and Figure (4.3.b) with 10ps jitter, input sampling clock jitter noise does not introduce harmonics or tones. Figure (4.4) shows this effect on SNR with jitter from 100 ps to 1 us.

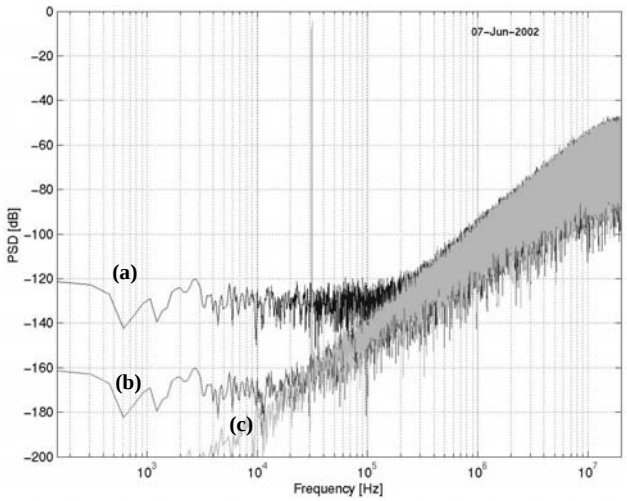

Figure (4.3) Effect of Input Sampling Clock Jitter on PSD.

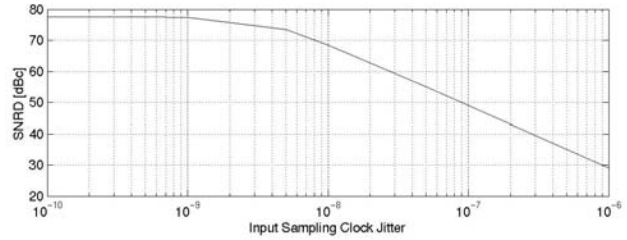

Figure (4.4) Effect of Input Sampling Jitter on SNRD.

4.3 Amplifier Thermal Noise Effect

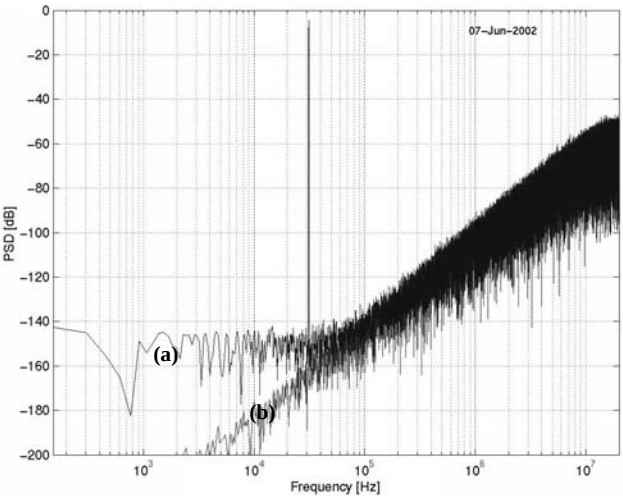

Figure (4.5) Effect of Amplifier Thermal Noise on PSD.

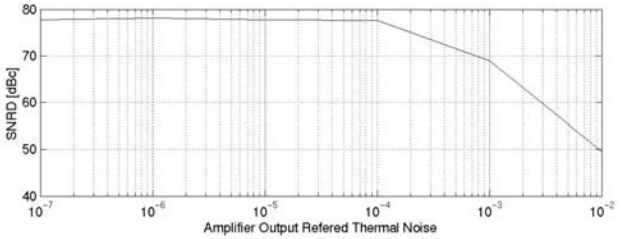

Figure (4.6) Effect of Amplifier Thermal Noise on SNRD.

Since the amplifier thermal noise is white, it has the same effect on SNR as the kT/C noise and input sampling clock jitter. Figure (4.5.a) shows the effect of amplifier thermal noise at the input of the first integrator with input referred noise power, *Vni*, of 10 uVrms. Thus, it is not noise shaped. Figure (4.5.b) shows the PSD of the ideal case.

4.4 Amplifier Slew-Rate Effect - Non-Linear Settling

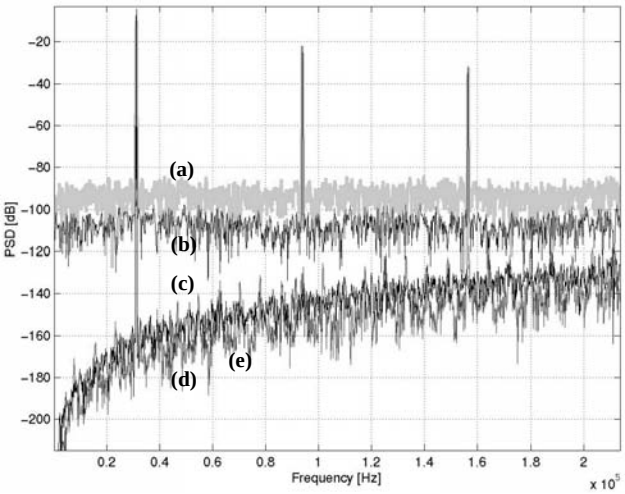

Figure (4.7) Effect of Amplifier Slew-Rate on PSD Plot.

Figure (4.8) Effect of Amplifier Slew-Rate on SNRD.

The slew rate of the amplifier used in Figure (4.7.a) is 50 V/us, Figure (4.7.e) is 500 V/us, and Figure (4.7.c) is without slewing. Figure (4.7.d) is for signal with 40 dB less than Figure (4.7.a). The raised noise floor has no noise shaping since the slewing error is introduced in the first integrator. When a 5-bit quantizer is used instead of 3-bit, the noise floor is reduced while the harmonics remain as shown in Figure (4.7.b). From these five figures, we can

infer that insufficient amplifier slew rate introduces harmonics and raises the noise floor. Figure (4.8) illustrates the relation between SNRD and the slew rate. The noise floor and harmonic distortion increases as the slew rate is decreased.

4.5 Amplifier Finite Bandwidth Effect – Linear Settling

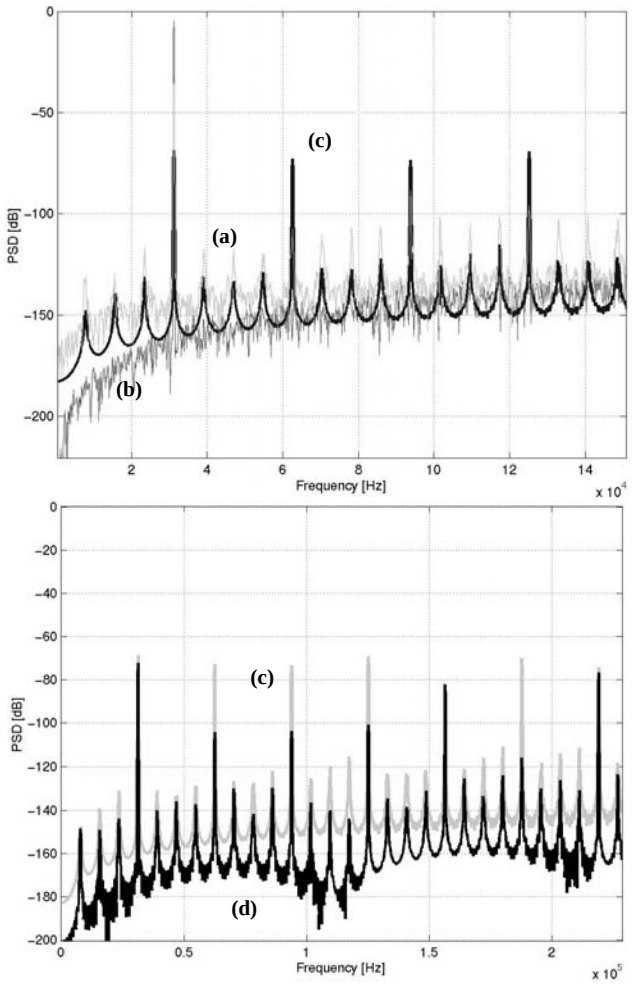

Figure (4.9) Effect of Amplifier Finite Bandwidth on PSD.

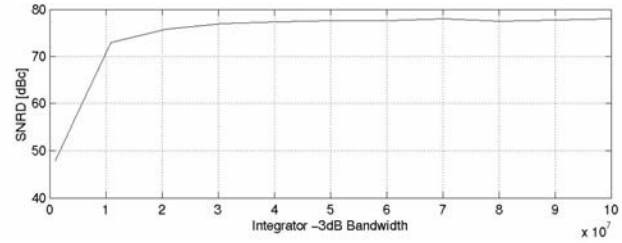

Figure (4.10) Effect of Finite Bandwidth on SNRD.

When an amplifier with –3 dB closed-loop bandwidth of 1 MHz is used in the first integrator instead of an ideal one as in Figure (4.9.b), Figure (4.9.a) with -4.5 dBFs input signal amplitude and Figure (4.9.c) with -44.5 dBFs input signal amplitude, shows that the amplifier finite bandwidth raises the system noise floor, which will affect the SNR. The effect of linear settling is quite similar to the effect of a DC gain. It causes imperfect noise shaping or noise leakage. In reality, the sigma-delta modulator is non-linear. In order to perceive it having the characteristics of a linear system, the four assumption made in section two has to be constantly met. As the linear settling error increases beyond a certain point when this approximation (assumption (1) and (4) in section 2) does not hold very well, noise that looks like tones starts to appear periodically. This effect is shown in figure (4.9.a) and worse in Figure (4.9.c). Sometimes, this noise is wrongly perceived as harmonics when the tones are exactly at the harmonics of the signal. However, by comparing Figure (4.9.a) to Figure (4.9.c), if the signal amplitude is changed, the amplitude of these noise tones will change inversely proportional. Thus, it is different from harmonic distortion whose the amplitude changes proportionaly with signal amplitude. A dithering technique can be used at the quantizer in order to make the quantization noise more random or "white". For simplicity, it can be demonstrated in Figure (4.9.d) that using a higher resolution quantizer (5-bit) can reduce the amplitude of this harmonic noise in Figure (4.9.c). Figure (4.10) shows that the SNRD performs better as the linear settling or the amplifier bandwidth improves.

4.6 Amplifier Finite DC Gain Effect

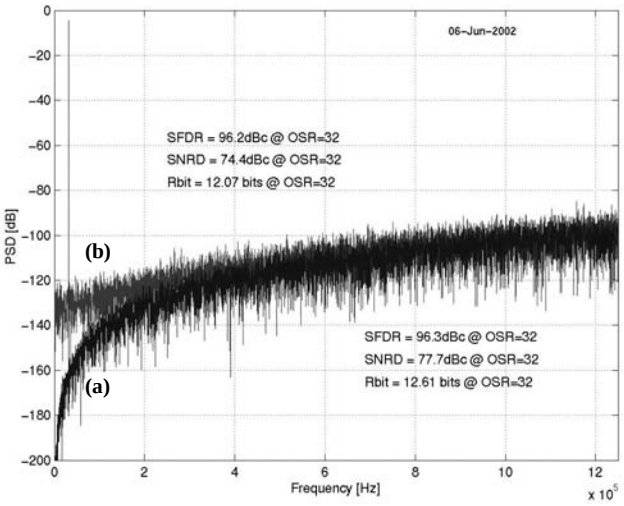

Figure (4.11) Effect of Amplifier Finite DC Gain on PSD.

Compared to an amplifier with finite DC gain of 100 dB in Figure (4.11.a), Figure (4.11.b) shows that with low amplifier finite DC gain of 20 dB the system noise floor increases, which will affect the SNR, but not the SFDR. The increase of the noise floor is due to quantization noise or any other noise not properly shaped. This effect is called noise leakage. Figure (4.12.a) shows the ideal case,

Figure (4.12.b) uses a finite DC gain amplifier in the first integrator, Figure (4.12.c) uses a finite DC gain amplifier in the second integrator, and Figure (4.12.c) uses an amplifier with finite DC gain in both the first and second integrator.

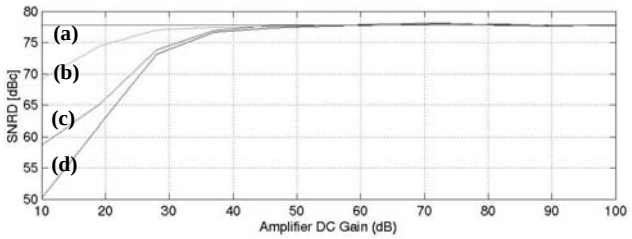

Figure (4.12) Effect of Amplifier Finite DC Gain on SNRD.

4.7 Gain Capacitor Mismatch, Cs/Ci, Effect

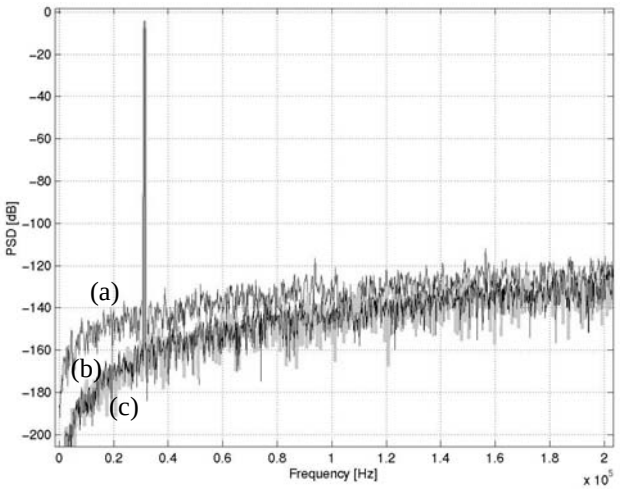

Figure (4.13) Effect of Gain Capacitor Mismatch, Cs/Ci on PSD.

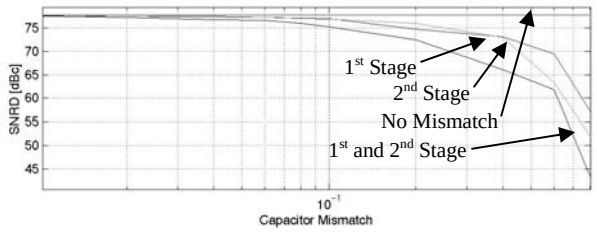

Figure (4.14) Effect of Gain Capacitor Mismatch, Cs/Ci on SNRD.

The gain capacitor mismatch causes an increase in the noise floor due to noise leakage. If the capacitor mismatch gain is more, distortion might occur due to dynamic range limitation. If the gain is less, the assumption of quantization error as noise might not hold. Thus noise might appear as tones. SFDR starts to deteriorate as the capacitor mismatch increases over 10% of matching, which is shown in Figure (4.13.b) while Figure (4.13.a) is with 40% mismatch. Capacitor mismatch for a second order modulator are less sensitive compared to MASH architecture. A MASH modulator needs the noise transfer function in the digital domain to exactly cancel the noise transfer function in the analog domain [4]. Power spectral density with no capacitor mismatch is shown in Figure (4.13.c). Figure (4.14) shows the effect of gain capacitor mismatch at different integrator stages. The integrator gain and quantizer gain will affect the net gain in the feedback loop. With lower net gain, the circuit will responds sluggishly to changing input while too high of a gain will cause the output to be unstable [6].

4.8 System Dynamic Range Effect

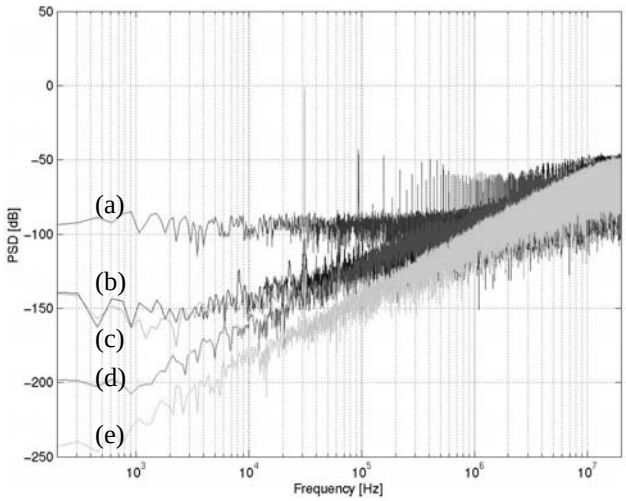

Figure (4.15) Effect of System Dynamic Range on PSD.

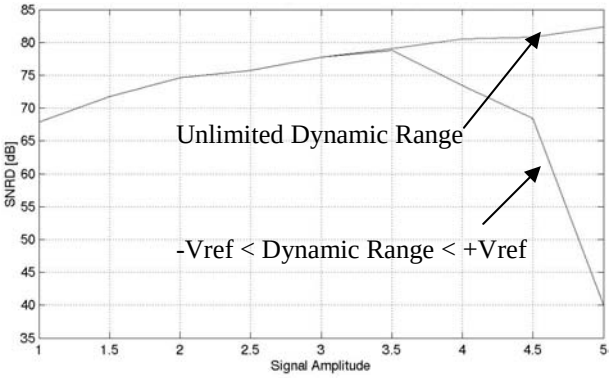

Figure (4.16) Effect of System Dynamic Range on SNRD.

Due to the fact that a 0 dbFs signal will clip at ±Vref (in this case, Vref = 5 V) of the dynamic range, the noise floor and harmonic distortion will increase compared to the ideal modulator with unlimited dynamic range. Figure (4.15.a) shows the effect of signal clipping in the first integrator, Figure (4.15.b) shows the effect of signal clipping at the switch after the first integrator, Figure

(4.15.c) shows the effect of signal clipping in the second integrator, Figure (4.15.d) shows the effect of signal clipping at the switch after the second integrator and in the quantizer, and Figure (4.15.e) show the PSD of and ideal modulator with unlimited dynamic range. The relation between SNRD and signal amplitude is shown in Figure (4.16) for a system with unlimited dynamic range and system with dynamic range of ±Vref.

5. SUMMARY

Table 5.1 shows the summary of the effect of circuit non-idealities on second-order sigma-delta modulator. These models can be used to analyze and help design any other more complex types of sigma-delta modulators.

Non-Idealities	Effects
Switched-Capacitor kT/C Noise	SNR
Input Sampling Clock Jitter	SNR
Amplifier Thermal Noise	SNR
Amplifier Slew-Rate	SNR/SFDR/THD
Amplifier Finite Bandwidth	SNR/SFDR
Amplifier DC Gain	SNR
Intergr. Gain Cap. Mismatch	SNR/SFDR/THD
System Dynamic Range	SNR/SFDR/THD

Table 5.1 Effects of the Non-Idealities on Second Order Sigma-Delta Modulator.

6. REFERENCES

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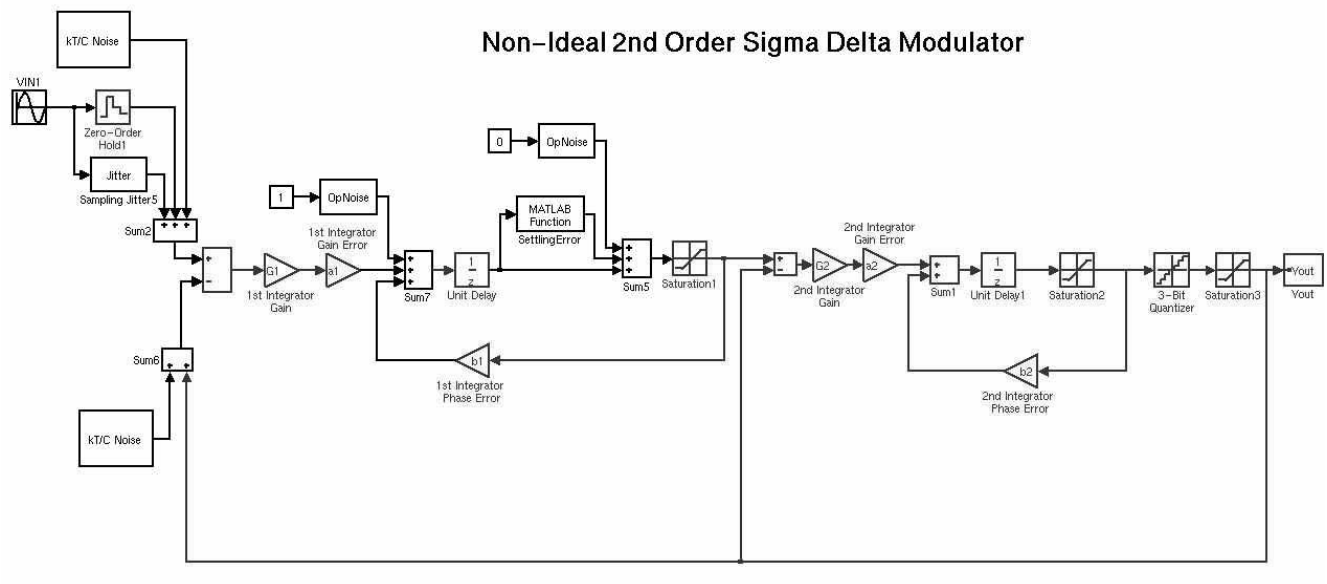

Figure (3.1) Simulink Model for Second Order Sigma-Delta Modulator with 3-bit Quantizer