A nonlinear simulation model for integrated Hall devices in CMOS silicon technology

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Abstract

A new simulation model for Hall devices in CMOS silicon technology is proposed. Nonlinearities caused by effects, as back-bias and vertical field-effect, transient effects caused by parasitics and wide operational range in temperature were taken into account and implemented in VHDL-AMS. Behavioral equations and parameters are based on fundamental theory of Hall devices and semiconductor physics and verified experimentally. Comparisons between simulation and measured behavior of productive ICs were done to prove the correctness and completeness of the implemented set of equations and the high accuracy of this model. To distinguish the benefits of the proposed model, simulations with the current Hall models are done with the same setups.

Introduction

Increasing requirements for the precision of integrated sensors, new techniques in electrical circuit design and the growing importance of Hall devices as sensor cells, lead to the necessity of a precise simulation model for silicon implementation of these sensors. Their compact size, high accuracy and low prize, highly integrated Hall sensors become more and more attractive for a wide range of applications. To stay attractive in price and satisfy all future customer's requirements in functionality, performance and stability, silicon CMOS or BICMOS technologies are the first choice for mass production of Hall sensors.

Although, the physical functionality of Hall devices is very well studied and known, almost all currently used spice simulation Hall models basically are restricted to linear behavior. Junction effects and vertical charge carriers distributions haven't been taken into account, yet. Compared with measurements, such simulations can show discrepancies up to 20-30% in full range operation.

The shape of an integrated Hall sensor cell is similar to a diffused resistor, that possesses two additional orthogonal contacts for the measurement of the Hall voltage. The technical realization of an integrated Hall device, provides a variety of top view shapes, starting from a circle, over a rectangle up to a Greek cross (fig.1). Symmetric shapes are recommended.

The cross section of an integrated Hall device is shown in

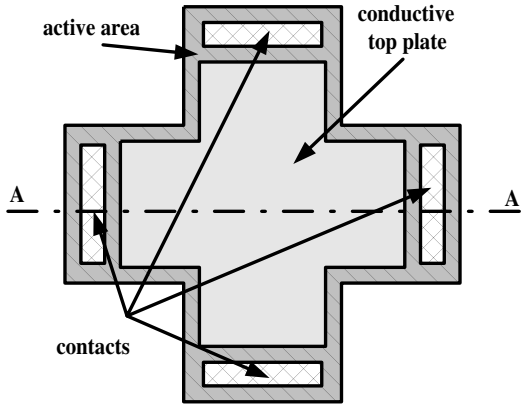

Figure 1: Top view of a Hall device with a Greek cross shape, which can be viewed as a resistor extended by two additional orthogonal contacts for the Hall voltage measurement.

fig.2. The Hall plate is usually implemented as a lowly doped diffusion area in the silicon substrate or epi layer. In order to decrease the flicker noise, a conductive top plate often covers the active area [5], as shown in fig.1 and fig.2. Generally, there are two ways to obtain a conductive top area: either, junction isolated, using an additional highly doped diffusion areas, or dielectric isolated, using polysilicon or metal layers. The basic properties of the Hall sensor cell, are their resistivity *R*, current related sensitivity *Si* or voltage related sensitivity *Su* and given by [1],

$$R = \frac{1}{q \cdot \mu \cdot N_q \cdot t} \left(\frac{l}{w}\right)_{eff} \tag{1}$$

$$Si = \frac{1}{B}\frac{\partial U_{ha}}{\partial I}. \tag{2}$$

$$Su = \frac{1}{B}\frac{\partial U_{ha}}{\partial U}. \tag{3}$$

Both sensitivity definitions are transformed into each other using

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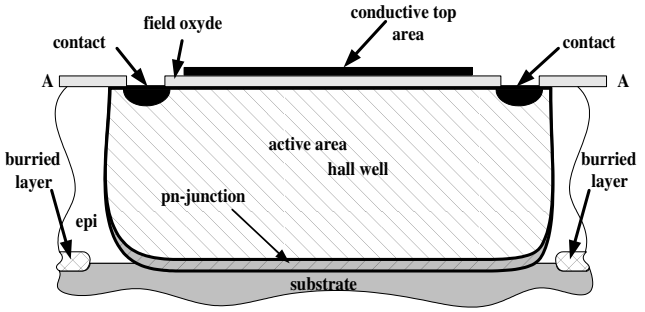

Figure 2: Cross section A - A shows the depth profile of a unbiased Hall device in a sandwich structure of different layers. Appropriate bias voltages establish junction isolation of the active area, causing depth modulation and nonlinearities.

$$R = \frac{Si}{Su}. \tag{4}$$

Used names and symbols are:

q *elementary charge (*$1.603 \cdot 10^{-19} C$*)*
μ_q *mobility of charge carriers*
N_q *doping concentration*
t *depth of Hall device*
l *length of Hall device*
w *width of Hall device*
B *applied magnetic field flux density*
R_H *Hall's constant*

$$R_H = \frac{r_h}{q \cdot N_q} \tag{5}$$

U_{ha} Hall Voltage

$$U_{ha} = \frac{R_h}{t} \cdot I \cdot G \tag{6}$$

r_H *scatter factor depending on doping concentration and temp. (*$0.2 \leq r_H \leq 1.7$*)*
I *applied current*
G *geometry factor (*≤ 1.0*)* [9]

Besides the basic structure of a Hall device, parasitics like diodes and capacitances are a direct consequence of its silicon realization. They limit the performance of modern offset reduction techniques, like the spinning current method [2][4], which require switching and are thus sensitive for parasitic capacitors, that have to be recharged after each switching operation. Further, different potentials of all involved layers cause undesirable nonlinear effects. As a result, the output signals suffer from strong nonlinearities and temperature dependencies. Common accuracy requirements for sensors in automotive applications, are below 1% of tolerance. However, both, the pn-junction and the potential differences between active area and top plate, cause nonlinearities in the output signal up to $9\%/V$ in the resistance and up to $7\%/V$ in the sensitivity of a Hall sensor cell. Concerning the whole operational range in temperature between -50°C and 180°C, all effects become even worse. It is obvious that used linear simulation models cannot satisfy accuracy requirements on sensor ICs.
The set of behavioral equations for the proposed model is based on the fundamental theory of Hall devices [1] and the basics of semiconductor physic[11]. It was verified experimentally. Not only the main effects were taken into account, but also their interdependencies. All experimental investigations were done on a wafer chuck to avoid mechanical stress in packaged ICs [6].
Hall device models in the literature [3] consider effects of large magnetic flux densities up to several tesla. They consider the concentration of the charge carriers on one side of the Hall device in case of high flux densities and account the mobility reduction with the increasing carrier density. The interaction between them increases and their mobility decreases. However, in most common applications, we find magnetic flux densities up to $\approx 200mT$, e.g. in strong permanent magnets. Investigations with $B = 250mT$ haven't shown any changes in the device resistivity nor in device's sensitivity! This effect wasn't implemented in this Hall model.

Back-Bias Effect[1]

Considering eq.1 and eq.2, the only parameter which is able to vary during operation, is the depth *t* of the Hall well. It is changed by the voltage dependent thickness of depletion zone of the reverse biased junction, which consists of two parts, that grow into the two inversely doped areas, respectively. The higher the difference in the inverse doping concentration, the deeper the pn-junction grow into the lower doped area. In case of a doped Hall device, the junction part, that grows into the Hall well is given by [7]:

$$y_q = \sqrt{\frac{2\epsilon_{Si} N_{\overline{q}} (\Phi - U_{pn})}{q N_q (N_{\overline{q}} + N_q)}} = \sqrt{k_2 (\Phi - U_{pn})}, \tag{7}$$

with

$$k_2 = \frac{2\epsilon_{Si} N_{\overline{q}}}{q N_q (N_{\overline{q}} + N_q)}. \tag{8}$$

U_{pn} is the voltage drop on the junction and $\Phi \approx 0.7V$ its diffusion potential. Further, $\epsilon_{Si} = \epsilon_0 \cdot \epsilon_r(Si) = \epsilon_0 \cdot 11.7$. $N_{\overline{q}}$ denotes the doping concentration of the substrate. Thus, the depth *t* extends to
$t_{eff} = t - y_q$.
For the calculation of the effective current through a voltage driven Hall device, with depth *t* and width *w*, we need further:

$\vec{I} = \vec{j} \cdot w \cdot t$
$dU = \vec{E} \cdot d\vec{x}$
conductivity: $\sigma = q \cdot N_q \cdot \mu_q$
current density: $\vec{j} = q \cdot N_q \cdot \mu_q \cdot \vec{E}$

With $t = t_{eff}$, $k_1 = \sigma \cdot w$ and $U_{pn} \rightarrow U_{pn}(x)$, we obtain

$$k_1 (t - \sqrt{k_2 (\Phi - U(x))}) dU(x) = I \cdot dx \tag{9}$$

[1] based upon the pn-junction field effect of MOSFETs

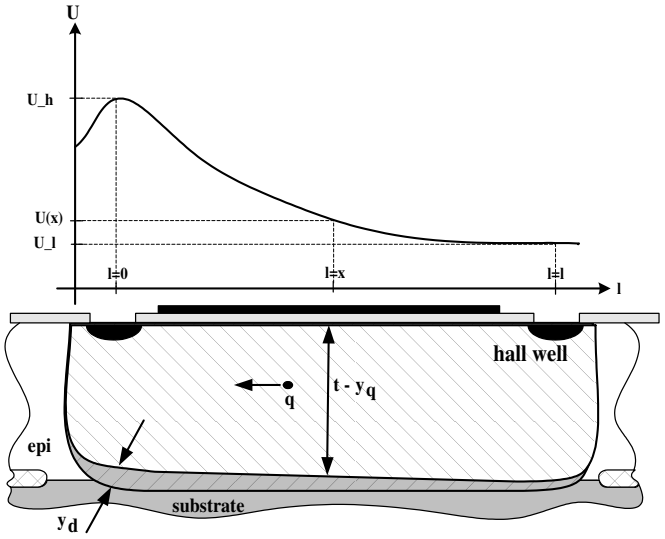

Figure 3: Thickness distribution y_d of the depletion zone and the applied voltage drop. The thickness consists of two parts, in respect to the p- and n-doped area. Responsible for the back-bias effect is the part, which grows into the Hall well.

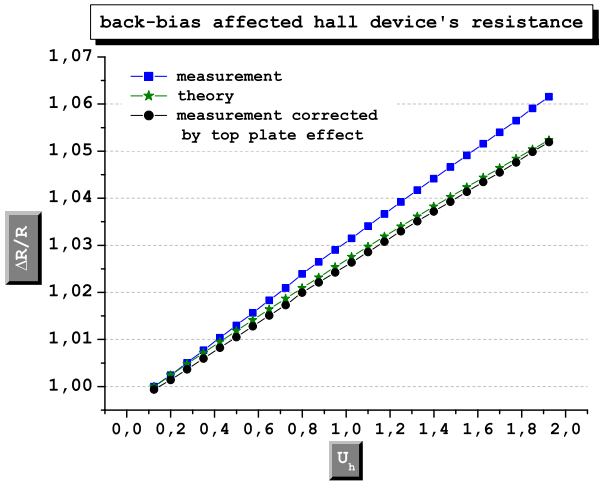

Figure 4: Back-Bias affected Hall device's resistance up to a voltage drop of 2V. The small gap ($\approx 1\frac{\%}{V}$) between measurement and theory was caused by the top-plate bias effect, which will be discussed later. U_l was set to zero.

$$\int_{U_h}^{U_l} k_1(t-\sqrt{k_2(\Phi+U(x))})dU(x) = \int_{l}^{0} I\cdot dx$$

$$\begin{aligned} I \;=\; & \frac{1}{3l}k_1[3t(U_h-U_l) \\ & -2(\Phi+U_h)\sqrt{k_2(\Phi+U_h)} \\ & +2(\Phi+U_l)\sqrt{k_2(\Phi+U_l)}] \end{aligned} \tag{10}$$

Assuming values for $N_q \approx 10^{16}\frac{1}{cm^3}$, $N_{\overline{q}} \approx 10^{15}\frac{1}{cm^3}$, both, theory and measurement can be compared with each other. In fig.4, R is obtained by dividing $(U_h - U_l)$ with eq.10.

Simulation models of Hall devices are built of networks of several resistors, whose currents can now be calculated using eq.10. Current models consist of a 4-resistor network, arranged as a Wheatstone Bridge. Each resistor is diagonal placed between two contacts. Modern connectivity topologies showed the insufficiency of such networks and lead to the necessity to extend the resistor network in size and arrangement. To decrease computation time, the equation for current calculation should be simplified.
Let's assume, $I\cdot dx \to l\cdot dI$ and $U_h - U_l = U_{pn}$. Hence, eq.9 can be rewritten as:

$$k_1(t-\sqrt{k_2(\Phi+U_{pn})})dU_{pn} = l\cdot dI \to$$

$$\frac{dU_{pn}}{dI} = R(U_{pn}) = \frac{l}{k_1(t-\sqrt{k_2(\Phi+U_{pn})})} \tag{11}$$

A Taylor expansion up to second order with Lagrange's reminder term of third order leads to.

$$R(U_{pn}) = \sum_{n=0}^{2}\frac{1}{n!}\frac{\partial^n R(U_{pn})}{\partial U_{pn}^n}(U_{pn}-0)^n$$
$$+\frac{1}{3!}\frac{\partial^3 R(\xi)}{\partial U_{pn}^3}(U_{pn}-0)^3 \quad with \quad \xi\in[0,U_{pn}]$$

$$\Longrightarrow R(U_{pn}) = \underbrace{\frac{l}{k(t-\sqrt{k_2\Phi})}}_{R_0} + \underbrace{\frac{1}{2}\frac{l\sqrt{k_2\Phi}}{k(t-\sqrt{k_2\Phi})^2\Phi}}_{R_0\cdot BBR1}U_{pn}$$
$$+\underbrace{\frac{-\frac{1}{8}\frac{l\sqrt{k_\Phi}}{k(t-\sqrt{k_2\Phi})\Phi^2}+\frac{1}{4}\frac{lk_2}{k(t-\sqrt{k_2\Phi})^2\Phi}}{t-\sqrt{k_2\Phi}}}_{R_0\cdot BBR2}U_{pn}^2 + O(U_{pn}^3) \tag{12}$$

Equation 12 is a simplification of eq.10, and has a polynomial shape, which is easy to calculate and decreases the number of needed coefficients in the implementation of the back-bias effect. R_0 is the unbiased Hall device resistance and its voltage dependence, described by the two back-bias coefficients BBR_1 and BBR_2. These parameters can be easily determined by special measurements. With technological values for doping concentration, mobility, conductivity and geometrical dimensions of the Hall device, all values can be calculated theoretically using eq.12 and proved with measurement results. Theoretical calculated values nicely fit the measurement results in magnitude and sign:

- $R_0 \approx 8k\Omega$, $BBR_1 \approx 8\frac{\%}{V}$ and $BBR_2 \approx -1\frac{\%}{V^2}$

As well as Hall device's resistance, their sensitivity is subject to these back-bias mechanisms and can be calculated in the same way. Using eq.2 and eq.6, which was extended by the voltage dependent thickness of the depletion zone t_{eff}, and a Taylor expansion result the values for the sensitivity and its back-bias coefficients

- $Si_0 \approx 400V/A/T$, $BBS_1 \approx 8\frac{\%}{V}$ and $BBS_2 \approx -1\frac{\%}{V^2}$.

However, the calculated back-bias coefficients diverge more than 30% from measurement. The reason of the mismatch is the geometrical gradient of the hall voltage, which has its maximum in the middle of the Hall device and decreases to the

borders [10]. Experimentally measured values for sensitivity and their back-bias coefficients can also be implemented as a polynomial of higher order.

$$Si(U_{pn}) = Si_0 \cdot (1 + BBS_1 \cdot U_{pn} + BBS_2 \cdot U_{pn}^2). \quad (13)$$

Top-plate bias effect

Another important effect in the functionality of Hall devices, is the depth modulation of the charge carriers by vertical electrical forces. To decrease flicker noise [5], Hall devices are usually shielded by a conductive plate, which is connected to a bias voltage. Negative chosen top plate voltages, prevent a concentration of charge carriers on the surface of the active area. As a consequence, another depletion zone grows with the negative strength of the top-plate potential (fig.5). In this manner, the effective Hall well depth is additionally reduced by the thickness of the depletion zone, which is caused by the negative top-plate potential and can be theoretically described with:

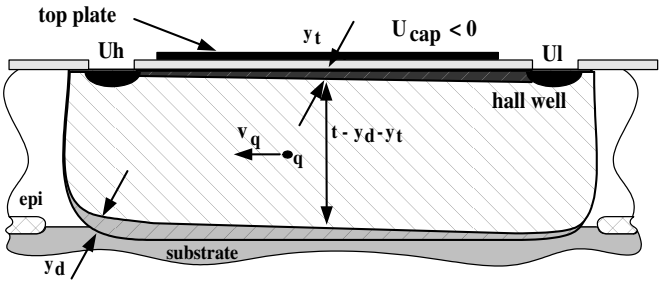

Figure 5: Depletion zone growth on top of the active area as a function of the applied top plate potential.

$$t_{eff} = t_{eff}(U_c) = t_{eff} \cdot (1 + \Theta_1 \cdot U_c + \Theta_2 \cdot U_c^2), \quad (14)$$

where t_{eff} is the Hall well depth, decreased by the applied back-bias effect and Θ_i are coefficients depending on doping concentration of the active zone. U_c is the applied voltage on the top plate. Values for Θ_1 are in the magnitude of $0.01\%/V$ and for Θ_2 of $0.0001\%/V^2$. Substituting eq.1 with eq.14, we obtain:

$$R(U_{pn}, U_c) = \frac{1}{q \cdot \mu \cdot N \cdot t_{eff}(U_c)} \left(\frac{l}{w}\right)_{eff} = \frac{R(U_{pn})}{(1 + \Theta_1 \cdot U_c + \Theta_2 \cdot U_c^2)} \quad (15)$$

Due to the equivalent dependency of the Hall well thickness, current related sensitivity S_i (eq.2) can be given by

$$Si(U_{pn}, U_c) = \frac{R_H \cdot G}{t_{eff}(U_c)} = Si(U_{pn}) \cdot (1 + \Theta_1 \cdot U_c + \Theta_2 \cdot U_c^2) \quad (16)$$

The potential of a conductive top plate additionally changes vertical potential distribution of the pn-junction voltage in the active area. Thus, it's possible to enhance and attenuate the back-bias effect by controlling the top plate potential. To figure out the impact of top plate potential on the back-bias effect, we appoint for every resistive back-bias coefficient

$$BBR(U_c)_i = BBR_i \cdot (1 + \alpha_1 \cdot U_c + \alpha_2 \cdot U_c^2) \quad (17)$$

and in sensitive case

$$BBS(U_c)_i = BBS_i \cdot (1 + \beta_1 \cdot U_c + \beta_2 \cdot U_c^2). \quad (18)$$

Measured values for α_1 and β_1, showed a magnitude of $\approx 1\%/V$ and for α_2 and β_2 a magnitude of $\approx 0.1\%/V^2$.

Temperature Effects

As well known, parameters of semiconductor devices have strong but well defined temperature dependencies. The reasons for the strong dependency were extensively studied before and can be found in literature on solid state physics [8]. The main aspect is the increasing number of charge carriers in the conductive band with increasing temperature and is described by Arrheniu's equation for doped silicon,
$N_q(T) = \frac{N_q}{2 \cdot \exp\left(\frac{E_F - E_i}{kT}\right) + 1}$.
E_F denotes Fermi level of doped silicon, E_i is the energy of the conduction band, k equals Boltzmann constant, T is the absolute temperature and N_i the intrinsic charge carriers concentration.
Additional, the temperature characteristics of the charge carrier mobility in a semiconductor device is strongly dominated by several scatter mechanisms:

- phonon scattering
  - optical phonon scattering $\mu_o \propto T^{1/2}$
  - accustical phonon scattering $\mu_a \propto T^{-3/2}$
- scattering on ionized impurity atoms $\mu_i \propto T^{3/2}$

In conclusion, temperature affected properties are charge carrier concentration and mobility. This leads to the fact, that both, Hall device's parameters like resistivity, sensitivity and all their bias coefficients should show a temperature dependency. Such effects can easily be implemented in VHDL-AMS as constants by using standard spice-model syntax, with a reference temperature of $27°C$:

$$BBR_1(T) = BBR_1(T_{27°C}) \cdot (1 + \sum_{i=1}^{n} Tcbbr_i (T - 27°C)^i) \quad (19)$$

Parasitics

The sandwich structure of the integrated Hall plate with its several layers also results in undesirable parasitic devices. Namely, in capacitors and diodes, that affect especially the transient behavior of the Hall device. The layers: conductive top plate, field oxide (FOX) and Hall-well (fig.2), form a simple linear capacitor of the value $C_{FOX} = \epsilon_0 \epsilon_f \frac{A_c}{d}$. ϵ_f denotes

the dielectric constant of the FOX and d its thickness. A_c is the whole area of the conductive plate. Common values are in the magnitude of several hundred fF - big enough to limit the switching frequency for the spinning current offset reduction method [2] [4]. The depletion zone, caused by the top plate potential, form an additional serial MOS-capacitor with a negligible value.
The dominant parasitic device is the reversed biased pn-junction between active area and substrate. Diodes affect the functionality in two ways: they have a voltage dependent pn-capacitance and they produce leakage currents, that dramatically increase on temperature. The theoretical equations for the pn-capacitor value and its voltage dependency, can be found in [7]. Increase of leakage current in temperature can be taken from [11].

$$C_{pn} = C_{j0}\left[1 - \frac{U_{pn}}{\Phi}\right]^{-m} \quad I_{pn} = I_0\left[e^{\frac{q}{kT}U_{pn}} - 1\right], \qquad (20)$$

where U_{pn} denotes the pn-voltage, C_{j0} is the pn-capacitance with $U_{pn} = 0V$. $\Phi_0 \approx 0.7V$ is the already introduced diffusion potential and m is a constant of $1/3 - 1/2$, which describes the profile of the pn-junction. Further, I_0 is the leakage-current of the diode. Spice simulation models for linear capacitors and diodes are available as spice standards. To take this parasitics into account, both models were attached to the proposed Hall model.

Macro Model of a Hall Device

The new macro model of a Hall device has a hierarchical structure. The inner core consists of a resistor network. Current Hall models have a network of four equal resistors, which are connected between the device ports as a Wheatstone Bridge. However, experimental results show the necessity to expand this network by additional resistors [5]. Each resistor is implemented with its figured out nonlinearities and temperature dependencies. Optional, a parallel flicker and thermal noise source can be attached. Alternative noise simulations can be performed by attaching noise sources to the symbol of the Hall device in the schematic view. Behavioral equations of each resistor, concerns all in the paper presented nonlinear effects.

The next level of the model deals with the calculation of the Hall voltage. It is implemented as a voltage source between the inner and the outer nodes of the model. Their calculation is a product of nonlinear implemented sensitivity, cumulated voltage drop or current, as a result from the resistor network, and the applied magnetic flux density.
The top level of the model, defines the model ports of the schematic symbol view and works as a interface between the inner behavioral model levels and the schematic circuit. All models of presented parasitics, has specific parameter sets and are attached to the top level ports. Further, it is the model reference for the spice simulator and called in the netlist.

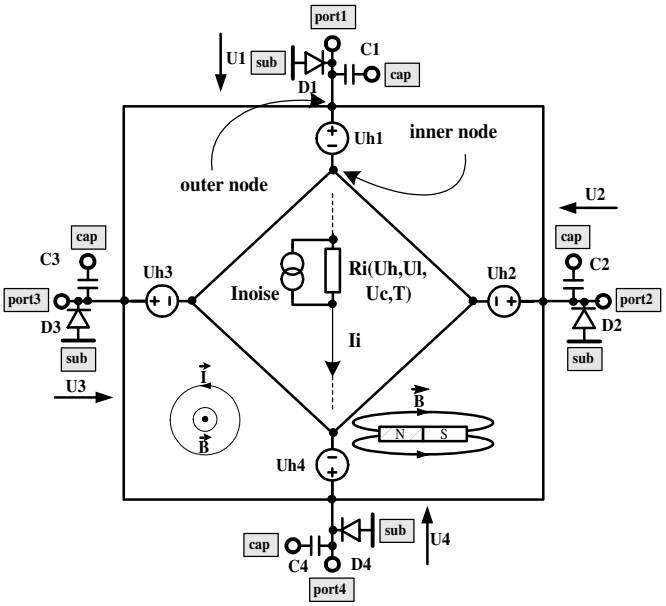

Figure 6: Hierarchical macro model for the implementation of the behavioral VHDL_AMS code. Inner core consists of a resistor network, followed by the Hall voltage circuit. Parasitics are attached to the model ports.

Simulation Results

The new model code was written in VHDL-AMS and includes in its current version more than 50 behavioral parameters and coefficients. First performance tests of the new Hall model included simulations of certain measurement setups during the parameter extraction. To show the correctness and accuracy of the model, in a second step, simulations of arbitrary connected Hall devices were performed and compared with the equivalent measurements. To distinguish the benefits of the proposed Hall model, corresponding simulations with old Hall models were performed and added to every simulation plot. Calculated errors are discrepancies between measurement and the equivalent simulation with the new Hall model.

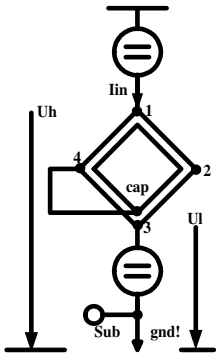

Figure 7: Measurement setup for the extraction of the back bias effect. U_h was swept from 50mV to 2,15V. U_l was set to be always 100mV lower than U_h.

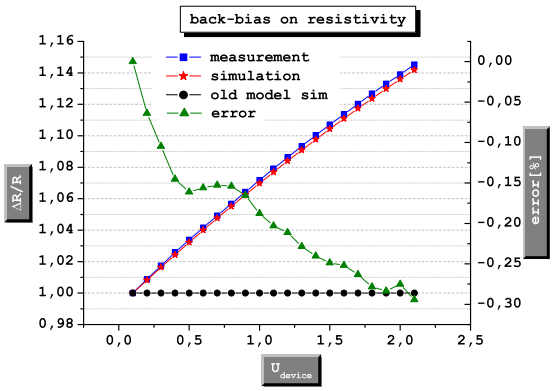

Figure 8: Back-Bias verification with simulations of the back-bias effected model resistors. Remaining gap with higher input voltage was caused by the influence of the conductive top plate.

The back-bias measurement setup for the parameter extraction was chosen in a way, to cancel out all other effects, as far as possible. However, a negligible part of $\approx 0.1\%/V$ remains (see fig.8).
Besides the nonlinearities caused by biasing, temperature simulations of the device's sensitivity behavior are getting a more important role during the design phase of future sensor ICs. In current models, sensitivity's temperature behavior shows only a linear shape. Due to different temperature coefficients of different wafer layers and involved effects, the measured sensitivity reaches a saturation at the high and low end of the temperature sweep (see fig.9). Fitting these trends linear gives unsatisfactory results, as can be seen in simulations with a current model and leads to the necessity of additional second or third order coefficients.

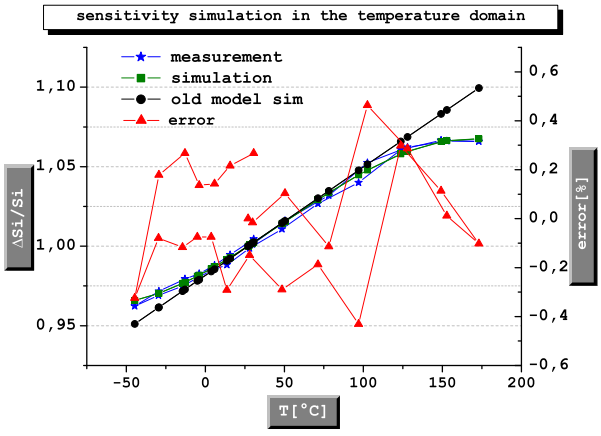

Figure 9: Model verification with a simulation of the temperature coefficients for the Hall device's sensitivity. The reference temperature for the calculations was chosen as $27°C \approx 300°K$.

In conclusion, after simulation of all performed parameter measurements, the results always fit the measurement results with a satisfying accuracy. Final model tests included simulations of common known Hall device circuits. Many of them can be found in Hall sensor IC's (fig.10,11,12).

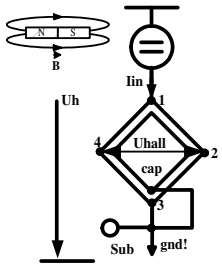

Figure 10: A Hall device in a usually used configuration with a voltage sweep from 0V to 2V. The Hall voltage was generated by a constant magnetic flux.

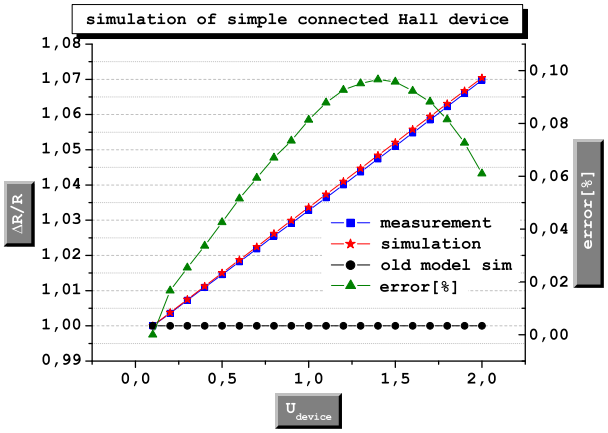

Figure 11: Model verification with a simulation of device's resistivity with a input voltage sweep of $0 - 2V$. This functionality simulation considered all model parameters and parasitics.

Conclusion

A new model for Hall device simulations has been presented including the most significant nonlinear effects. It allows simulations up to an accuracy of better than 99% over temperature and different bias conditions. With the study of the body structure, the main effect causing nonlinearities was found in the voltage dependency of the pn-junction thickness. The value was determined theoretically up to $8\%/V$ in device's resistance and up to $5\%/V$ in its sensitivity, respectively. Experimental investigations confirmed these results. Using a biased conductive plate, additional effect of $\approx 1\%/V$ in resistance and sensitivity has been observed. The role of the temperature dependent charge carrier concentration in the theoretical parameters

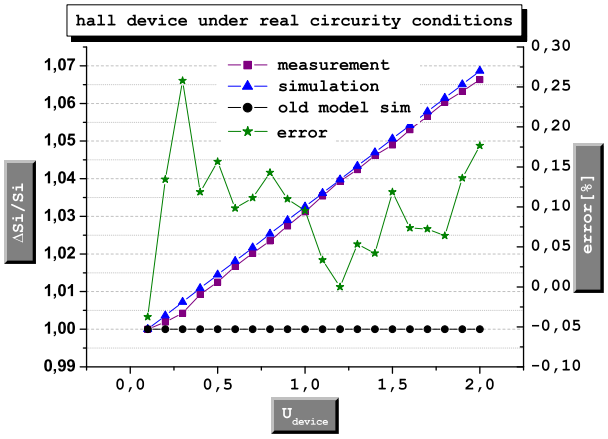

Figure 12: Model verification with a simulation of device's sensitivity with a performed input voltage sweep of $0 - 2V$ and a constant magnetic flux density of $B = 0.1T$. This simulation considered all model parameters and parasitics.

and coefficients, motivated temperature investigations of these. Parasitics are taken into account by attaching their standard spice models onto the new Hall simulation model. The model is implemented in VHDL-AMS and consists in its current version of about 50 behavioral coefficients. Performance tests included simulations equal to parameter measurements and common circuit configurations for Hall devices. As final tests for model correctness and high accuracy, simulations of complete Hall sensor ICs were performed and compared with measurement result. Remaining discrepancies are mostly caused by induced stress during packaging.

Acknowledgments

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