MIXED-SIGNAL BEHAVIORAL SIMULATION OF AN ENVELOPE PREDISTORTION LINEARIZATION SYSTEM FOR RF POWER AMPLIFIERS

Wangmyong Woo, Eungsic Park*, Kongpop U-yen, and J. Stevenson Kenney

School of Electrical and Computer Engineering, Georgia Institute of Technology,
Atlanta, GA 30332-0250, USA
*Danam Communications Inc., Korea
wmwoo@ece.gatech.edu

***Abstract*—**This paper presents a mixed-signal behavioral simulation for an RF power amplifier predistortion system. The predistortion architecture is based on FPGA-based look-up tables that drive RF vector modulators. Behavioral models are extracted from the RF components and simulated in the same file with the digital components. Trade-offs are made between the FPGA design and the RF component designs to optimize the performance of the system.

1. INTRODUCTION

The next generation of wireless components will consist of mixed-signal circuits and subsystems [1]. Simulation of RF and digital signals has been problematic, in that RF components are generally simulated in the frequency domain at circuit level, whereas the digital subsystem is simulated behaviorally in the time domain. Moreover, increasing system complexity, reduced size, and decreasing time-to-market drive the need for full system-level simulation and optimization. [2]. Behavioral modeling of RF components has been proposed as a way to bridge the gap to do full system simulation [3-5].

A power amplifier (PA) is an indispensable component in a communication system and has intrinsically nonlinear characteristics. Moreover, PA distortion degrades with increasing power, while efficiency improves. To reduce the impact of this trade-off in system design, linearization techniques have been proposed [1, 3]. Predistortion (pre-D) is one of the linearization architectures that utilize digital signal processing (DSP) to modify in PA input signal in such a way as to compensate for the nonlinear distortion. This is often done at baseband [6]. Recently, envelope pre-D has come into favor because of the improved bandwidth, and the fact that the baseband I/Q streams are often unavailable to the PA designer [7].

This paper presents a mixed-signal behavioral simulation of an envelope predistortion system. The behavioral technique allows for trade-offs to be made between the digital subsystem and the RF component design so as to optimize the system performance.

2. POWER AMPLIFIER PREDISTORTION LINEARIZATION

Predistortion linearization utilizes in nonlinear mapping function before the PA that is exactly the inverse of the PA distortion characteristic. The combined transfer characteristic of the cascade is thus linear over some operating power range as shown in Fig. 1. This technique reduces the distortion and enables the operating point of a power amplifier to be much higher, improving the efficiency.

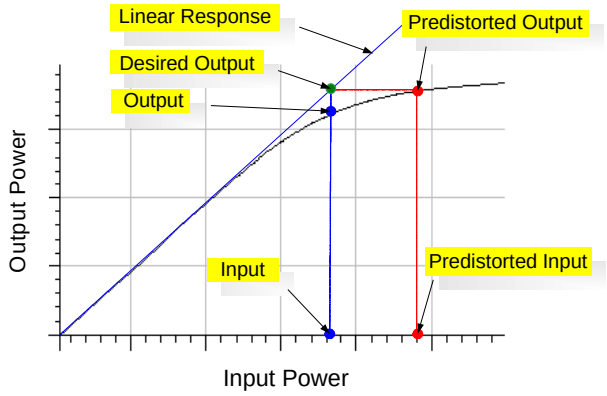


Figure 1. Operation of a Predistortion System.

In the envelope predistortion architecture, a vector modulator (VMOD) is used to vector predistort the RF input signal before the PA. The vector modulation is controlled according to the inverse function of the PA distortion characteristic, for which discrete values are stored and read-out from the look-up table (LUT). The LUT is indexed by the amplitude obtained from an RF envelope detector (EDET) as shown in Fig. 2. The output signal, $s_{out}(t)$, can be derived as

$$\begin{aligned} s_{out}(t) &= G\left(s_{PD}(t)\right) = G\left[F\left(s_{in}(t)\right)\right] \\ &= \mathrm{Re}\left\{g\left[f\left(|s_{in}(t)|\right)\right]\cdot e^{j\left\{\arg\left[s_{in}(t)\right]+\psi\left[|s_{in}(t)|\right]+\theta\left[f\left(|s_{in}(t)|\right)\right]\right\}}\right\} \end{aligned} \quad (1)$$

where $s_{PD}(t)$ is the predistorted signal, $G(\cdot)$ and $F(\cdot)$ are the complex nonlinear transfer function of the PA and predistortion circuit, respectively, $s_{in}(t)$ is the input signal,

$g(\cdot)$ and $\theta(\cdot)$ are the amplitude and phase response function of the PA, and $f(\cdot)$ and $\psi(\cdot)$ are the amplitude and phase response functions of the predistortion circuit.

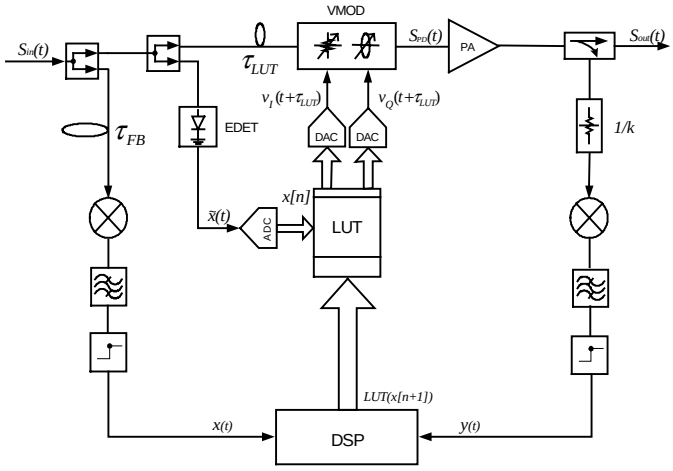


Figure 2. Block diagram of the RF envelope predistortion system

In the LUT adaptation, the envelopes are extracted after the RF signals are downconverted and sampled. They are then processed to identify the nonlinear characteristic of the PA in the digital signal processor (DSP). The results are used for updating the LUT adaptively using the following least mean square (LMS) algorithm:

$$LUT(x[n+1]) = LUT(x[n]) + \mu \cdot e[n] \qquad (2)$$

where μ is a stability factor, and $e[n] = (x[n]-y[n])/x[n]$. The size of the LUT, and the DAC resolution are determined by the extent of the nonlinearity of the PA. *Herein lies the basic trade-off between the RF portion, mixed-signal devices, and the FPGA.*

3. MIXED-SIGNAL SIMULATION MODELS

A mixed-signal behavioral model was developed using Agilent ADS™. The model includes frequency dependent models in time domain simulation. The RF components such as the VMOD and the EDET were modeled by using microstrip lines based on the transmission line theory.

The most common method for the VMOD implementation is to use variable attenuators that operate on quadrature signals to produce the desired amplitude and phase values when summed. It should be noted that the attenuator control characteristics are not linear. However, the errors are automatically compensated in the LUT as it adapts to minimize the overall distortion. The VMOD, shown in Fig. 3, consists of a 90deg hybrid coupler, two variable attenuators, and a Wilkinson combiner.

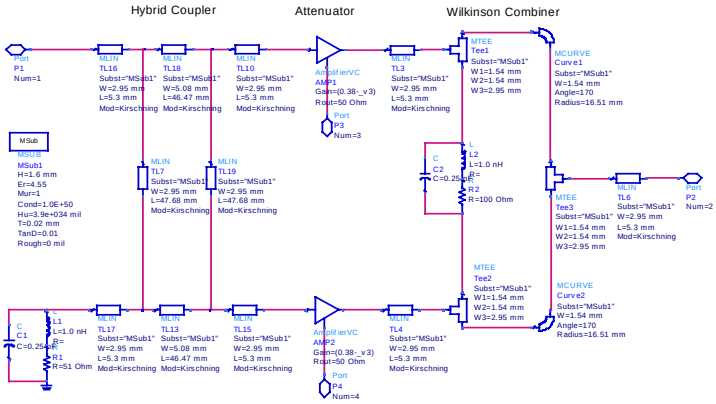


Figure 3. Schematic of the VMOD module.

The RF input is split into I and Q signals by the quadrature hybrid coupler. Each of I and Q signals is attenuated by the modulating signals ($v_I(t)$ and $v_Q(t)$) which come from the LUTs through the digital-to-analog converters (DACs).

Fig. 4 shows the RF envelope detector that is used for the system to monitor the signal amplitude and index the LUT. The balanced configuration in conjunction with the matching networks provides a good voltage standing wave ratio (VSWR) and low reverse intermodulation distortion (IMD). The matching network provides the minimum return loss for a signal detector. A 90deg hybrid coupler is employed to minimize the reflected odd harmonics. The voltage doubling detector gives twice the voltage level as high as a single diode detector.

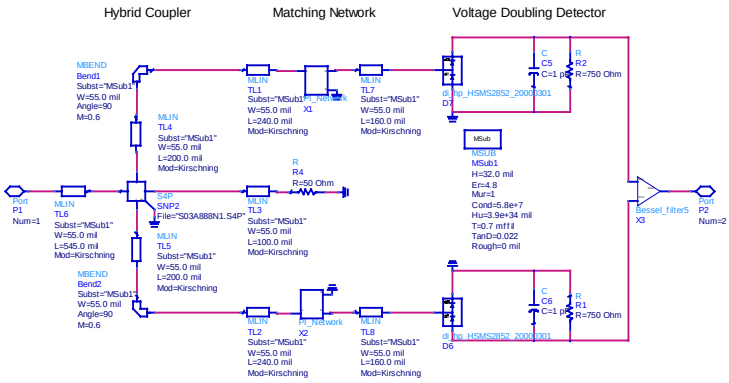


Figure 4. Schematic of the EDET module.

The lowpass filter (LPF) designed using the normalized transfer function, $H(s)$, removes aliasing signals and unwanted harmonic frequencies, providing a flat group delay in a wide range.

$$H(s) = \frac{1}{0.591 \cdot s^3 + 1.764 \cdot s^2 + 2.318 \cdot s + 1} \qquad (3)$$

After RF signals are converted into digital signals, they are used by the digital components such as arithmetic components and random access memory (RAM) that is employed in a LUT. The LUT, shown in Fig 6, can be modeled by a hardware description language (HDL). Thereby, it enables a field programmable gate array (FPGA) configuration design to be simulated and confirmed in its feasibility. The predistortion system adopting a LUT is not sensitive to loop delay since it is not coupled to a low-order parametric model such as a polynomial. There are different LUT spacing methods for the LUT spacing strategy. The LUT used in this simulation has entries equally spaced in the input signal amplitude without interpolation. As mentioned in [8], the equispacing by amplitude gives many advantages such as operation simplicity, good performance, and independency of amplifiers, modulation format, etc.

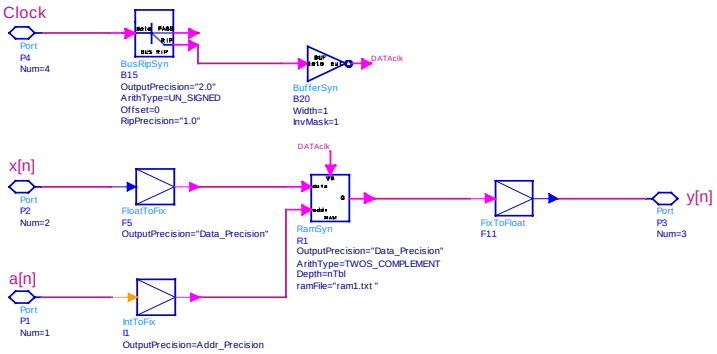
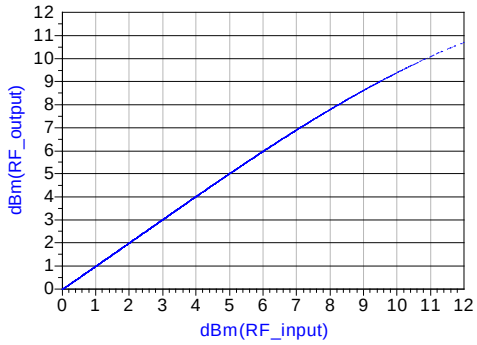


Figure 5. Schematic of the LUT module.

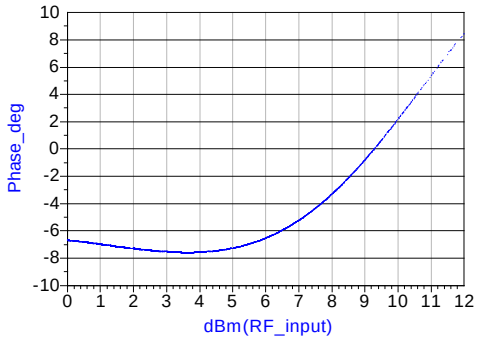
In this simulation, the power amplifier under test (AUT) was the Sirenza 0.5W HFET PA (SHF-0189). A behavioral model was extracted at 850 MHz by fitting the AM-AM and AM-PM distortion functions to 9th order polynomials. In the simulation, the output power at 1dB gain compression point (P_{1dB}) was 27dBm, as shown in Fig. 6.

4. Simulation Results and Analysis

The IS-97 9-channel CDMA signal with 11dB peak-to-average power ratio (PAPR) was used as the input signal. In order to satisfy the specification defined in [9], spurious emission must be at least 45dB below the channel power for offset frequencies greater than 750 kHz. In this simulation, only the backoff without linearization cannot satisfy the requirement as shown in Fig. 7. It can be achieved with pre-D and 8dB input power backoff (IBO). The amount of the distortion created depends upon the amplitude distribution of the signal modulation as well as the linearity of the PA. The relation between the signal backoff and the PA characteristic affects the pre-D performance in the adjacent channel power ratio (ACPR) improvement. The input power level should be selected so that the high linearity and efficiency can be achieved simultaneously.



(a) Amplitude



(b) Phase

Figure 6. Sirenza 0.5W HFET power amplifier characteristics.

Signals are converted between analog and digital domains using analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). When a signal moves from a domain to the other, it causes a quantization error and degrades the system performance.

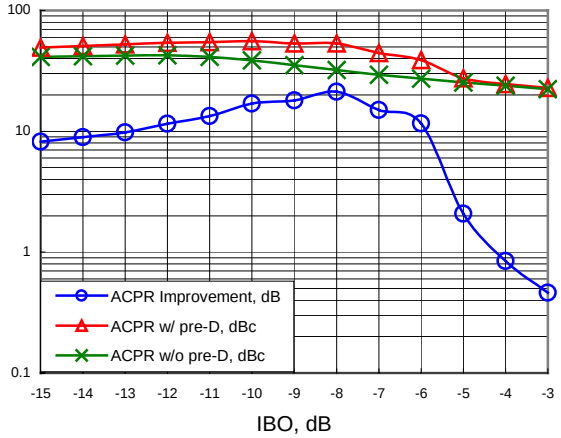


Figure 7. ACPR vs. IBO after pre-D.

According to Fig. 8, the ADC for DSP requires at least 12 bits to reduce the errors, the ADC for LUT 8 bits, and the DACs for VMOD more than 10 bits. Since the ADC for DSP is on the iteration loop to extract the PA nonlinear characteristics, its resolution should be as high as possible. On the other hand, the required resolution of the ADC for LUT should be considered in that the hitting rate of a LUT bin depends on the resolution and affects the adaptation speed. The DAC for VMOD is less sensitive than the ADCs for the performance

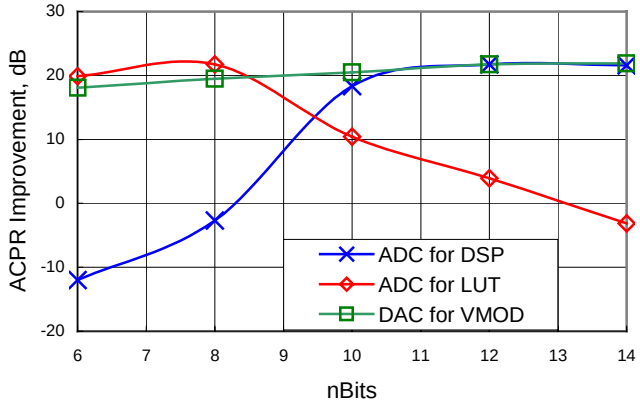


Figure 8. Optimum resolutions for ADC and DAC.

Fig. 9 shows the simulated performance of the predistortion system and the sampling frequency requirement for the ADC/DAC. Spectrum (a) and (c) indicates that the sampling frequency must be at least 4 times the input signal bandwidth in order to deal with 3rd and 5th order spectral regrowthes and get the linearization. As shown in (d), a 20dB improvement in ACPR was obtained at 885 kHz offset. This was achieved at 8dB IBO using an LUT size of 256 words, and a 12 bit DAC, which covered an input power range of 8 dB.

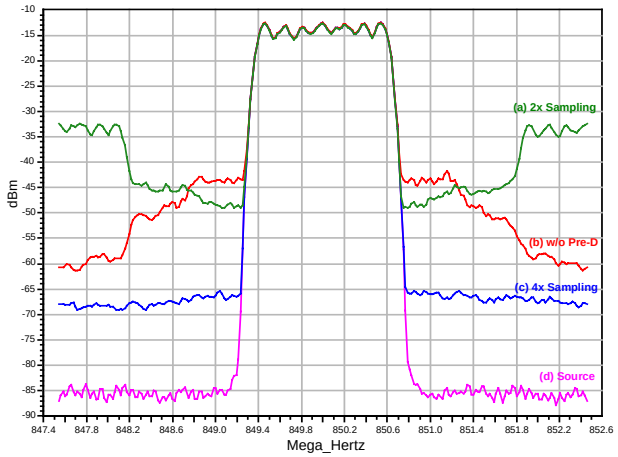


Figure 9. Spectrum results (at 8dB IBO).

CONCLUSIONS

A LUT-based, RF envelope predistortion architecture for power amplifier linearization was simulated and optimized using Agilent ADS™. The mixed-signal behavioral technique allowed real-time optimization of both RF, digital, and data conversion components. Once optimized, the resulting system showed a simulated improvement of 20 dB in the adjacent channel power ratio over the basic RF PA performance.

ACKNOWLEDGEMENT

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