# Mixed Compact and Behavior Modeling Using AHDL Verilog-A

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## Abstract

The way from the compact model development to implementation into a commercial circuit simulator is often time consuming. Moreover, it is not always straightforward how to implement behavior models in SPICE-like simulators. In this paper, a capability of the analog hardware description language (AHDL) Verilog-A to handle state-of-the-art compact bipolar transistor modeling mixed with behavioral substrate coupling modeling has been demonstrated.

## Introduction

The Verilog-A is a high-level language developed to describe the structure and behavior of analog systems and their components (1). It is an extension to the IEEE 1364 Verilog HDL specification for digital design. The analog systems are described in Verilog-A in a modular way using hierarchy and different levels of modeling complexity. The motivation is to invest in a new higher level of abstraction in analog design and its combination with the digital one.

The basic programming unit for the structural and behavioral description of the analog systems in Verilog-A is a *module*. The analog system structure is defined through the module's input and output signals and their connections. On the other hand, the sequence of mathematical equations is employed at the core of the module to describe its behavior. It is also possible to control the equations by a set of parameters that can be passed to the module at the moment of its instantiation into the analog system. With these features, Verilog-A language represents an excellent environment for rapid development and verification of compact and behavioral modeling ideas in the commercial circuit simulators.

In order to practically verify capabilities of Verilog-A to serve as a framework for mixed compact and behavioral model developments we have implemented the bipolar transistor compact model Mextram Level 504 directly following the model description in the Philips documentation (2). Since the present Mextram release does not include substrate model, it is added here in the form of a Verilog-A behavioral model based on the Laplace transfer function.

## Compact Model Implementation and Testing

The Verilog-A Mextram 504 implementation has been tested using the Cadence circuit simulator Spectre equipped with the Verilog-A interface. As it was expected, the Verilog-A based simulations appeared to be quite inferior in CPU time compared to the equivalent simulations based on the hard-coded models. The reason is the fact that the present Verilog-A interfaces (including one in Spectre) are only interpreters of the Verilog-A language. It is likely that this deficiency will disappear in the future with the introduction of Verilog-A translators and/or compilers (3).

Perhaps, the most important question related to the Verilog-A implementation of Mextram 504 is the achieved accuracy of the simulated electrical characteristics. To this end, the hard-coded implementation of Mextram 504 in Agilent circuit simulator ADS has been used as a reference for comparison. As a measure of the discrepancy between two model implementations, we have considered the relative error of simulated electrical characteristics. Since only the computational accuracy has been analyzed, the comparison has been based on the standard setups for Mextram model parameters extraction and the default values of the model parameters (4). Fig. 1-6 show the comparisons of various electrical characteristics obtained by Verilog-A Mextram 504 (dot lines) implementation, hard-coded Mextram 504 (solid lines) implementation and the corresponding relative error.

It has been observed that in most cases the relative error of electrical characteristics used in our comparisons is quite low with the worst case of $\approx 1\%$. Only the first point in both forward and reverse Gummel characteristics (Figs. 3 and 4) will exceed 1% due to convergent problems. The source of < 1% discrepancies could be the numerical accuracy of the variables and functions within the Verilog-A interpreter (in comparison to C double precision variables and functions), and the order in which the expressions are executed (especially in the symbolic evaluation of. Jacobian derivatives).
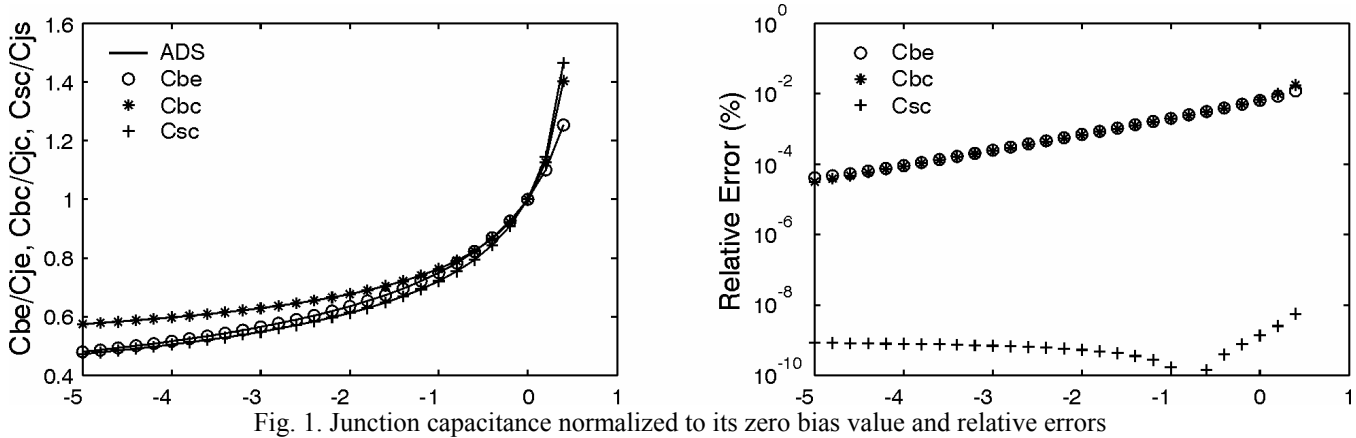
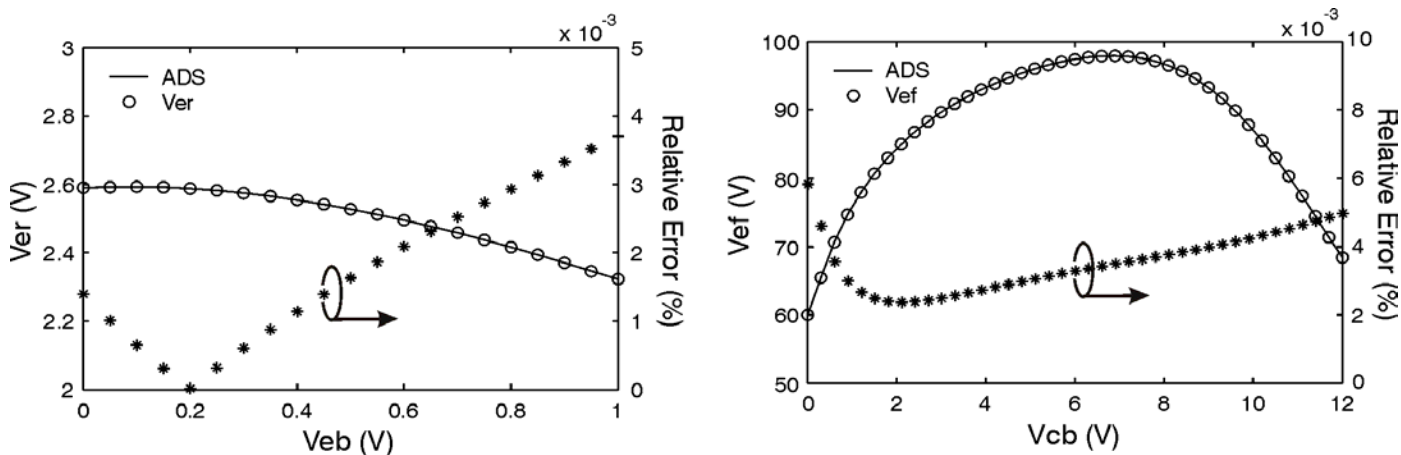Fig. 1. Junction capacitance normalized to its zero bias value and relative errors



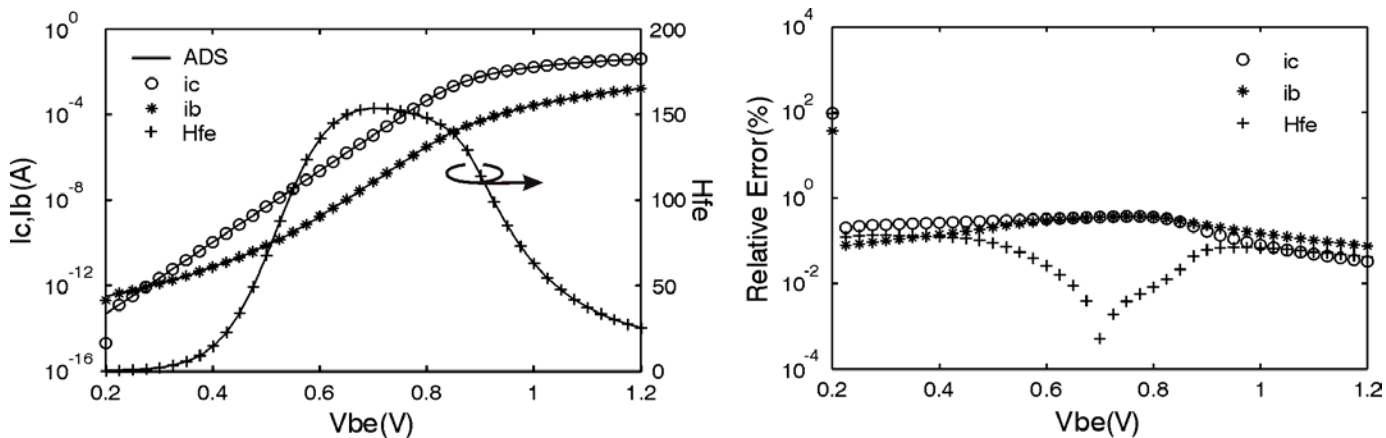Fig. 2. Reverse, forward Early voltage and relative errors



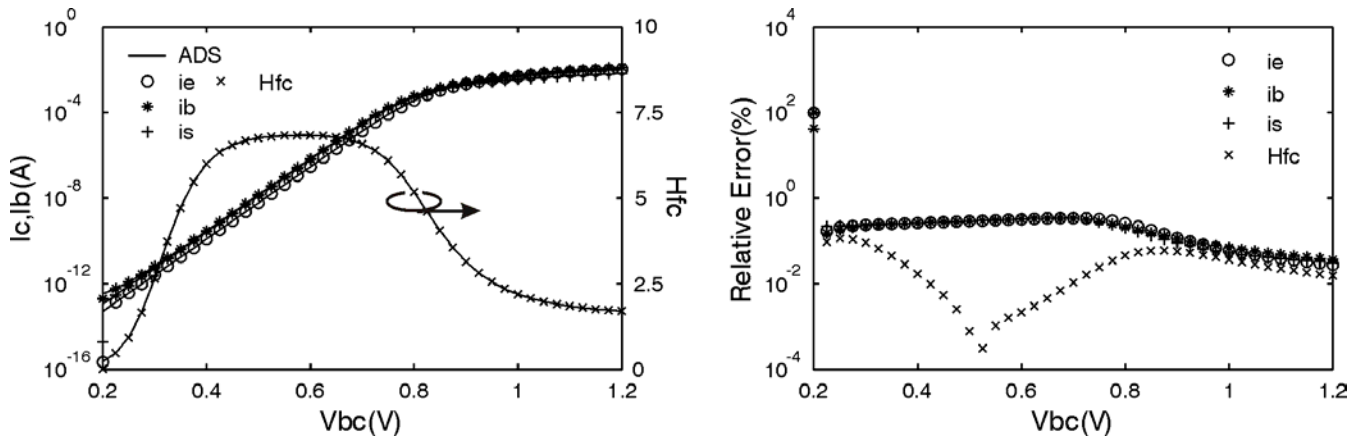Fig. 3. Forward Gummel characteristics and relative errors

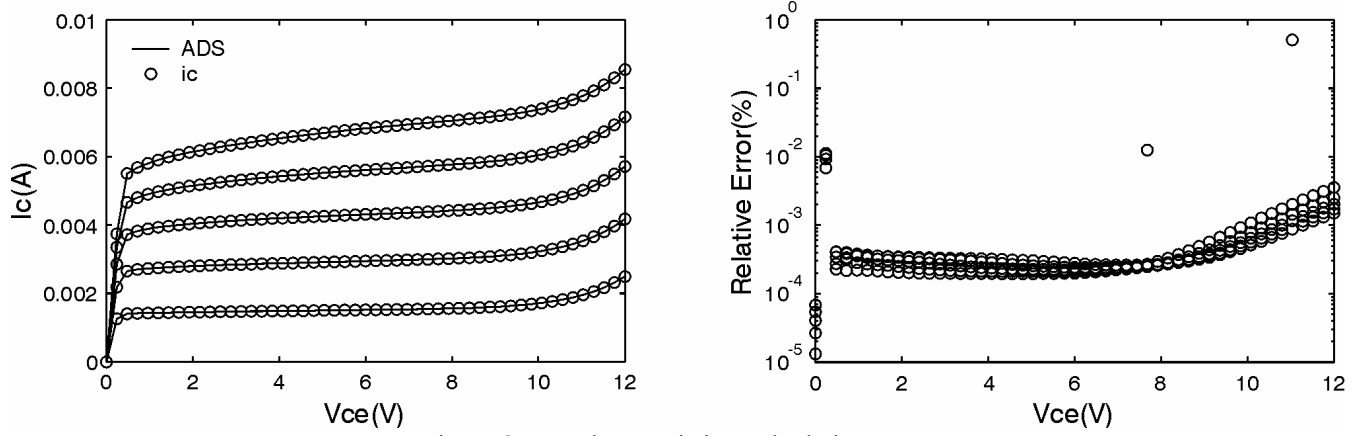Fig. 4. Reverse Gummel characteristics and relative errors
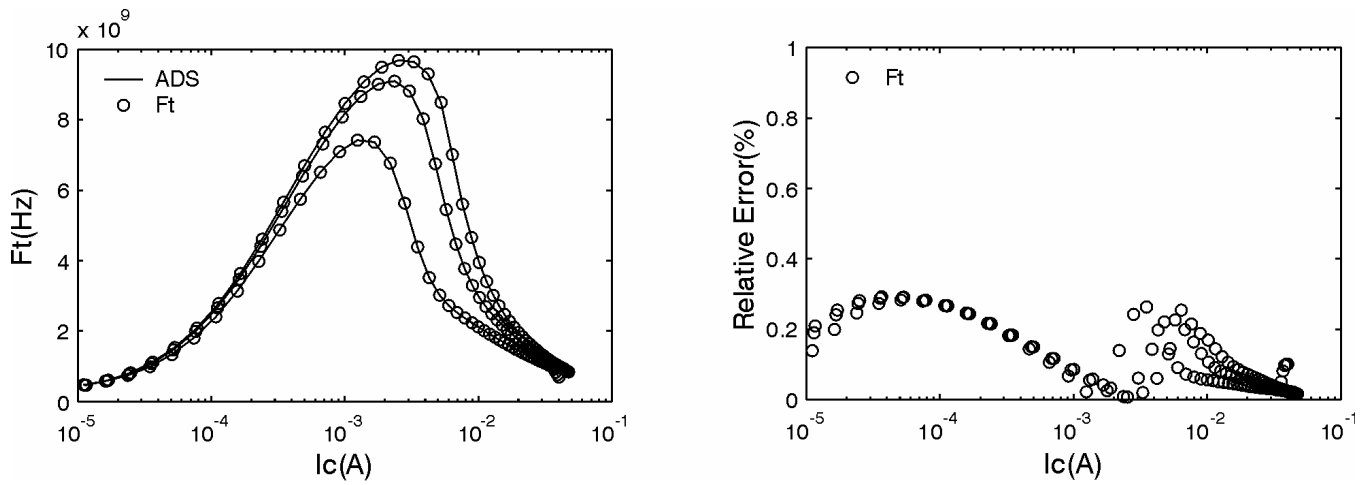
Fig. 5. Output characteristics and relative errors

Fig. 6. Ft vs. Ic and relative errors

## Behavior modeling of substrate effect

For most of the bipolar transistor compact models, like Mextram, substrate effect is not included in the model, or like Hicum (5), it uses a simple R-C network for the substrate effect. In reality, bipolar transistors are made on top of the silicon substrate. When a bipolar device operates at radio frequency range, the lossy Si substrate becomes a distributed substrate network connected to intrinsic device as shown in fig.7.
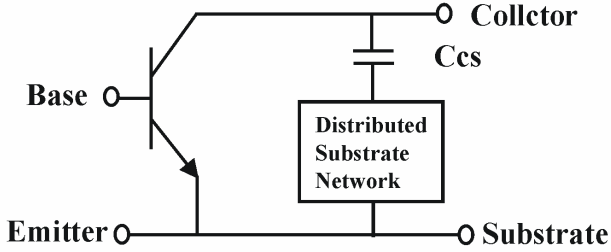


Fig. 7. Transistor with embed distributed substrate network on a Si wafer

The distributed substrate network will changed if the substrate contact of the bipolar device is changed. That is the reason why Mextram model doesn't take substrate as a part of the model since the substrate contact may be different from modeling devices to the final circuit design. But for some bipolar processes, transistor's substrate contact is well defined as a p-cell to reduce designer's burden in determining the complicated substrate network. Then, accurate modeling the substrate network will be greatly helpful for high frequency circuit design.

In order to account for substrate effect on the single transistor characteristics at high frequency region, we can use compact model for transistor itself and a behavior model for the distributed substrate network. Based on the off state S-parameters measurement (6), we can get substrate impedance as a function of frequency from its off-state equivalent circuit (fig. 8) and measured $Z_{22}$
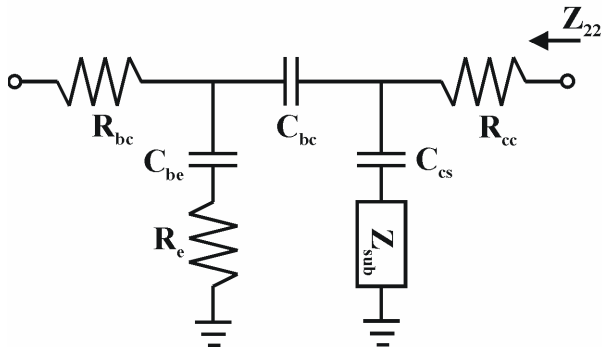


Fig. 8. Off state equivalent circuit of a bipolar transistor

model
The measured substrate impedance $Z_{sub}$ Will be:

$$\mathbf{Z}_{sub}(s) = \frac{(Z_{22} - R_{cc})(1 + S \cdot C_{bc} \cdot Z_1)}{1 + S \cdot C_{bc} \cdot (Z_1 - Z_{22} + R_{cc})} - \frac{1}{S \cdot C_{cs}} \quad (1)$$

where $\mathbf{Z}_1(s) = R_e + \frac{1}{S \cdot C_{be}}$

For the purpose of the behavioral modeling, a distributed substrate network is considered as a 1-port functional block with associated potential and current. In the Laplace domain the relationship between the input excitation and the corresponding response has been described by the rational complex function

$$Z(s) = \frac{\sum_{k=1}^{n} a_{n-k} s^{n-k}}{s^n + \sum_{k=1}^{n} b_{n-k} s^{n-k}} \quad (2)$$

where "Z" and "a" are scalar elements, respectively. For a given set of frequency response data, $2n$ model parameters for the behavioral model $((a_i, b_i), i = 0, n-1)$ are obtained by solving the linear least square problem.

$$\sum_{k=1}^{n} (a_{n-k} - Z(j\omega_l) \cdot b_{n-k}) \cdot (j\omega_l)^{n-k} = Z(j\omega_l) \cdot (j\omega_l)^n$$
$$l = 1, ..., N_\omega \quad (3)$$

where $N_\omega$ is the number of frequency samples.

Fig.9. shows the extracted substrate impedance of a SiGe HBT (7) as a function of frequency. In this particular case, rational complex function with $n = 6$ can fit measured data very well. In Verilog-A, we can easily implement this rational complex function with the *Laplace transform* analog operator "laplace_nd" (1).
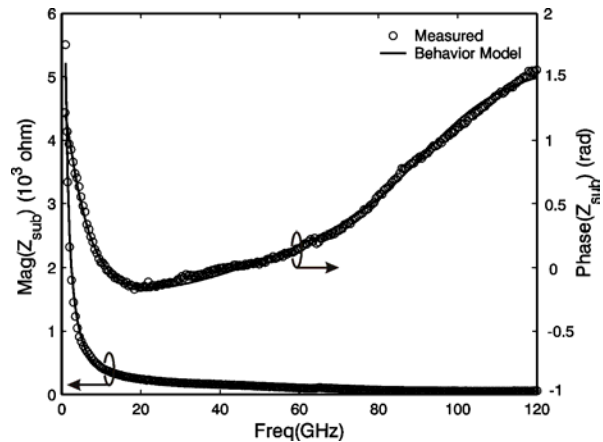
Fig. 9. Magnitude and phase of substrate impedance vs. frequency

Since $Y_{22}$ is the most influential parameters of the substrate effect, fig.10 shows measured and simulated $Y_{22}$, which is biased at around peak Ft of the same SiGe HBT.
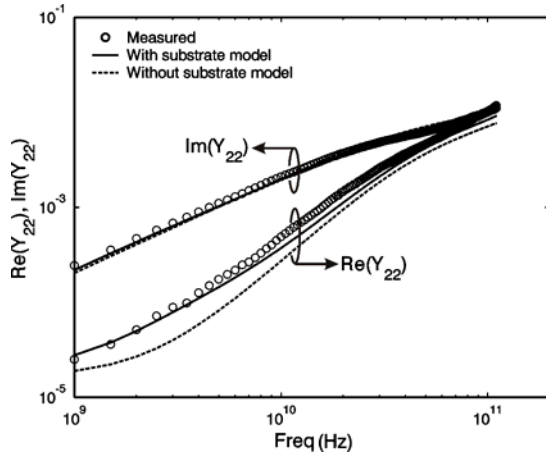


Fig. 10. Measured and simulated $Y_{22}$ vs. frequency

Also in fig. 10, we can find with the behavior model of substrate adding to the intrinsic SiGe bipolar model, which has been extracted based on the standard Mextram parameters extraction procedures, simulated $Y_{22}$ fits measured $Y_{22}$ better than without it. It is because of Verilog-A language, we can model such a complex distributed network in a very efficient way.

## Discussion
One of the first observations and potential benefits of using Verilog-A in compact model development is that Verilog-A facilitates quite "compact" representation of the compact models. The size of the Verilog-A Mextram 504 code is around 800 lines. It is mainly due to the fact that there is no need to program: (a) interfaces to the simulator (concern of the particular circuit simulator with Verilog-A interface) and (b) derivatives of electrical quantities (evaluated using symbolic derivation of the equation describing electrical signals). However, the writer of the Verilog-A code is still fully responsible for the numerical stability of the governing model equations (smooth transitions, range of functions, etc.). A good programming practice and experiences from the C-code implementations could be very useful in achieving effective Verilog-A code.

## Conclusion
The general conclusion could be that Verilog-A indeed represented an effective environment for the fast evaluation and exchange of new compact modeling ideas. It will also be employed for implementation adds on modeling features like substrate coupling and other network, like improved thermal coupling network, etc.

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