# Behavioral modeling of continuous time $\Delta\Sigma$ modulators

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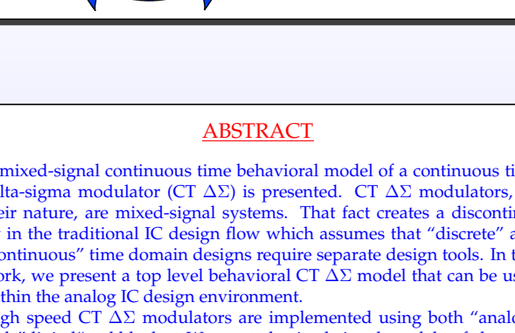
ABSTRACT

A mixed-signal continuous time behavioral model of a continuous time delta-sigma modulator (CT $\Delta\Sigma$) is presented. CT $\Delta\Sigma$ modulators, by their nature, are mixed-signal systems. That fact creates a discontinuity in the traditional IC design flow which assumes that "discrete" and "continuous" time domain designs require separate design tools. In this work, we present a top level behavioral CT $\Delta\Sigma$ model that can be used within the analog IC design environment.
High speed CT $\Delta\Sigma$ modulators are implemented using both "analog" and "digital" subblocks. We created mixed-signal models of the subblocks in order to efficiently perform simulations that accurately reflect circuit behavior in the continuous time domain. The models were built out of primitives available in $SPICE$ and $Verilog-A^{TM}$.
We present a first order CT low-pass $\Delta\Sigma$ (CTLP $\Delta\Sigma$) as well as a fourth order CT band-pass $\Delta\Sigma$ (CTBP $\Delta\Sigma$) to demonstrate the modeling technique and simulation methodology. We explored the influence of the loop delay and clock jitter on the CT $\Delta\Sigma$ performance.

## 1 Introduction

The traditional approach to simulate the behavior of a $\Delta\Sigma$ modulator is by creating z-domain models and using a discrete time (DT) simulator, such as MATLAB$^{TM}$. This approach is logical since $\Delta\Sigma$ modulators are sampled systems by nature. As a result, most of the $\Delta\Sigma$ implementation were done by using techniques such as switched capacitor and switched current. The increased interest in the high speed continuous time $\Delta\Sigma$ modulators created a problem with the traditional IC design flow, which is not well suited for this application. The principle reason is that the discrete domain simulators were not well connected to the back end IC design tools, while at the same time continuous time simulators were lacking top level behavioral modeling capability. However, mixed-signal simulators are now becoming more practical and are incorporated in the analog IC design environment. Previously published works on $\Delta\Sigma$ modeling were based either on SIMULINK® models [1], custom made C programs, or $Verilog-A^{TM}$ [2].

### 1.1 General $\Delta\Sigma$ architecture




### 1.2 Problem

The presence of the high speed clock and quantizer makes the simulation time very long if CT simulators are used, while discrete time simulators use high level models which do not offer enough insight into the circuit behavior.
A CT $\Delta\Sigma$ modulator is an example of a mixed-signal circuit that creates discontinuities in the IC design flow. It requires a smooth connection between the behavioral models developed in discrete time and the physical realization of the IC circuits. Bridging these two worlds is one of the motivations behind this work.

## 2 Basic building blocks

In this section, we present behavioral models of the basic functional blocks required to create a complete CT $\Delta\Sigma$ modulator. Our models are developed in $SPICE$ and $Verilog-A^{TM}$ [3], while the simulator used was $Spectre^{TM}$ within $Analog-Artist^{TM}$.

Our set of basic blocks consist of the following DT/CT behavioral modules: integrator, general s-transfer function, comparator, D flip-flop (DFF), DAC with non-return to zero (NRZ), return to zero (RZ) and hold-return to zero (HZ) pulses, summing block, ideal gain, and clock with controlled jitter. All of the blocks have controlled delay included.

### 2.1 Integrator

We used:

```
V(vout) <+ laplace_nd( V(vin) [ n0 ], [ d0, d1 ])
```

to create the $k/s$ function, where `n0=k`, `d0=0`, and `d1=1`. The integrator is sufficient to create loop filters for a CTLP $\Delta\Sigma$ modulator.

A general s-transfer function is needed to create a higher order filter $\Delta\Sigma$ loop function. The, $Verilog-A^{TM}$ `laplace_nd` function was used to create the transfer function $H(s) = N(s)/D(s)$. Where `n0, n1, .. nN` are the $N(s)$ polynomial coefficients and `d0, d1, .. dD`, $(N+1 \leq D)$ for the $D(s)$ polynomial.

### 2.2 D flip-flop

We used the following code to implement the D flip-flop, which is a basic delay unit $z^{-1}$:

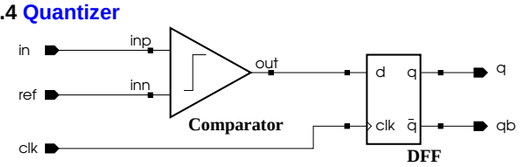
```
@(cross(V(CLK)-Vth, +1)) x=(V(d) > Vth);
V(q) <+ transition(voutHigh*x +
          voutLow*!x, delay, transitTime);
V(qbar) <+ transition(voutHigh*!x +
          voutLow*x, delay, transitTime);
```

### 2.3 AND gate

The AND digital gates, were created as:

```
out = (logic1 && logic2) ?  vlogicHigh :  vlogicLow;
V(vout) <+ transition(out, delay, trise, tfall);
```

### 2.4 Quantizer




The code that implements the comparator function is:

```
V(out) <+ 0.5*(outHigh-outLow)
          * tanh(slope*(V(in, ref)
          - inOffset))
          + 0.5*(outHigh + outLow);
```

One of the problems with using $SPICE$ to model a comparator is that the *min-max* range used in the $VCVS$ function is not exported by the $Analog-Artist^{TM}$ netlister. The small syntax differences that are not supported by the $Analog-Artist^{TM}$ netlister are important factors that have to be taken into consideration when the goal is to make a versatile model that works both within the $Analog-Artist^{TM}$ and as a stand-alone model.

### 2.5 Summing block

```
V(out) <+ absdelay(V(in1)+V(in2),delay);
```

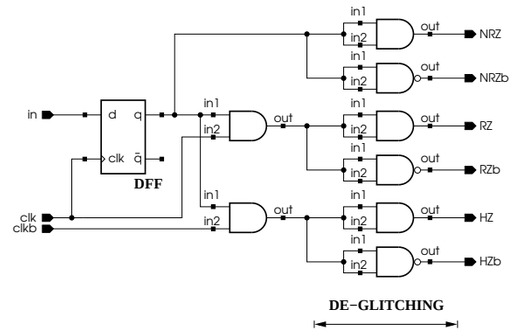
### 2.6 Ideal Gain

```
V(out) <+ absdelay(V(in)*k,delay);
```

### 2.7 Clock modules

The most convenient way to implement an ideal clock that has no jitter is by using the `vpulse` function from $SPICE$.
The main problem with modeling clock jitter in the time domain is in not knowing the jitter distribution before starting the simulation. Mean value and variance are defined over the *length of the simulation*.
We used `randn` (MATLAB$^{TM}$) function to generate a vector of random numbers with normal distribution and $var = 1$ over a given number of clock periods.

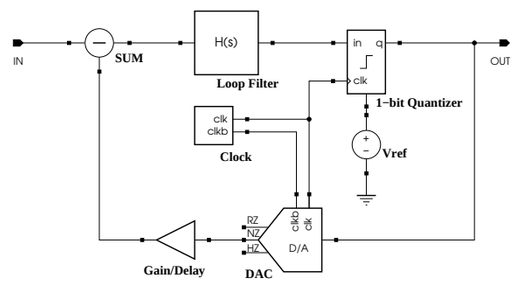
### 2.8 DAC



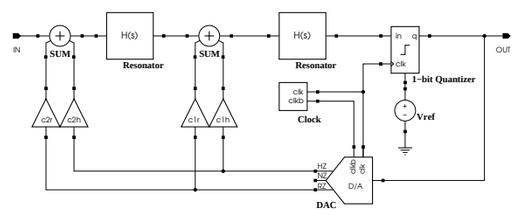

Finite rising and falling times of the pulse edges cause glitches in switching logic. These glitches are one source of the "rising the noise floor". The usual practice in CT design is to add "de-glitching" buffers at the interface of DT to CT domains.

## 3 $\Delta\Sigma$ architectures

### 3.1 CTLP and CTBP general architecture




### 3.2 CTBP double loop architecture [6]

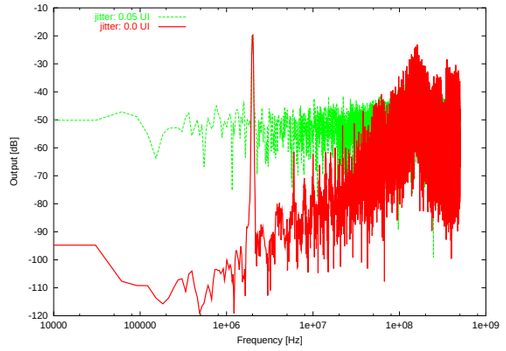



## 4 Simulation performance

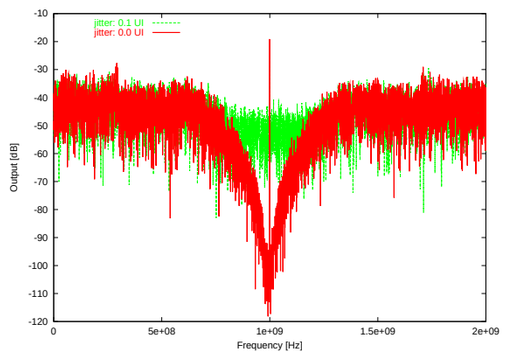
Our models were developed using elements from 'analogLib' and 'ahdlLib' libraries available through $Analog-Artist^{TM}$ environment. Efficient use of the mixed - signal environment and models, combined with SUN Blade1000 machine running SunOS 5.8, resulted in simulations that were typically taking less then 2min per run.

## 5 Simulation results

### 5.1 SDLP with and without jitter




### 5.2 SDBP with and without jitter




## 6 Conclusions

A mixed-signal behavioral model for a CT $\Delta\Sigma$ modulator circuit has been presented. It has been shown that by using mixed-signal approach for behavioral modeling one can achieve high simulation speed and produce meaningful results by staying within one design environment throughout the design process. A mixture of $Verilog-A^{TM}$ and $SPICE$ models makes possible rapid behavioral level simulations within the $Analog-Artist^{TM}$ environment used by analog IC designers.

## References

[1] S. Brigati et al., "**Modeling sigma-delta modulator non-idealities in SIMULINK©**," in Proceedings of the IEEE International Symposium on Circuits and Systems 1999, ISCAS '99, May 1999, pp. 384–387.

[2] M. Vogels, B. D. Smedt, and G. Gielen, "**Modeling and simulation of a Sigma-Delta digital to analog converter using VHDL-AMS**," in Proceedings 2000 IEEE/ACM International Workshop on Behavioral Modeling and Simulation, BMAS 2000, 2000, pp. 5–9.

[3] D. Fitzpatrick and I. Miller, **Analog Behavioral Modeling with the Verilog-A Language**. Kluwer Academic Publishers, 1998, no. 0-7923-8044-4.

[4] J. A. Connelly and P. Choi, **Macromodeling with SPICE**. Prentice Hall, 1992, no. 0-13-544941-3.

[5] O. Shoaei and W. M. Snelgrove, "**Design and Implementation of a Tunable 40MHz-70MHz Gm-C Bandpass $\Delta\Sigma$ Modulator**," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 7, pp. 521–530, July 1997.

[6] O. Shoaei, "**Continuous-time delta-sigma A/D converters for high speed applications**," Ph.D. dissertation, Carleton University, Ottawa, Canada, 1995.

[7] J. A. Cherry and W. M. Snelgrove, **Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion**. Kluwer Academic Publishers, 2000, no. 0-7923-8625-6.