Mixed Compact and Behavior Modeling Using AHDL Verilog-A

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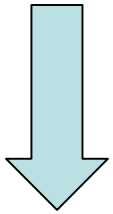
Outline

- Introduction
- Compact Model Implementation and Testing
- Behavior modeling of substrate effect
- Discussion
- Conclusion

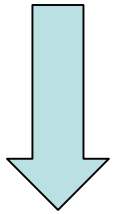
Model

An analogy, representation or description of a certain system (phenomena, process). The models are necessary to perform ***analysis*** and/or ***simulation*** of the system.



Analysis

Getting insight into some system components provided that the effects one wants to extract are built into the model.



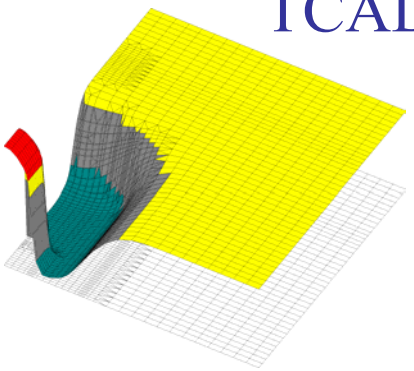
Simulation

Imitative representation of the system functioning in order to examine a problem not subject to physical experimentation (realization)

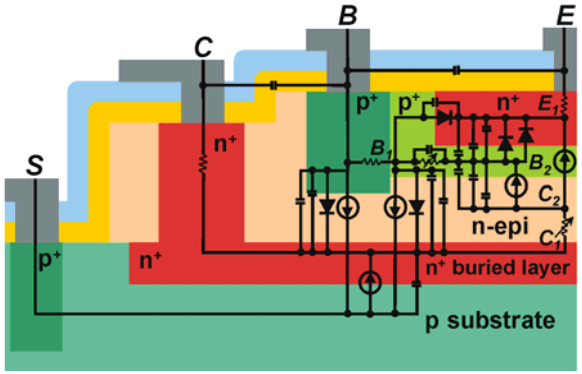
Semiconductor device modeling

Physical modeling

TCAD

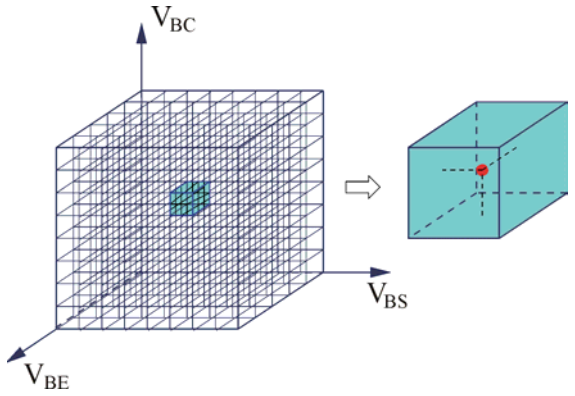


Compact models

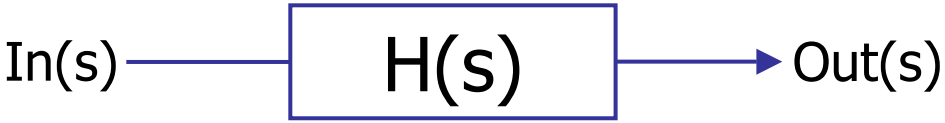


Behavioral modeling

Look-up tables



Transfer Function



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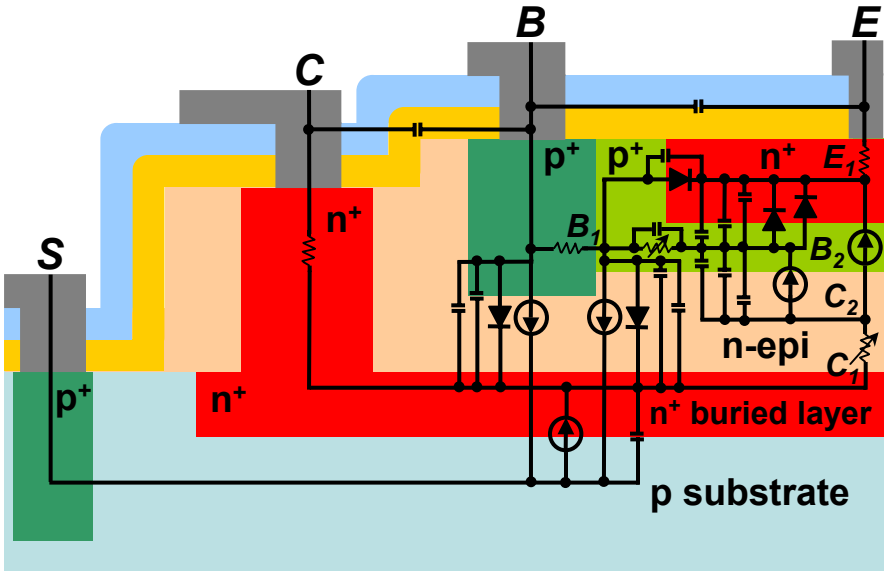
Verilog-A language

- The Verilog-A is a high-level language developed to describe the structure and behavior of analog systems and their components
- It is an extension to the IEEE 1364 Verilog HDL specification for digital design.
- The analog systems are described in Verilog-A in a modular way using hierarchy and different levels of modeling complexity.
- The motivation is to invest in a new higher level of abstraction in analog design and its combination with the digital one

Compact Model Implementation




```
module mextram (c, b, e, s, dt);

// External ports
inout e, b, c, s, dt;
electrical e, b, c, s;
electrical dt;

// Internal nodes
electrical e1, b1, b2, c1, c2;

// Model parameters
parameter real    TREF  = 25.0 from [273.15:inf);
parameter integer EXAVL = 0    from [0:1];

analog begin
// Add branch equations here based on Mextram
504 model report
end

// Add branch current contributions
   I(c2, e1) <+ TYPE * In;
   I(b2, e1) <+ TYPE * (Ib1 + Ib2);
```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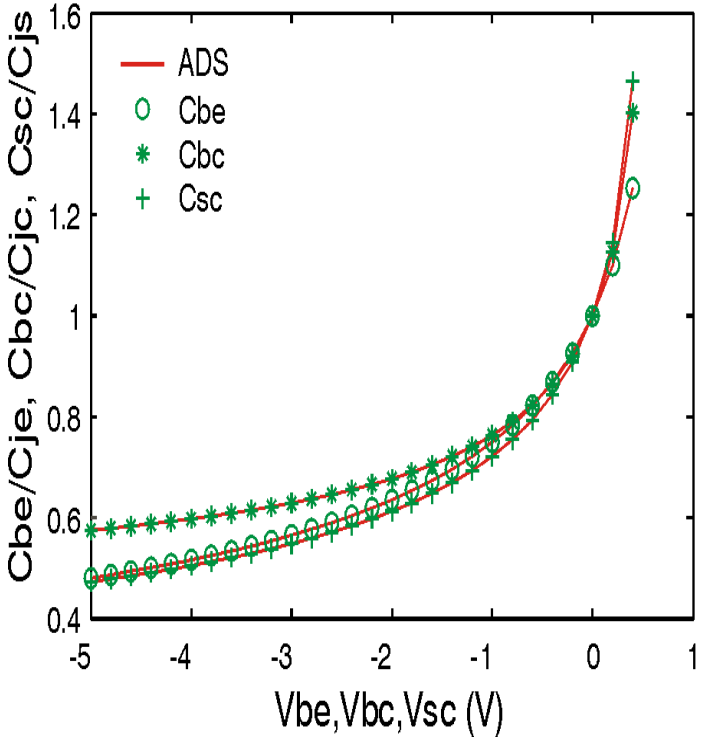
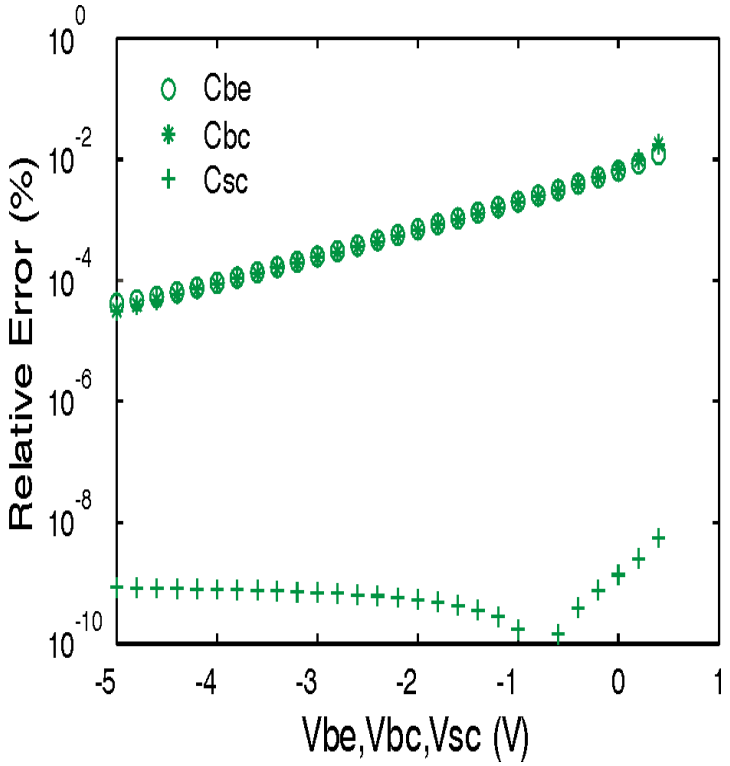
Testing

- Using the Cadence circuit simulator Spectre equipped with the Verilog-A interface
- Using hard-coded implementation of Mextram 504 in Agilent circuit simulator ADS as a reference
- The comparison is based on the standard setups for Mextram model parameters extraction and the default values of the model parameters in the Mextram parameters extraction report

Junction capacitance and relative errors





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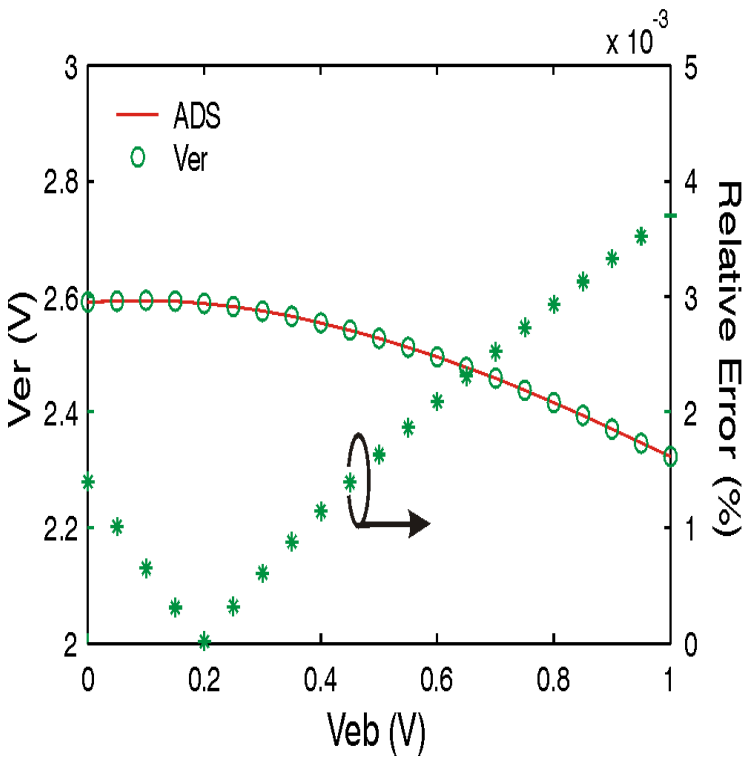
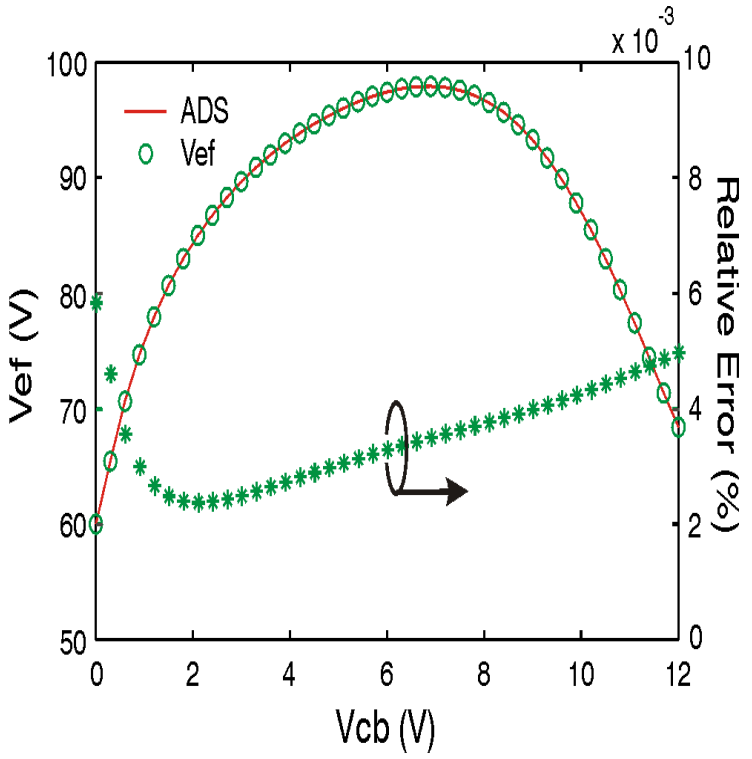
Reverse, forward Early voltage and relative errors





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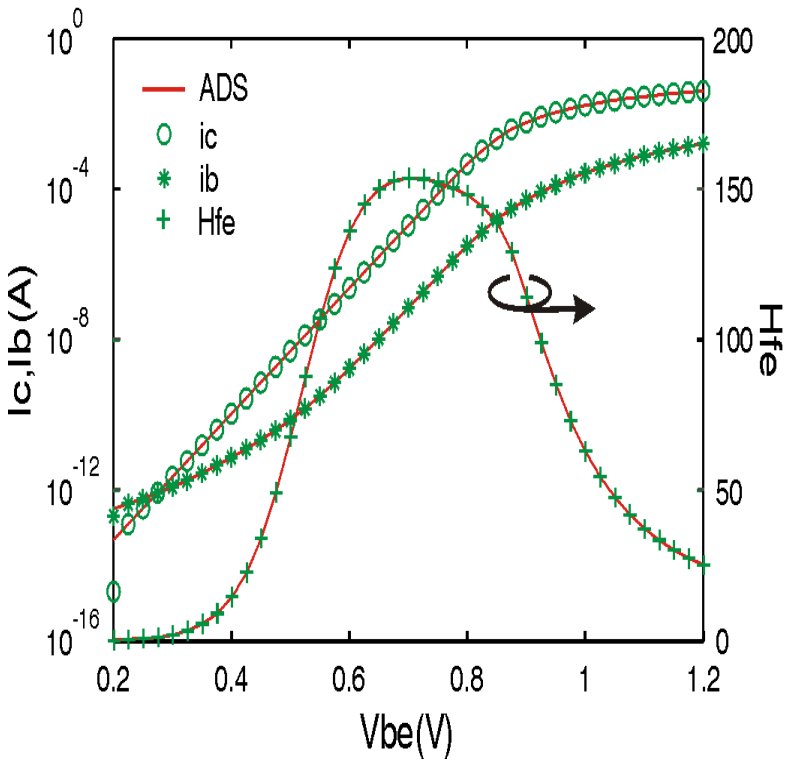
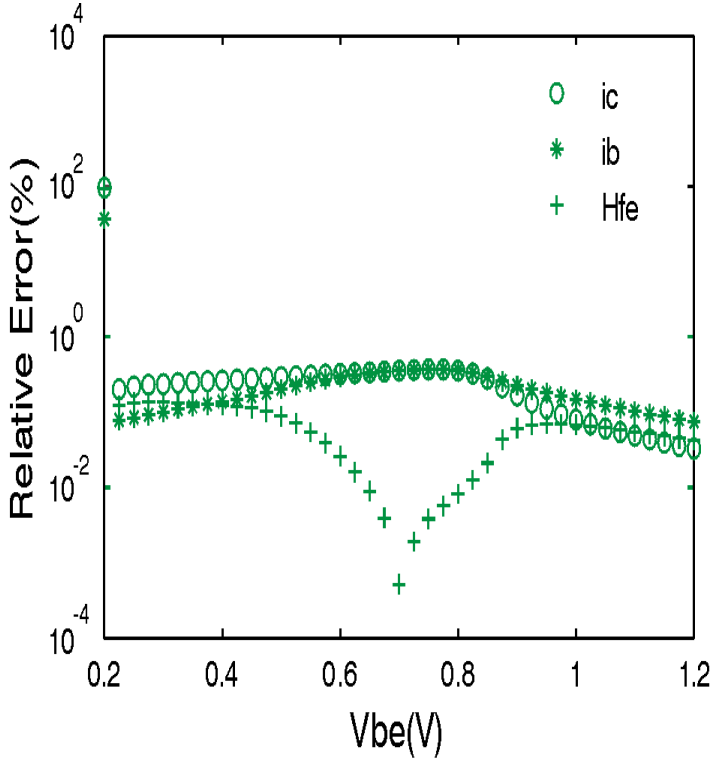
Forward Gummel characteristics and relative errors





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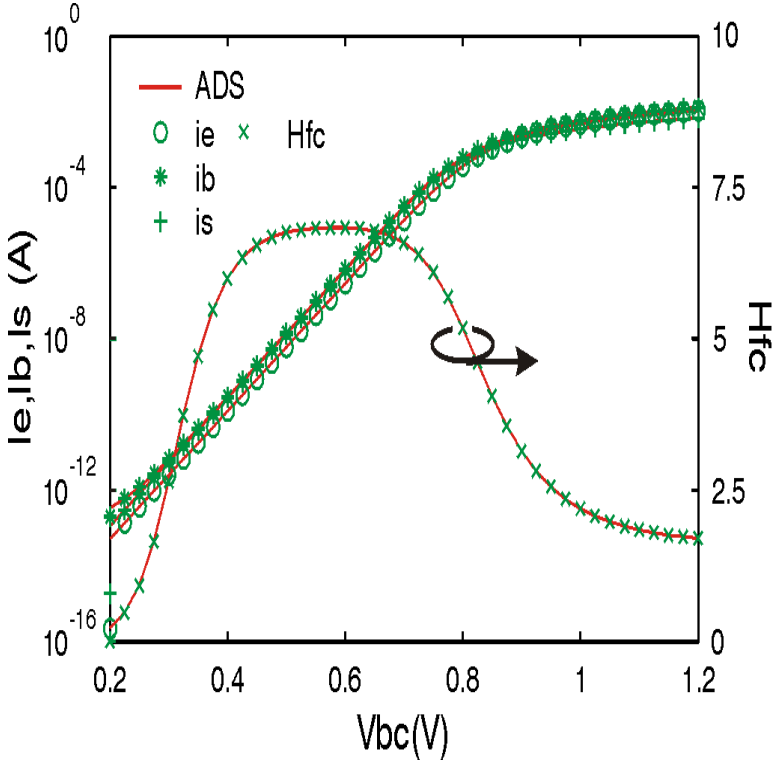
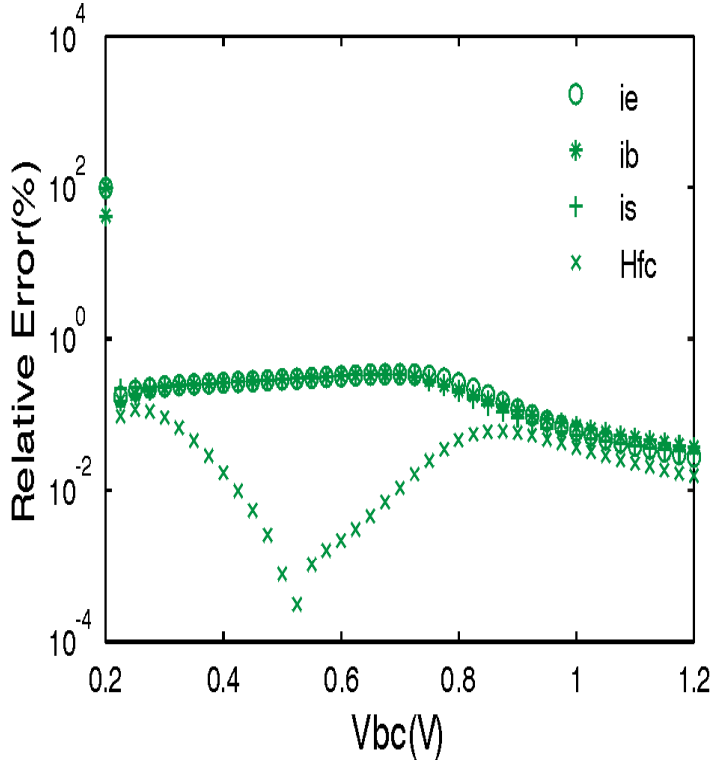
Reverse Gummel characteristics and relative errors





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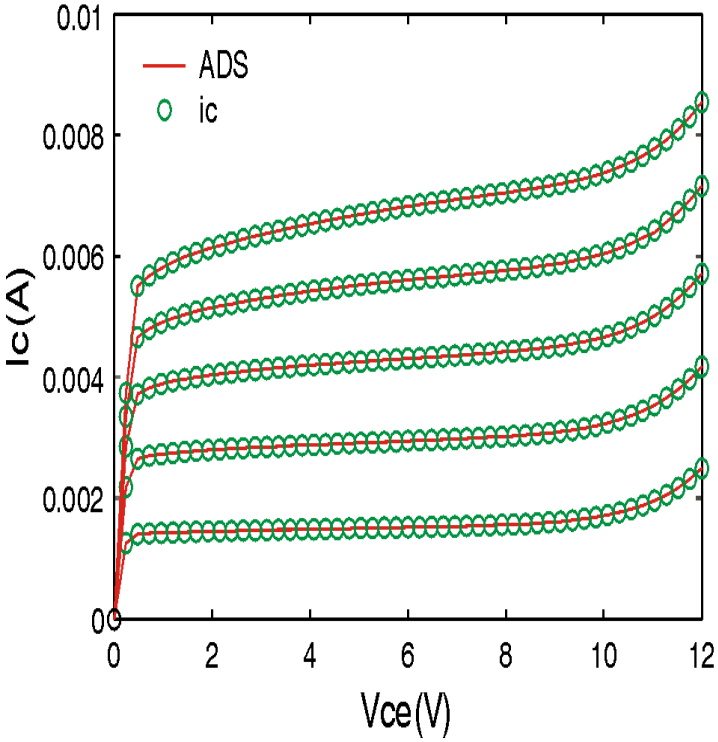
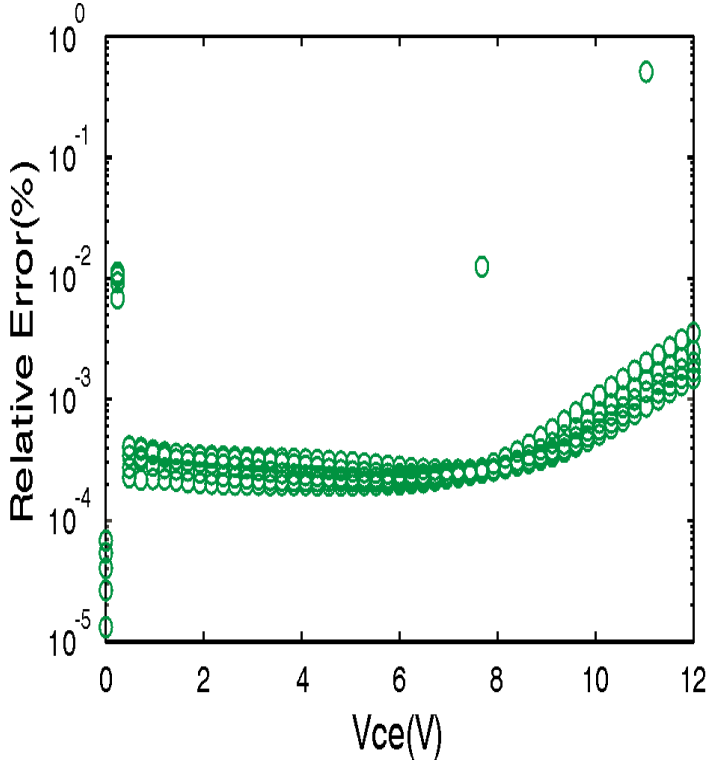
Output characteristics and relative errors





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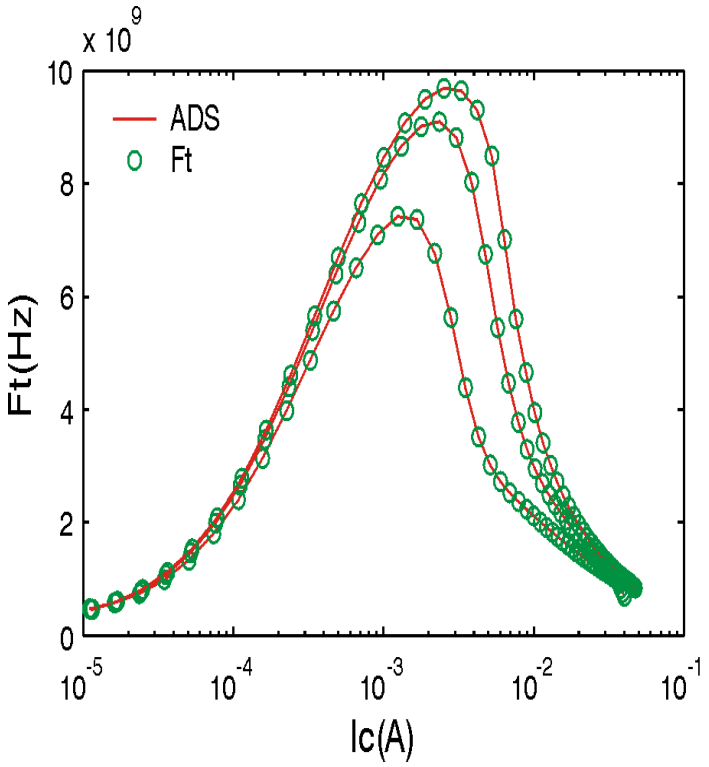
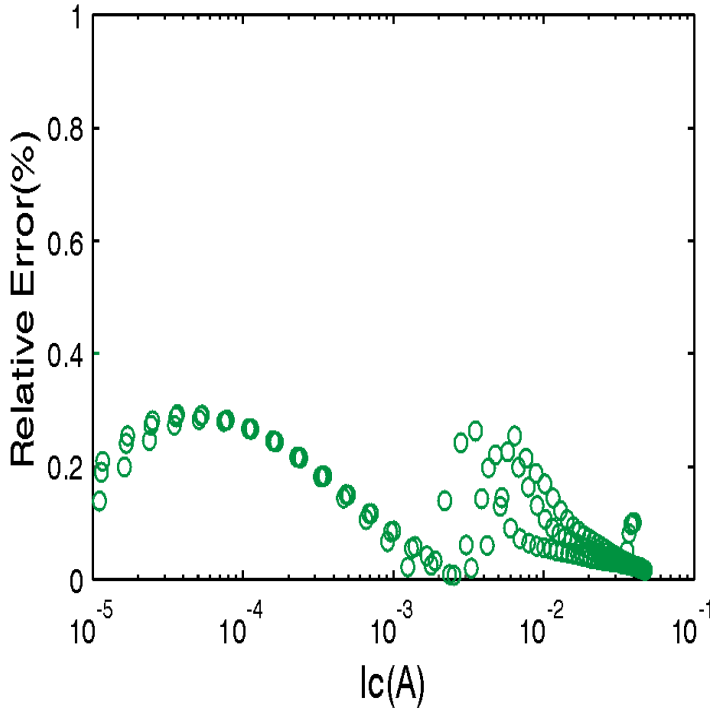
Ft vs. Ic and relative errors





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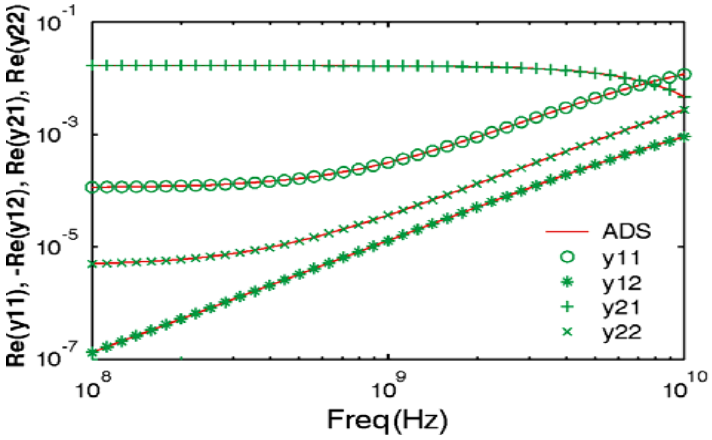
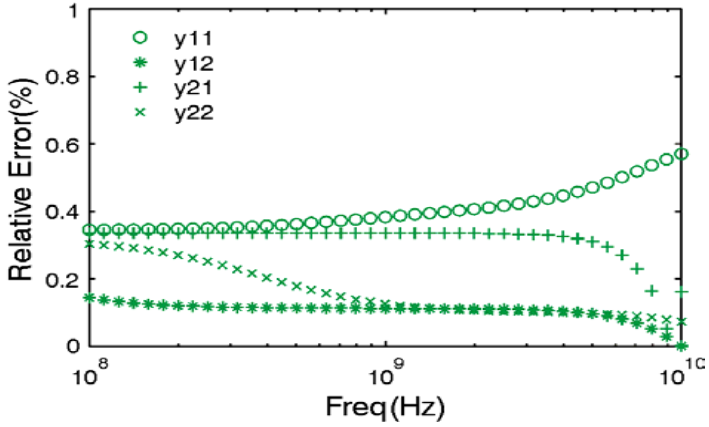
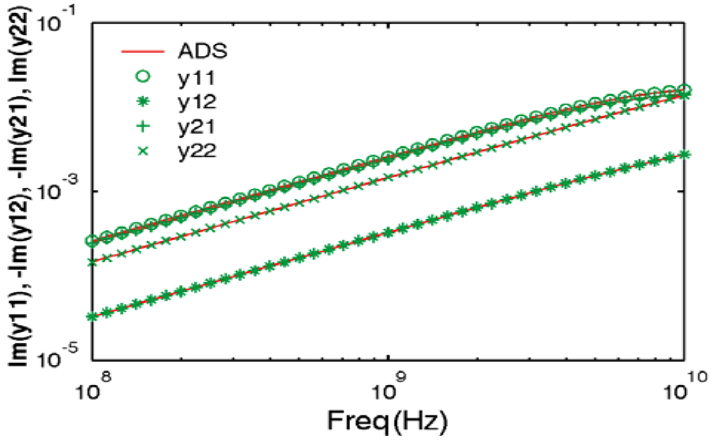
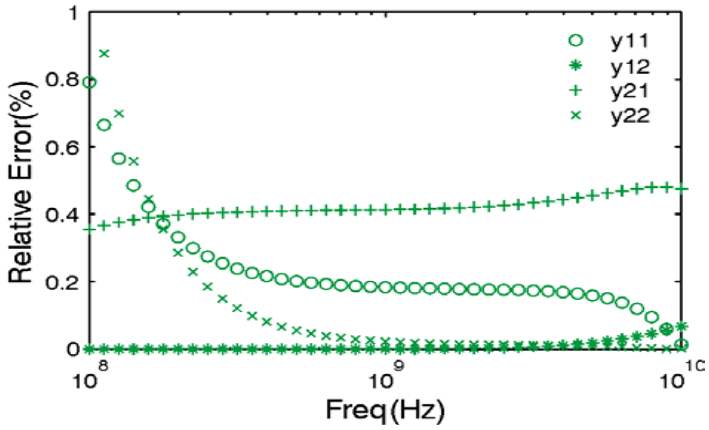
Real, Imaginary y-parameters and relative errors









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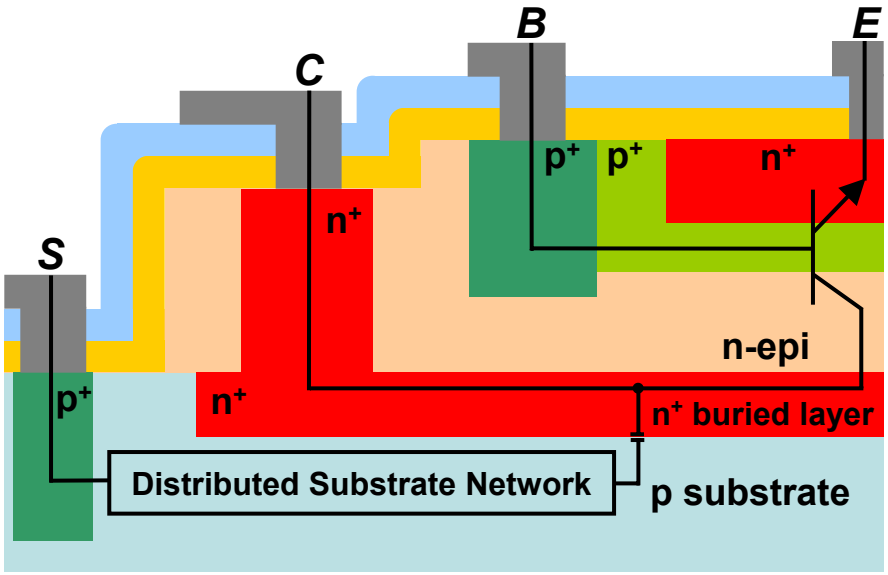
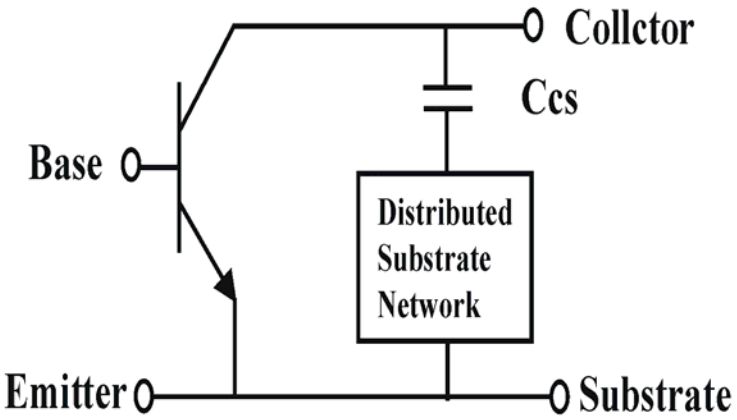
Behavior modeling of substrate effect





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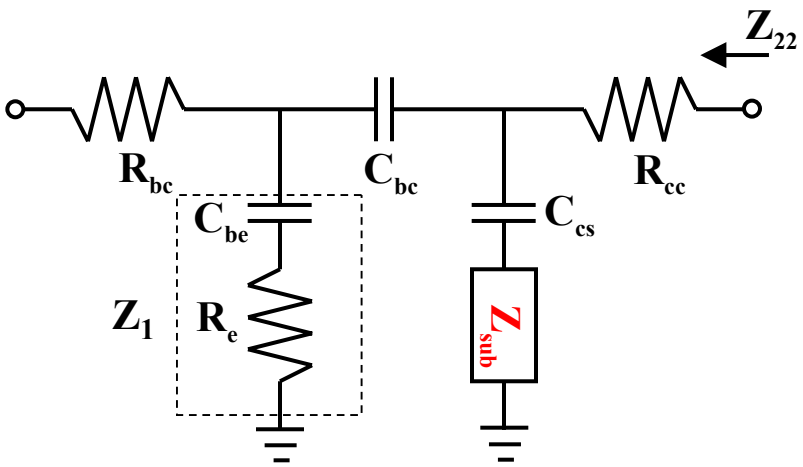
Extraction of measured substrate impedance



Off state small-signal equivalent circuit of a bipolar transistor

$$Z_{22} = R_{cc} + \left(\frac{1}{Z_{sub} + \frac{1}{SC_{cs}}} + \frac{1}{Z_1 + \frac{1}{SC_{bc}}} \right)^{-1}$$

$$Z_{sub} = \frac{(Z_{22} - R_{cc})(1 + SC_{bc}Z_1)}{1 + SC_{bc}(Z_1 - Z_{22} + R_{cc})} - \frac{1}{SC_{cs}}$$

$$Where \;\; Z_1 = R_e + \frac{1}{SC_{be}}$$

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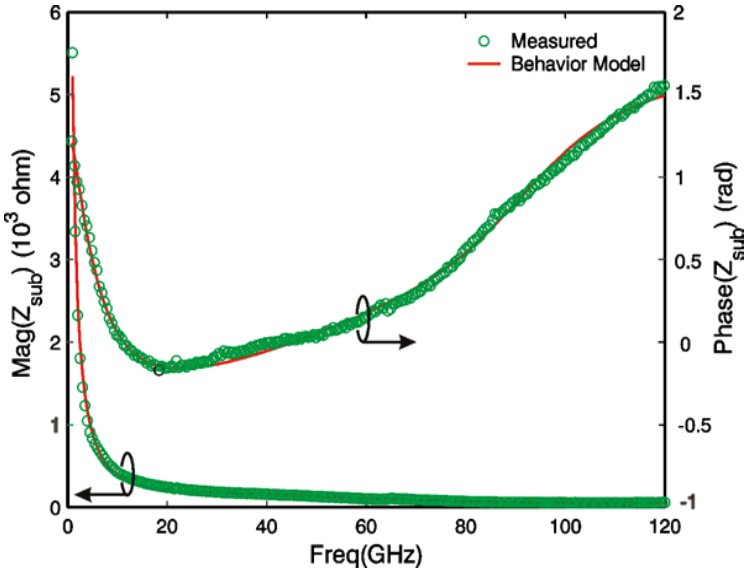
Extraction of substrate impedance

$$Z_{sub}(s) = \frac{\sum_{k=1}^{n} a_{n-k}\, s^{n-k}}{\sum_{k=0}^{n} b_{n-k} s^{n-k}}$$

Least square fit to measured Z_{sub}

$n = 6$ gives good fit to measured Z_{sub}



$$Scale\_factor = \frac{1}{2\pi \times 10^9}$$

$a_0 = -1.2539 \times 10^{12}$

$a_1 = 9.2386 \times 10^{10} \times scale\_factor$

$a_2 = 5.0314 \times 10^{9} \times scale\_facrtor^2$

$a_3 = -5.9068 \times 10^{7} \times scale\_factor^3$

$a_4 = 3.5507 \times 10^{4} \times scale\_factor^4$

$a_5 = -1.0560 \times 10^{4} \times scale\_factor^5$

$b_0 = -2.7422 \times 10^{7}$

$b_1 = 2.3107 \times 10^{8} \times scale\_factor$

$b_2 = 4.2432 \times 10^{7} \times scale\_factor^2$

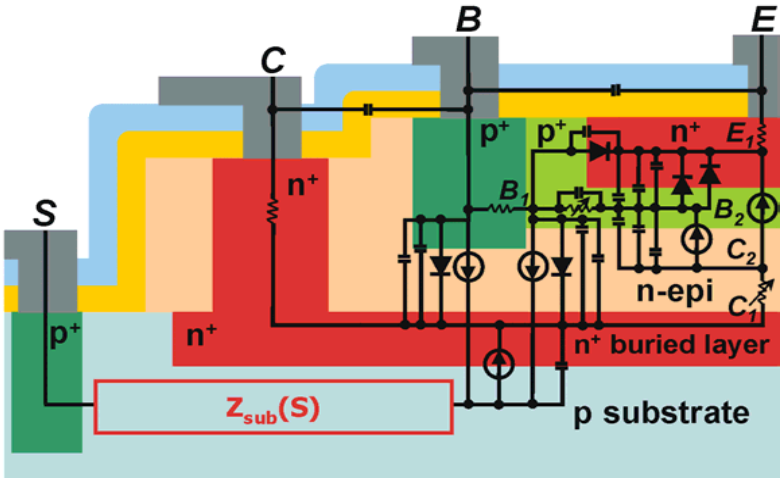
$b_3 = -4.3021 \times 10^{5} \times scale\_factor^3$

$b_4 = 4.3207 \times 10^{3} \times scale\_factor^4$

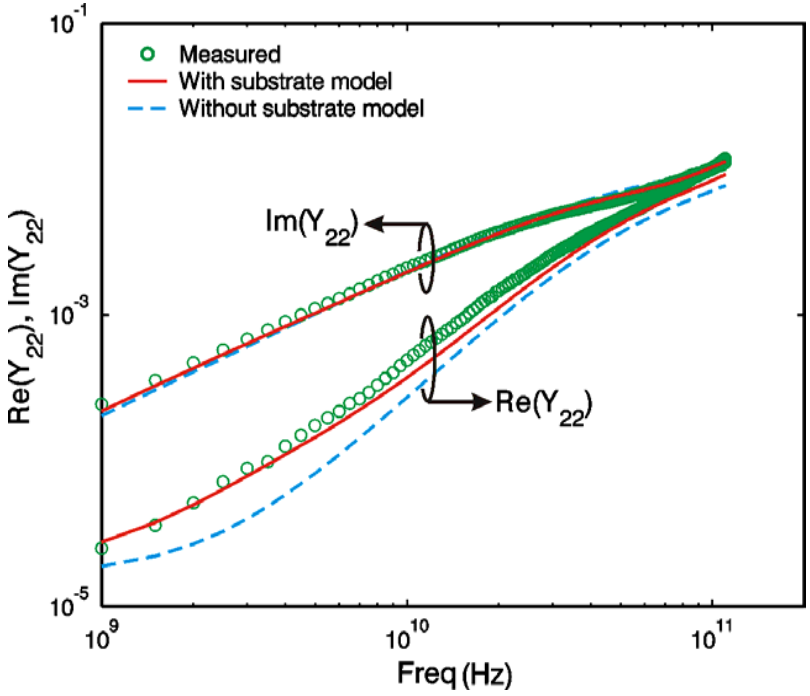
$b_5 = 7.4071 \times scale\_factor^5$

$b_6 = 1 \times scale\_factor^6$

Implementation and Verification of substrate network



$$V(s,g) <+ laplace\_nd\left(I(s,g), a, b\right)$$



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Discussion

- Verilog-A facilitates quite ”compact” representation of the compact models (~800 lines for Mextram 504 in Verilog-A) due to :
  a) Interfaces to the simulator
  b) Derivatives of electrical quantities
- However, a writer of the AHDL code is still fully responsible for the numerical stability of the governing model equations (smooth transitions, range of functions, etc.); good programming practice and experiences from the C-code implementations could be very useful

Conclusion

- Verilog-A indeed represented an effective environment for the fast implimentation and exchange of new compact modeling ideas.
- It will also be employed for implementation adds on modeling features like substrate coupling and other network, like improved thermal coupling network, etc.

Acknowledgement

We would like to thank :

- Mr. R.J. Havens and Dr. J. C. J. Paasschens both from Philips Research for high frequency measurement and helpful discussions
- Philips financial support of the project
- TSMC offers test devices

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