Construction of a VHDL-AMS Simulator in Matlab™

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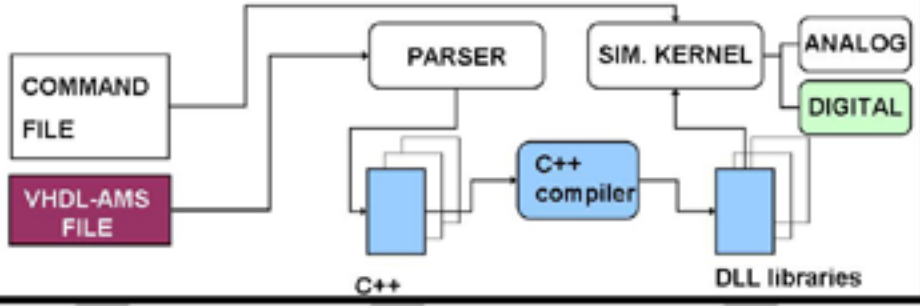
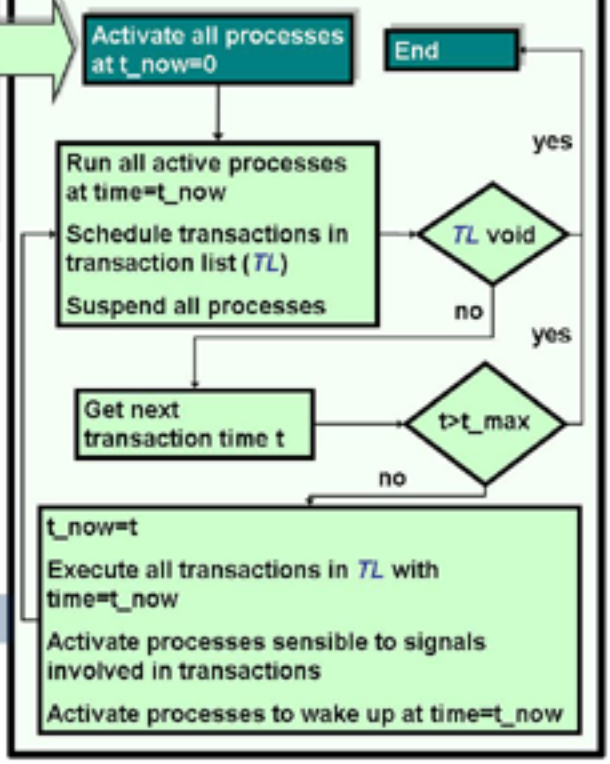
Abstract:
In this work we describe the digital kernel implementation of the simulator S.A.M.S.A., a tool for the simulation of Vhdl-Ams systems in Matlab™. The digital kernel was validated by simulating different systems. In particular we will show the simulation of a low-power multistage decimator for a Δ-Σ wideband Analog to Digital Converter (ADC). This example was correctly simulated given the same results as other VHDL commercial tools.

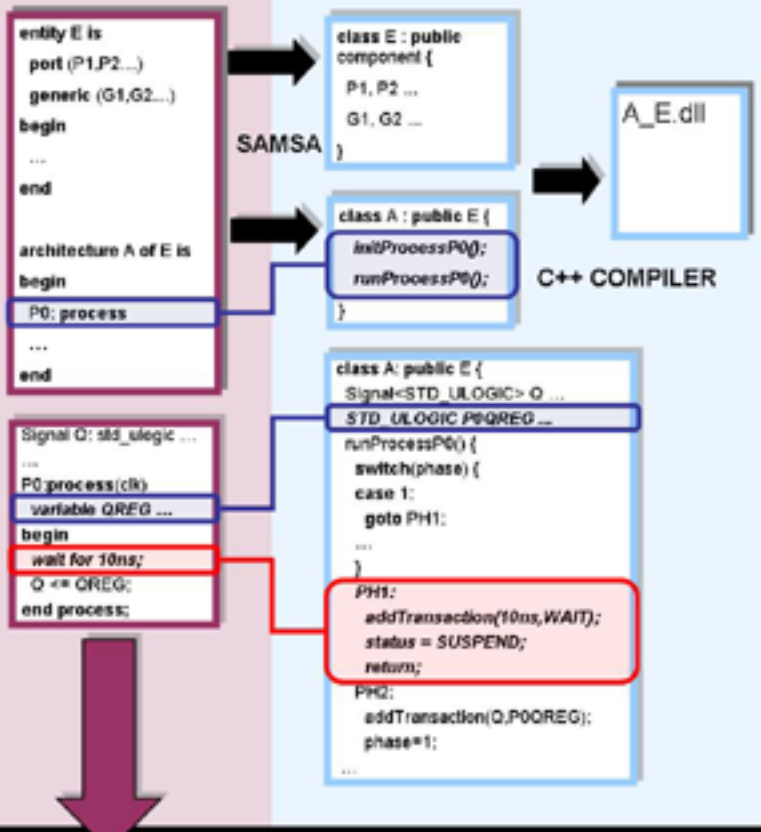
SAMSA architecture



Digital kernel algorithm

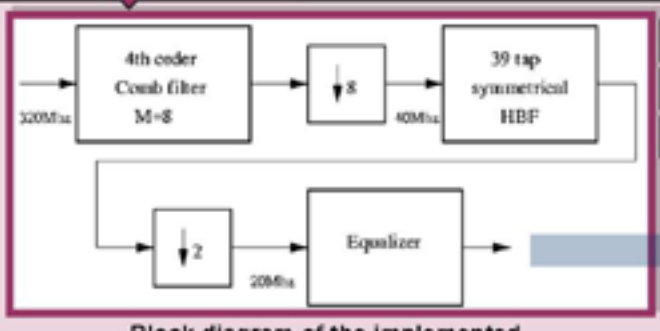


VHDL-AMS mapping



Example: low power multistage decimator

The proposed example is the VHDL implementation of a low-power multistage decimator for a wideband Δ-Σ analog to digital converter (ADC). More exactly, the output of a 2-bit 2nd order Δ-Σ Modulator (DSM) with optimized Noise Transfer Function (NTF) is supposed to be sampled at Fs=320Ms/s having an oversampling ratio OSR=Fs/2fB=18.82 where fB=8.5MHz is the baseband frequency of the signal of interest (like could be for example an OFDM signal in the standard IEEE802.11). The simulated decimator down-samples the output of the converter to 20Ms/s applying a decimation factor of M=16 and meeting requirements like almost same SNR at the output of the decimator as in input (SNR=60[dB] or 10 equivalent bits), low power consumption (less than 10mW) and latency delay less than 1μs.

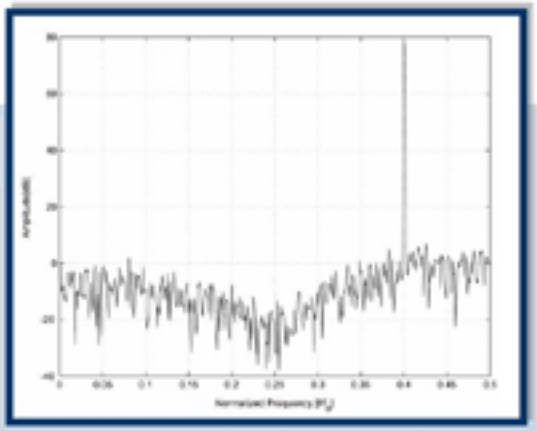


Block diagram of the implemented decimator.

74 COMPONENTS
607 INSTANCES
4478 PROCESSES

OUTPUT

SAMSA



Decimated signal power spectral density (N = 1024 samples)