A high-level VHDL-AMS model design methodology for analog RF LNA and Mixer

Wei Yang
yangwe@ececs.uc.edu

Hal Carter
hal.carter@uc.edu

Jianping Yan
yanj@ececs.uc.edu

Distributed Processing Laboratory, Department of ECECS,
University of Cincinnati, Cincinnati, OH 45220

***Abstract*—**VHDL-AMS supports the time and frequency domain modeling and noise modeling which make the RF circuit and system modeling in VHDL-AMS possible, while some restrictions do exist. For instance, the parameters of 'LTF attribute of a quantity must be static is a difficulty to model a flexible bandwidth specification. We represent a methodology to design and optimize the analog RF circuit in VHDL-AMS to get a RF model with flexible specification input and high fidelity to noise and nonlinearity issues. Some suggestions on the extension of VHDL-AMS simulator to better support the RF circuit and system simulation are presented.

***Keywords*—**VHDL-AMS, SoC, Model, Filter, LNA, Noise Figure, IIP3

I. INTRODUCTION

With rapidly increasing transistors density and the booming market of wireless applications, several new areas in the integrated circuit design are System-on-Chip (SoC, both digital and mixed signal) and increased operating frequency. These complex SoCs always integrate digital signal processing and control part together with analog transceiver front-end in a single die. Though the digital circuit's top-down design procedure has been fully developed, design of the RF analog front end was always a very intensive process which makes the gap between the need of rapid time-to-market and the complex design and verification procedure of the SOCs.

Thus new or extended electronic design automation tools and design method are needed. For instance, it is impractical to simulate a full chip at the transistor level in SPICE. At the same time, design analog or RF blocks and verification in a high level or top level allows the developing team to design the complex chip by a top-down methodology and check whether the subsystem fulfill the specifications of the system from the beginning. Rather, new simulation languages, environments and verification methodologies are needed [1].

VHDL allows the digital system can be designed by a top-down methodology. VHDL-AMS which is a superset of VHDL is a relative new standard description language for modeling mixed-signal and mixed-technology system. An advantage of VHDL-AMS is that it supports modeling a system at different levels of abstraction from behavioral level to circuit level thereby providing an appropriate trade-off between accuracy and simulation time [2].

A need exists to create a SoC model library containing building blocks from which a system designer can select, configure, integrate and simulate the collection of models representing the behavior of a designed system. System designers desire accurate models that can be easily specified. Some related research has been done. In [2], components of a FM receiver are modeled and simulated in VHDL-AMS. Parts of these models are behavioral model and parts of them are structural models. However, nonlinear and noise issues had not be considered in the models. An existing model library designed to support analog and RF design is the behavioral RF library implemented in Verilog-A by Cadence that contains eight models including filters and LNA [3]. In [3], the scattering or S parameter concept is used to model the two port network and the concept of equivalent noise temperature (Te) is used to model the noise of the circuit. A VHDL-AMS library of RF blocks models have been design in [4], but in these models, the noise figure and IIP3 which are important RF specifications have not been considered to be the input of the models.

This paper presents a high-level VHDL-AMS model design methodology for analog RF front-end circuit. A method of using an automation procedure to design, optimize and publish the VHDL-AMS models is presented. Thus, high fidelity VHDL-AMS model with any specification can be generated in a very short time to fulfill the need of the SOC's first stage design and the stage of verification. After giving background in section 2 and demonstrating the design and optimization methodology in section 3, a LNA is given as an example. Its behavioral model is validated compared with a transistor level LNA implemented in TSMC25 technology in section 4. Conclusion, future work and some assumptions had been made are provided in section 5.

II. BACKGROUND

A. EDA Tool and Modeling Language Requirements for RF

1) In order to evaluate the performance of RF circuit and system, the EDA tool must support time-domain and frequency-domain simulation. The modeling language must

support the time-domain and frequency-domain model.

2) Noise and harmonic nonlinearity issues in high frequency communication system are such big concerns that EDA tool must support noise simulation and harmonic analysis. The modeling language must have the feature of modeling the noise and nonlinearity or thus features can be created in the circuit model.

3) In order to simulate and verify the RF circuit and system, especially to fulfill the demand of top-down design and mixed-mode simulation, EDA tool and modeling language also need to support high abstraction level simulation and modeling and support the simulation in hierarchical system.

B. Capability of VHDL-AMS

VHDL-AMS which is a superset of VHDL language is a very rich-featured language to model the analog, mixed-signal and mixed-mode system.

VHDL-AMS supports time-domain and frequency-domain modeling. VHDL-AMS also support noise modeling by noise source quantity. VHDL-AMS provides for various numerical forms and supports flexible modeling objectives[8].

Though some restrictions like the requirement of the coefficients of 'LTF attribute of a quantity must be static set some limits on flex modeling, some strategy can be used to conquer it. However, VHDL-AMS simulation needs some extension to support the RF circuit simulation.

C. Suggested extensions for VHDL-AMS simulator

In order to evaluate the non-linearity performance of RF circuit and system, either the harmonic analysis should be included as part of the simulator or a harmonic analysis package can be developed for VHDL-AMS to be a part of the IEEE standard.

III. DESIGN APPROACH

A. Modeling the impedance matching

The models are designed to be input impedance matching with the input source $50\,\Omega$ impedance at designed frequency. To model the non-real impedance at the input of the model at other frequencies, a passive series RLC network is used. The value of the resistor designed to be $50\,\Omega$. The value of the inductor will be set to an experienced value according to the designed frequency. The value of the capacitor is computed according to the designed frequency and the value of the inductor by equation (1).

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad (1)$$

ω_0 is the designed frequency.

B. Modeling the function of the RF block

The functions of RF blocks are different. For LNA, the function is a gain, so the block function is an expression which is the input signal multiplied by a constant. This constant is computed according to the specified gain. For a mixer, its basic function is to provide frequency translation. If it is a passive mixer, it does not provide any gain, while active mixers generally provide gain. The function of frequency translation can be expressed by a multiplication of two signals in the time domain by equation (2) [6].

$$(A\cos\omega_1 t)(B\cos\omega_2 t) = \frac{AB}{2}[\cos(\omega_1 - \omega_2)t][\cos(\omega_1 + \omega_2)t] \qquad (2)$$

C. Modeling the bandwidth

1) Behavioral model of filter in VHDL-AMS

To model the bandwidth of RF circuit in VHDL-AMS, an automation tool is designed to generate behavioral VHDL-AMS filter model [7].

Butterworth bandpass filter is chosen to model the bandwidth of RF circuit.

2) Modeling bandwidth of RF circuit

For RF circuit, people do not want to attenuate the useful (in-band) signal too much. Usually -3dB is used as a limit for attenuation. While if a wide band RF circuit is designed, the maximum attenuation of the in-band signals should be as small as possible and -3dB seems a little bit large. Using -0.2dB as the limit for maximum attenuation is obviously not bad.

After initializing the coefficients of the Laplace transfer function, repeat procedure of simulating, measuring the 0.2dB point and changing the edge frequencies of the filter starts till the bandwidth specification is fulfilled. Then the coefficients of Lapace transfer function will be set to model the bandwidth model of the circuit.

D. Modeling the noise

A very important characteristic of LNA and mixer is noise figure. To model a specified noise figure and at the same time keep the input impedance matching, two resistors are used. The idea is illustrated by Figure 1.

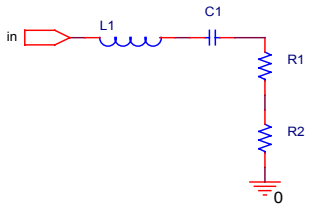

Figure 1: model for noise figure

R1 is a noisy resistor which contributes noise to the whole

circuit. R2 is an ideal resistor which acts as a non-noisy resistor. The value of R1 will be between zero and $50\,\Omega$. The design automation tool uses bisection algorithm to optimize the value for the R1 according to the specified noise figure. The value of R2 should be computed according to equation (3) to keep the model's input impedance matching at the designed frequency.

$$R2 = 50 - R1 \tag{3}$$

E. Modeling the nonlinearity

Another very important characteristic of LNA and mixer is IIP3 point.

Assume the non-linear behavior of the RF circuit is

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 \tag{4}$$

When x(t) are the signals with different frequencies and assume x(t) = $A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, we get the following intermodulation products[6]:

$$\omega = \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t \tag{5}$$

$$= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2)t \tag{6}$$

$$= 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 - \omega_1)t \tag{7}$$

and fundamental components[6]:

$$\omega = \omega_1 : (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2) \cos \omega_1 t \tag{8}$$

$$\omega_2 : (\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2) \cos \omega_2 t \tag{9}$$

In a typical two tone test, $A_1 = A_2 = A$. The ratio of the amplitude of the output third-order products to $\alpha_1 A$ defines the IM distortion (IMD) [6].

The IIP3 is

$$IIP_3|_{dBm} = \frac{IMD}{2} + P_{in}|_{dBm} \tag{10}$$

Since other frequency in intermodulation products of the two tone signal are not big concern, the equation (4) is enough to model nonlinearity characteristic of RF circuit. The value of α_1 is designed by simulating the circuit and measuring the output fundamental component's amplitude, if it is fulfill the gain designed in the previous procedure within a tolerance, then the value of α_3 is optimized using bi-section algorithm. Since the intermodulation product of $\omega_1 \pm \omega_2$ is not the concern, α_2 is set to be 1.

F. Design Flow

The design flow of a procedure that implements the approach presented above is shown in Figure 2. Each design and optimization block is a repeat simulation procedure. To describe this procedure clearly, the noise model design and optimization block is given as an example and is shown in Figure 3.

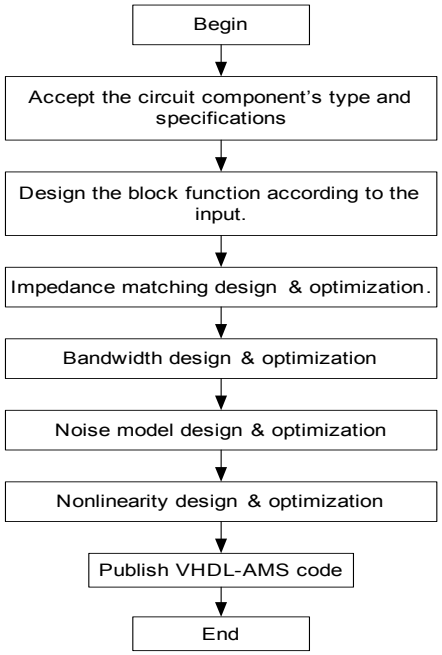

Figure 2: The design flow for behavioral modeling RF amplifiers and mixers

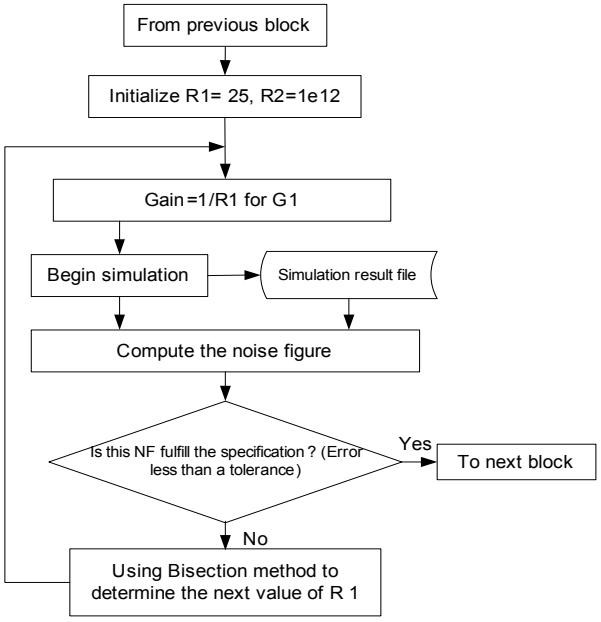

Figure 3: The design flow of noise modeling block

IV. MODEL VALIDATION IN THE CASE OF LNA

In this section, the design methodology is validated by comparing the simulation results between the behavioral model and transistor-level circuit of a 1.9GHz LNA implemented in TSMC25 technology.

A. Transistor- level 1.9GHz LNA in TSMC25 technology

Common-source cascade amplifier with source inductive degeneration configure is chosen to use [5].

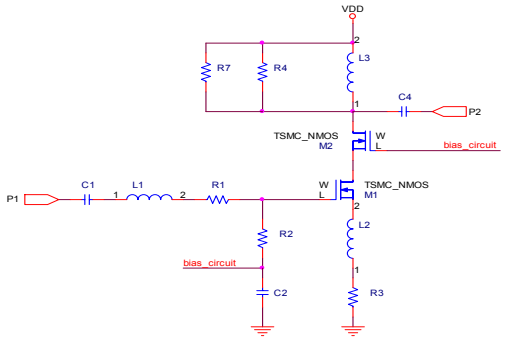

Figure 4: The schematic of a 1.9GHz LNA in TSMC25 technology

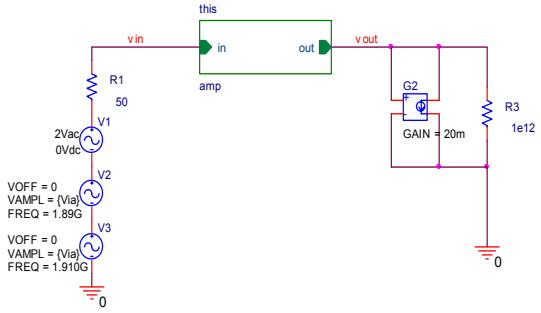

Figure 5: The test circuit of the LNA

G2 together with R3 in Figure 5 act as a 50Ω ideal resistor without any noise.

The characteristics of this LNA are listed in Table1.

Table 1: Characteristic Table of the transistor level LNA

Gain	17.1dB
Bandwidth	>25M
Noise Figure	0.775dB
IIP3	3.62dBm

B. Behavioral model LNA in VHDL-AMS

Table 2: Parameters in the behavioral LNA model

L1	10nH
C1	701.67f
R1	9.75Ω
Gain of G1	24.8e-3
R2	1e12
Laplace transfer function	$\frac{3769911040.0s}{14251708750730205593 6.0+3769911040.0s+s^2}$
Coefficients for the nonlinearity expression	$\alpha_1=1,\ \alpha_2=1,\ \alpha_3=0.1183$

C. Model Validation

1) Gain and Bandwidth Simulation

The gain and bandwidth model is validated by VHDL-AMS simulation with the results shown in Figure 6.

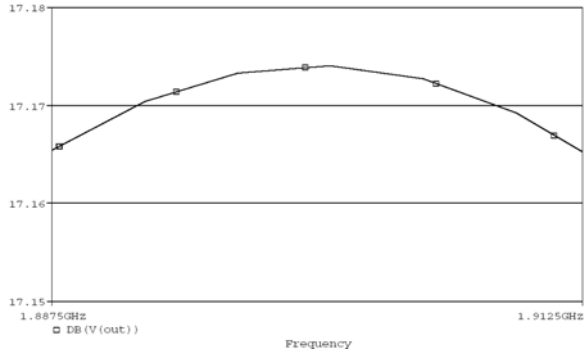

Figure 6: Gain and bandwidth simulation

Figure 6 shows that the gain variation between 1.8875Ghz and 1.9125Ghz is 0.01db, the bandwidth requirement is met.

2) Noise Figure Simulation

We included noise in the VHDL-AMS model, but since the simulator available to us did not have the noise source implemented, we converted the model to Spice and simulated it.

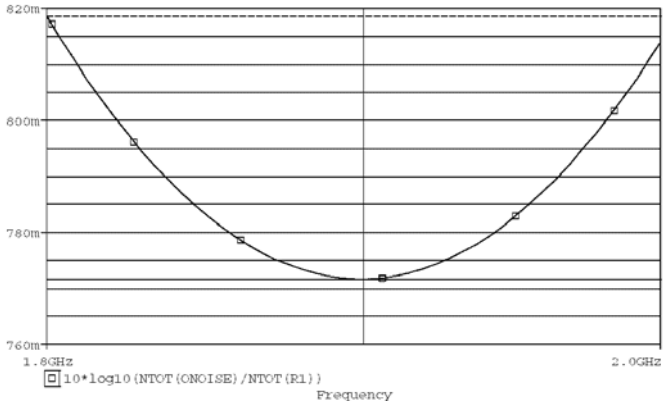

Figure 7: Noise figure simulation

Figure 7 shows that the noise figure at 1.9Ghz is 0.772dB.

3) Two-tone analysis

The two-tone analysis test circuit is setup as Figure 5. The simulation result is shown in Figure 8. The four signals are the third order intermodulation products of the two input signals and the fundamental components respectively. The IMD equals to 60.0182dB according to the definition of IMD and Pin (the mean of the input power) equals to -26.48dBm by hand

computation. So we get the IIP3 equals to 3.52dBm according to equation (10). Results of the characteristic of the behavioral LNA model are listed in Tables 3.

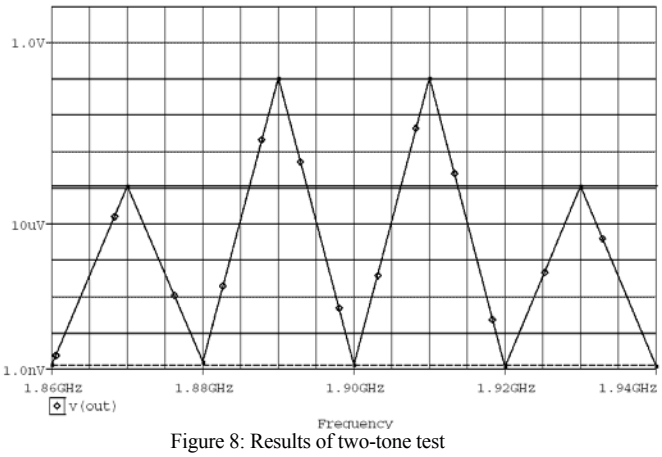

Figure 8: Results of two-tone test

Table 3: Characteristic Table of the behavioral LNA

	Value
Gain	17.174dB
Bandwidth	>25M
Noise Figure	0.772dB
IIP3	3.52dBm

Comparison between Table 1 and Table 3 shows that the generated model's characteristics have fidelity to the transistor level counterpart. Since the analog kernel solves the equations in the same way by SPICE and VHDL-AMS, these results should be the same after simulation by VHDL-AMS simulator once noise quantities are available in the VHDL-AMS simulator.

Figure 9 shows the LNA VHDL-AMS model.

V. CONCLUSION

This modeling methodology is not necessarily general for all RF components, but is applicable to low noise amplifier and mixers since LNAs and mixers have similar specifications. In the future, this methodology will be extended to design oscillators and PLLs.

To support RF circuit and system simulation and verification, harmonic analysis or FFT function is suggested to be added as part of the simulator or as a standard package.

```
architecture stru_beha of lna is
   constant num:real_vector:=(0.0, 3769911040.000000);
   constant den:real_vector:=(1425170875073020559360.000000000,
                              3769911040.000000000, 1.000000000);
   constant CAP:real:=701.67e-15;
   constant IND:real:=10.0e-9;
   constant R1:real:=9.75;
   constant R2:real:=40.25;
   constant GAIN_OF_G:real:=22.1e-3;
   constant GAIN:real:= 7.146;
   constant ALPHA_1:real:=1.0;
   constant ALPHA_2:real:=1.0;
   constant ALPHA_3:real:=0.1183;
   quantity vin across iin through input to electrical_ref;
   quantity vout across iout through output to electrical_ref;
   terminal t1, t2, t3, t4, t5: electrical;
   quantity v_lap_in  across i_lap_in  through t2 to electrical_ref;
   quantity v_lap_out across i_lap_out through t4 to electrical_ref;
   quantity v_after_5 across t5 to electrical_ref;
begin
   L1: entity work.inductor(ideal)
       generic map( ind => IND)
       port map   (p1=> input, p2=> t1)
   C1: entity work.capacitor(ideal)
       generic map( cap => CAP)
       port map   ( p1=> t1, p2=> t2)
   R1: entity work.resistor(noisy)
       generic map( res => R1)
       port map   ( p1=> t2, p2=> t3)
   R2: entity work.resistor(ideal)
       generic map(res => R2)
       port map   ( p1 => t3, p2 => electrical_ref)
   v_lap_out=v_lap_in'ltf(num, den);
   v_out_5 = GAIN*v_lap_out;
   vout = v_out_5*ALPHA_1+v_out_5*v_out_5*ALPHA_2
          +v_out_5*v_out_5*v_out_5*ALPHA_3
end architecture stru_beha;
```

Figure 9: LNA VHDL-AMS model

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