Automatic Generation of Compact Semiconductor Device Models using Paragon and ADMS

Vivek Chaudhary, Matt Francis, Wei Zheng, Alan Mantooth, Laurent Lemaitre*

Mixed Signal CAD Laboratory
Department of Electrical Engineering
University of Arkansas

*Freescale Semiconductor
Geneva Switzerland
Outline

- Introduction
- Abstract Model Representation
- XML Schema
- Modeling Methodology
- Model Compilation
- BSIMSOI Model
- Conclusion
Introduction

- Semiconductor device modeling is extremely time consuming
- Model implementation in SPICE-like simulators is cumbersome
- Designers from different scientific backgrounds do not use the same analysis tools or same modeling languages
Various Levels of Abstraction

- GUI-based tools (Paragon)
- Language Independent Model Abstraction
- Simulator-Specific Code (SPICE, Spectre, etc.)

Supports multiple languages

Highest level description of model behavior

One model supports several simulators
Model Representation

Goals for XML format:
- Simulator independent
- Higher than HDLs
- Captures semiconductor device physics and multi-physics (electro-thermal, etc.)

XML

VHDL-AMS  HDLs  Verilog-AMS

C/C++ (SPICE, Spectre, Eldo)
Why XML?

XML:
• Superset of HTML, simple/structured format
• Lends itself to open source and standardization
• Much XML-based technology already exists
  • Example: MathML, used for model expressions, is becoming *de facto* standard for math on the web
• Extensible
• Self-documenting
<?xml version="1.0"?>
<!DOCTYPE model [
<!ELEMENT model (comment?, interface, body+)>
<!ATTLIST model
  name CDATA #REQUIRED
  version CDATA #REQUIRED>
<!ELEMENT comment (#PCDATA)>
<!ELEMENT interface (comment?, parameter*, port*)>
<!ELEMENT parameter (comment?, validity*)>
<!ATTLIST parameter
  default CDATA #IMPLIED
  name CDATA #REQUIRED
  nature (real | integer | time) #REQUIRED
  unit CDATA #REQUIRED
  type (instance | process) #REQUIRED>
<!ELEMENT validity (range+)>
<!ATTLIST validity
  message CDATA #REQUIRED
  type (note | error | warning) #REQUIRED>
<!ELEMENT range EMPTY>
<!ATTLIST range
  min CDATA #REQUIRED
  max CDATA #REQUIRED
  exclude_max (yes | no) #IMPLIED
  exclude_min (yes | no) #IMPLIED>
<model>
  <!-- model interface ports -->
  <!ELEMENT port (comment?)>
  <!ATTLIST port
    name CDATA #REQUIRED
    mode (in | out | inout) #REQUIRED
    nature (electrical | mechanical_angular_speed |
    mechanical_angular_displacement |
    mechanical_translational_speed | mechanical_translational_displacement | thermal | optical |
    magnetic) #REQUIRED
    type (terminal | quantity | signal | logic) #REQUIRED
  >
  <!-- end of model interface declaration -->
  <!-- model body -->
  <!ELEMENT body (branch*, equation*, piecewise*, eqblock*,
  macromodel*)>
  <!ATTLIST body
    name CDATA #REQUIRED
  >
  <!-- model body symbol -->
  <!ELEMENT symbol (vector_graphics)>
  <!-- model body branch -->
  <!ELEMENT branch (connection+, quantity+, equation*,
  piecewise*, eqblock*, comment?)>
  <!ATTLIST branch
    name CDATA #IMPLIED
  >
  <!-- model body branch quantity -->
  <!ELEMENT quantity EMPTY>
  <!ATTLIST quantity
    name CDATA #REQUIRED
    nature (through | across) #REQUIRED
    unit CDATA #IMPLIED
  >
Modeling Methodology

Paragon UI

VHDL-AMS

MCAST Model Compiler

spice3f5

XML

Verilog-A

ADMS Model Compiler

Spectre C (CMI Interface)
Model Compilation

- Model compilation is automatic generation of compact semiconductor device models for various SPICE-like simulators.
- ADMS is a freely available model compiler for SPICE-like simulators.
Advantages

- Model development time is dramatically reduced
- Generated model is easier to maintain and reuse
- Same abstract representation of the model can be used by a model compiler to generate low level C/C++ code for different simulators
Paragon Implementation
Paragon Implementation

```
PARAGON - Model Creator (bsimpd)

10/25/2004
```
Paragon Implementation
Model Compilation using ADMS

Paragon UI

XML

Verilog-A

ADMS Model Compiler

Spectre C (CMI Interface)
Results

- Duration: about two week to implement and validate the BSIMSOI model in Paragon model and generate C model for Spectre using ADMS.
- Results for all analyses match exactly with native Spectre model
Interesting Behavior
Relative Performance

Transient analysis of a 2 transistor circuit
## Relative Performance

<table>
<thead>
<tr>
<th>Model</th>
<th>CPU time</th>
<th>Time factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Native Spectre</td>
<td>140ms</td>
<td>1X</td>
</tr>
<tr>
<td>Verilog-AMS</td>
<td>33.2s</td>
<td>237X</td>
</tr>
<tr>
<td>ADMS</td>
<td>200ms</td>
<td>1.4X</td>
</tr>
</tbody>
</table>

![Diagram of a circuit labeled Vdd](image)
Radhard Opamp
DC Curve
Open Loop Frequency Response

Magnitude Plot

Phase Plot

10/25/2004
Conclusion

- Modeling methodology described enables the user to quickly and correctly create new compact semiconductor device models for various SPICE and SPICE-like simulators.

- Model development time is significantly reduced.
Conclusion

- Time required to validate and test a new model is also significantly reduced.
- Higher-level XML description of the model is easy to maintain, reuse and update and this leads to an increased efficiency in the overall model creation process.