ARCHITECTURAL AND PARAMETRIC OPTIMIZATION OF LOW-PASS RF FILTERS IN VHDL-AMS BASED HIGH-LEVEL SYNTHESIS

T. J. Kazmierski and F. A. Hamid
{tjk,fah99r}@ecs.soton.ac.uk
Summary

- RF filter modelling in VHDL-AMS for automated architectural synthesis
- Cell selection and architectural optimization using patterns in VHDL-AMS parse tree
- Three-tier parametric optimization embedded in synthesis
- Case study
Architectural filter synthesis from VHDL-AMS

FIST - filter synthesis system

Parse parse tree formation

University of Southampton, UK
## Filter cell models

<table>
<thead>
<tr>
<th>2nd order cell type</th>
<th>Time-domain equation</th>
<th>Equivalent VHDL-AMS simultaneous statement</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Low pass</strong></td>
<td>[ V_{in} = Coeff \times \frac{d^2 V_{out}}{dt^2} + Coeff_2 \times \frac{dV_{out}}{dt} + Coeff \times V_{out} ]</td>
<td>[ vin = \text{coeff1} \times vout' \text{dot}' \text{dot} + \text{coeff2} \times vout' \text{dot} + \text{coeff3} \times vout ]</td>
</tr>
<tr>
<td><strong>Band pass</strong></td>
<td>[ \frac{dV_{in}}{dt} = Coeff \times \frac{d^2 V_{out}}{dt^2} + Coeff_2 \times \frac{dV_{out}}{dt} + Coeff \times V_{out} ]</td>
<td>[ vin' \text{dot} = \text{coeff1} \times vout' \text{dot}' \text{dot} + \text{coeff2} \times vout' \text{dot} + \text{coeff3} \times vout ]</td>
</tr>
<tr>
<td><strong>High pass</strong></td>
<td>[ \frac{d^2 V_{in}}{dt^2} = Coeff \times \frac{d^2 V_{out}}{dt^2} + Coeff_2 \times \frac{dV_{out}}{dt} + Coeff \times V_{out} ]</td>
<td>[ vin' \text{dot}' \text{dot} = \text{coeff1} \times vout' \text{dot}' \text{dot} + \text{coeff2} \times vout' \text{dot} + \text{coeff3} \times vout ]</td>
</tr>
</tbody>
</table>
Sample description of a 1GHz low pass filter

architecture behavioral of filter is
  constant a: real := 4.15e-10;
  constant b: real := 8.64e-20;
  constant c: real := 1.05e-29;
  constant d: real := 7.88e19;
  constant e: real := 6.41e-40;
  constant num: real_vector := (0,0,a);
  constant den: real_vector := (b,c,d,e,1.0);
begin
  Vout == Vin'LTF(num,den);
end architecture behavioral;

Butterworth 4th order

LTF – Laplace Transfer Function
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Architectural optimization process in FIST

AC response data → Three-tier optimisation

Filter netlist → Cost function

Filter Topologies → Architecture Estimator

Library of filter topologies → Filter topology with lowest cost function
Cell selection using VHDL-AMS parse tree (time domain model)

Found SSS in the form term1 + term2 + term3

Reduce filter type from
Cell selection using VHDL-AMS parse tree (frequency domain model)

Found SSS in the form Q2'LTF(num, den)

Static calculator to get and values of num
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Performance criteria

Accuracy of AC response:

\[ err_{total} = \left[ \frac{1}{n} \cdot \sum_{i=1}^{n} err_i^2 \right]^{1/2} \]

where

\[ err_i = \frac{M_i - C_i}{\max(MINVAL, M_i)}, i = 1, n \]

Combined performance criterion:

\[ CF = err_{total} \cdot w + Power \]
Three-tier parametric optimization

Filter specification

Generate frequency response curve

Get filter topologies

Performance verification is based on full HSPICE simulation in innermost tier

Run HSPICE optimisation

amoeba() completed?

no

yes

Randomly generate N+1 sets of N initial points, and evaluate the cost functions

Increment stochastic search counter

Maximum stochastic search count?

yes

no

Log result

Select the best filter cell

More candidate design?

yes

no

Optimised filter netlist

Stochastic search count = 0

no

yes

Generate frequency response curve

Get filter topologies

Run downhill simplex optimisation - amoeba()
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Case study: 4\textsuperscript{th}-order low-pass 1GHz configurations selected by synthesiser

1. Simple OTA cascade
2. Wide-swing OTA cascade
3. LF with simple OTA (BEST)
4. LF with wide-swing OTA
5. IFLF with simple OTA
6. IFLF with wide-swing OTA
Case study: 4\textsuperscript{th}-order low-pass 1GHz synthesis results

<table>
<thead>
<tr>
<th></th>
<th>Topology</th>
<th>Error figure</th>
<th>Size (no of MOSFETs)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Simple OTA cascade</td>
<td>0.663</td>
<td>20</td>
<td>160</td>
</tr>
<tr>
<td>2</td>
<td>Wide-swing OTA with output buffer cascade</td>
<td>0.513</td>
<td>64</td>
<td>2900</td>
</tr>
<tr>
<td>3</td>
<td>LF with simple OTA</td>
<td>0.307</td>
<td>20</td>
<td>163</td>
</tr>
<tr>
<td>4</td>
<td>LF with wide-swing OTA with output buffer</td>
<td>0.634</td>
<td>64</td>
<td>2900</td>
</tr>
<tr>
<td>5</td>
<td>IFLF with simple OTA</td>
<td>0.458</td>
<td>20</td>
<td>111</td>
</tr>
<tr>
<td>6</td>
<td>IFLF with wide-swing OTA with output buffer</td>
<td>380</td>
<td>64</td>
<td>420</td>
</tr>
</tbody>
</table>
Case study: 4\textsuperscript{th}-order low-pass 1GHz

HSPICE simulation results showing ideal curve and curve for best configuration
Conclusion

• A methodology has been developed for behavioural modelling in VHDL-AMS and synthesis of RF analogue filters and its implementation named FIST.
• The synthesis algorithm used by FIST is based on the parse tree of the behavioural VHDL-AMS description.
• Inclusive and vital in the synthesis methodology is the parametric optimisation step which works on a selection of filter cells from a library to give the best filter circuit in terms of accuracy.
• Main application is targeted for integrated RF use; the filter cells as well as the optimisation formulation are geared for this application area.
• The feasibility of the presented method has been demonstrated with two case studies of 1GHz 4th order filter synthesis.