Use of Symbolic Performance Models in Layout-Inclusive Synthesis of RF Low-Noise Amplifiers

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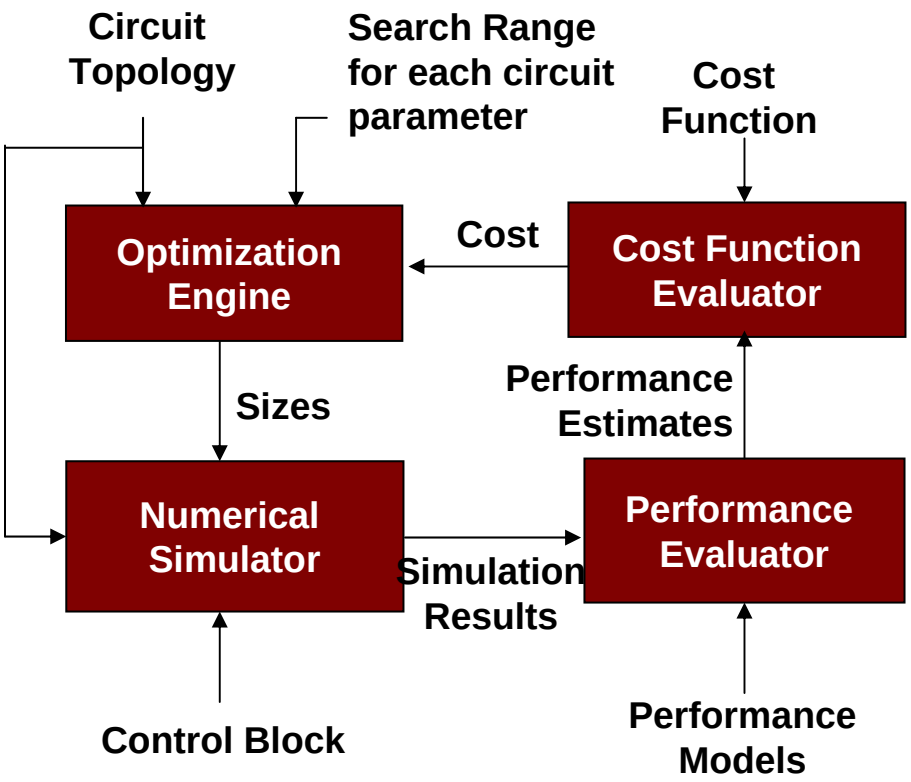
Outline

- Introduction & Motivation
- Proposed Circuit Synthesis Approach
- Layout Generation & Extraction
- Post-Processing
- Symbolic Performance Modeling
- Inclusion of Layout Effects
- Experimental Results
- Conclusions

Analog/RF Circuit Synthesis



Optimization Engine Algos : Simulated Annealing, Genetic Algorithms etc.

Sizes : Values of circuit parameters, like W, L, R, C etc.

Numerical Simulator : Berkeley SPICE, HSpice, Spectre, Eldo, variants of Spice etc.

Control Block : Different Analyses, like, DC, AC, Transient, Distortion, Noise etc.

Performance Models : Methods to use simulation results & generate numerical values of performance parameters

Performance Estimates : Circuit characteristics like, S-parameters, CMRR, Open-loop Gain, Phase Margin etc. HD2, HD3, IM3, IIP3

Motivation

- **Traditional Circuit Synthesis**
  - **Computationally expensive performance estimation due to numerical simulator**
  - **Parasitics unaware / partially aware, leads to failure of synthesized circuit after layout.**

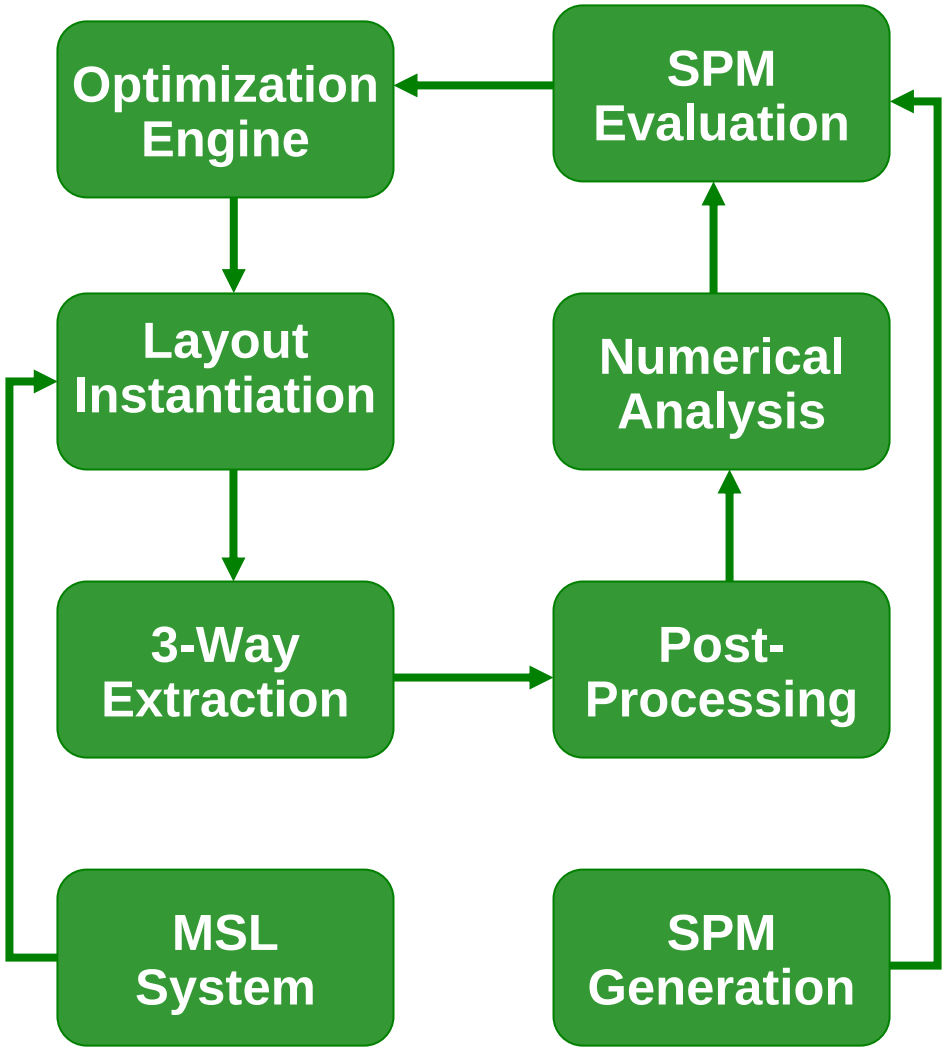
- **Our method**
  - **Performance estimation using Symbolic Performance Models (SPMs).**
  - **Layout-Inclusion in Synthesis Loop using Module Specification Language (MSL).**
  - **Quasi-static extraction of on-chip inductances and interconnects. Rule based extraction of active devices and parasitic capacitances.**

Proposed Circuit Synthesis Approach

Definitions

- **Layout-Inclusive Synthesis**
  - **Layout generation & extraction done in synthesis loop**
  - **Also known as Layout-in-Loop approach**
- **Symbolic Performance Models**
  - **Symbolic equations in terms of circuit parameters**
  - **Built using transfer functions obtained by symbolic analysis.**
  - **Represent the characteristics of analog circuit**
  - **SPMs used for repetitive performance estimation**

Proposed Approach



Layout Generation and Extraction

Layout Generation: MSL System

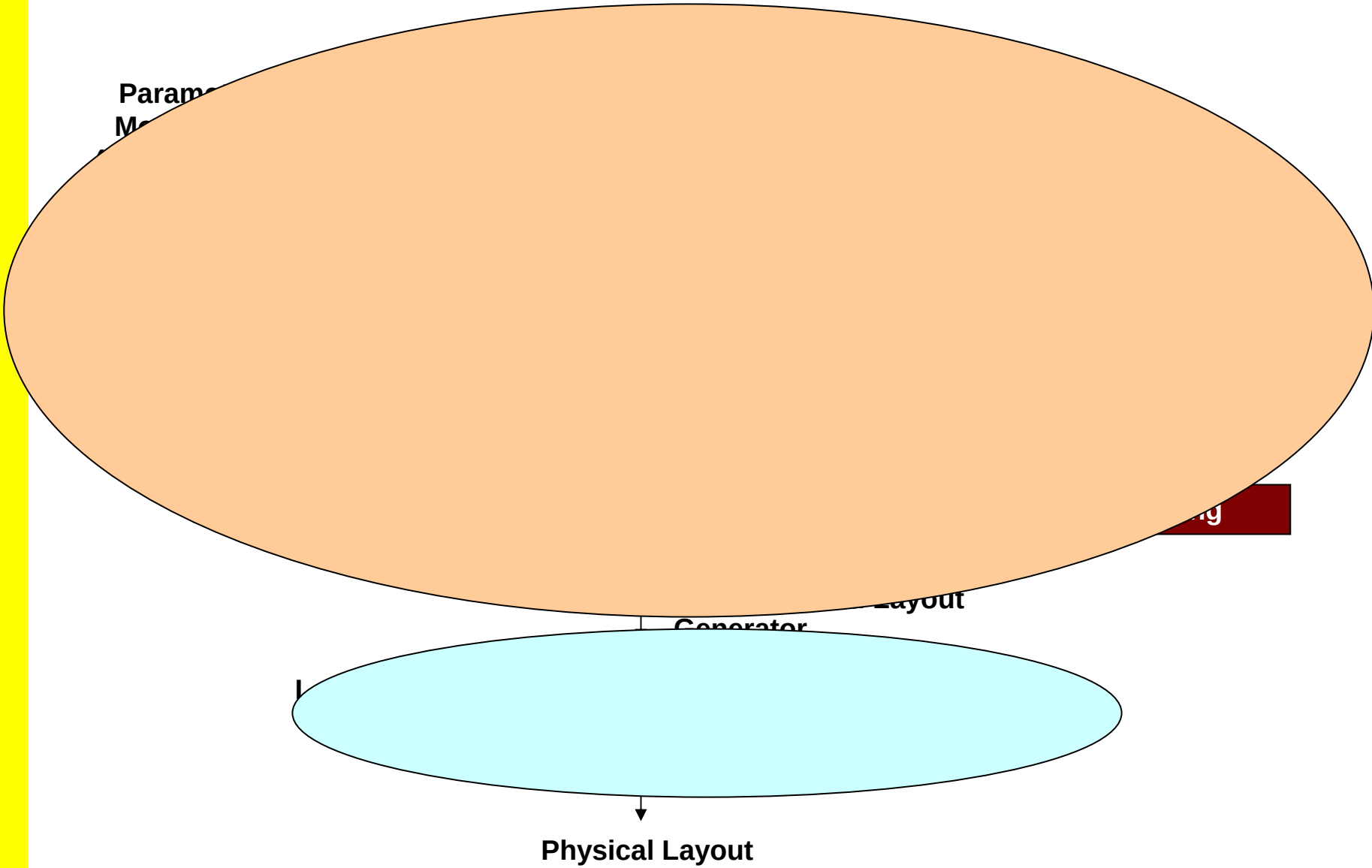
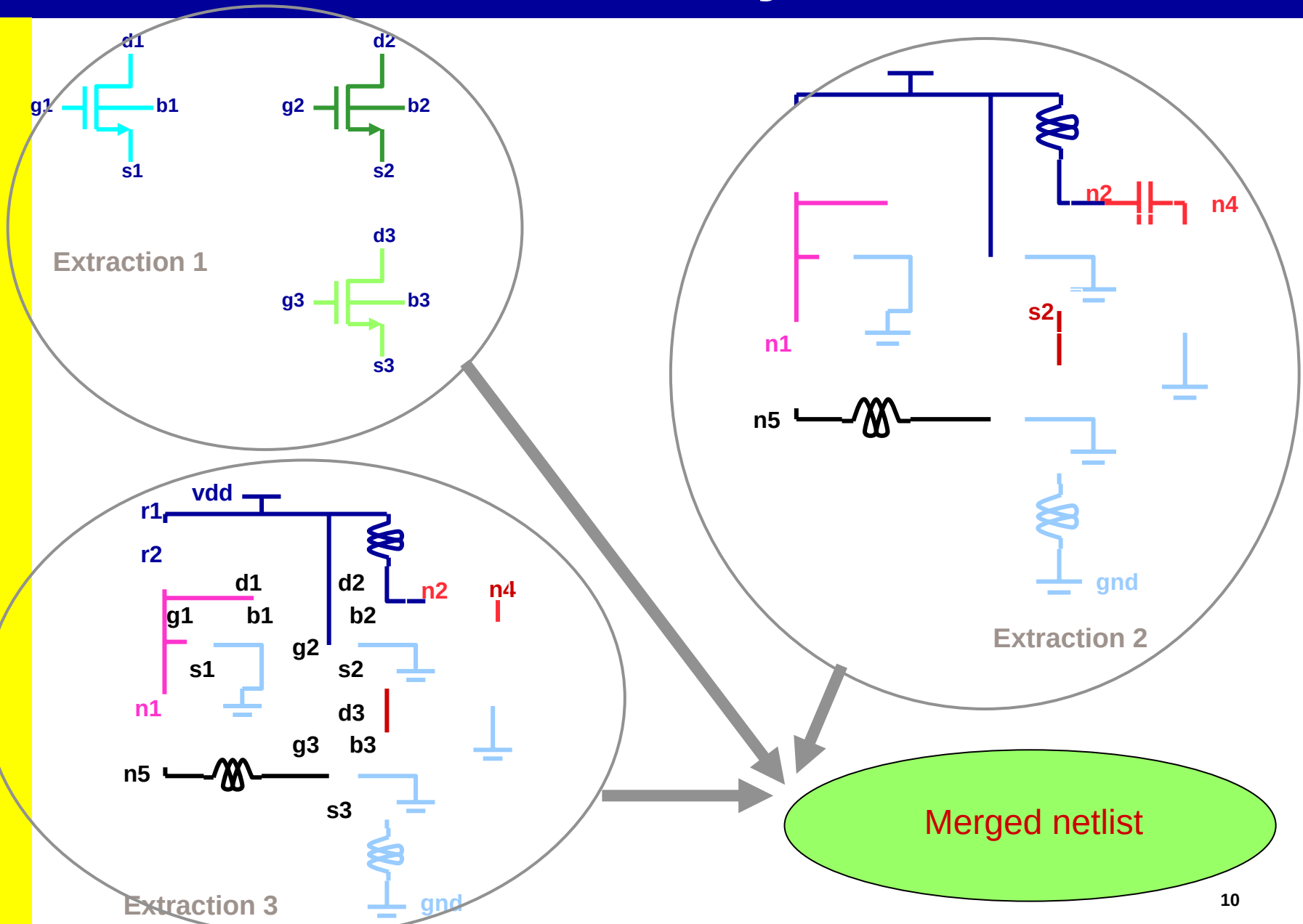


Illustration of 3-Way Extraction



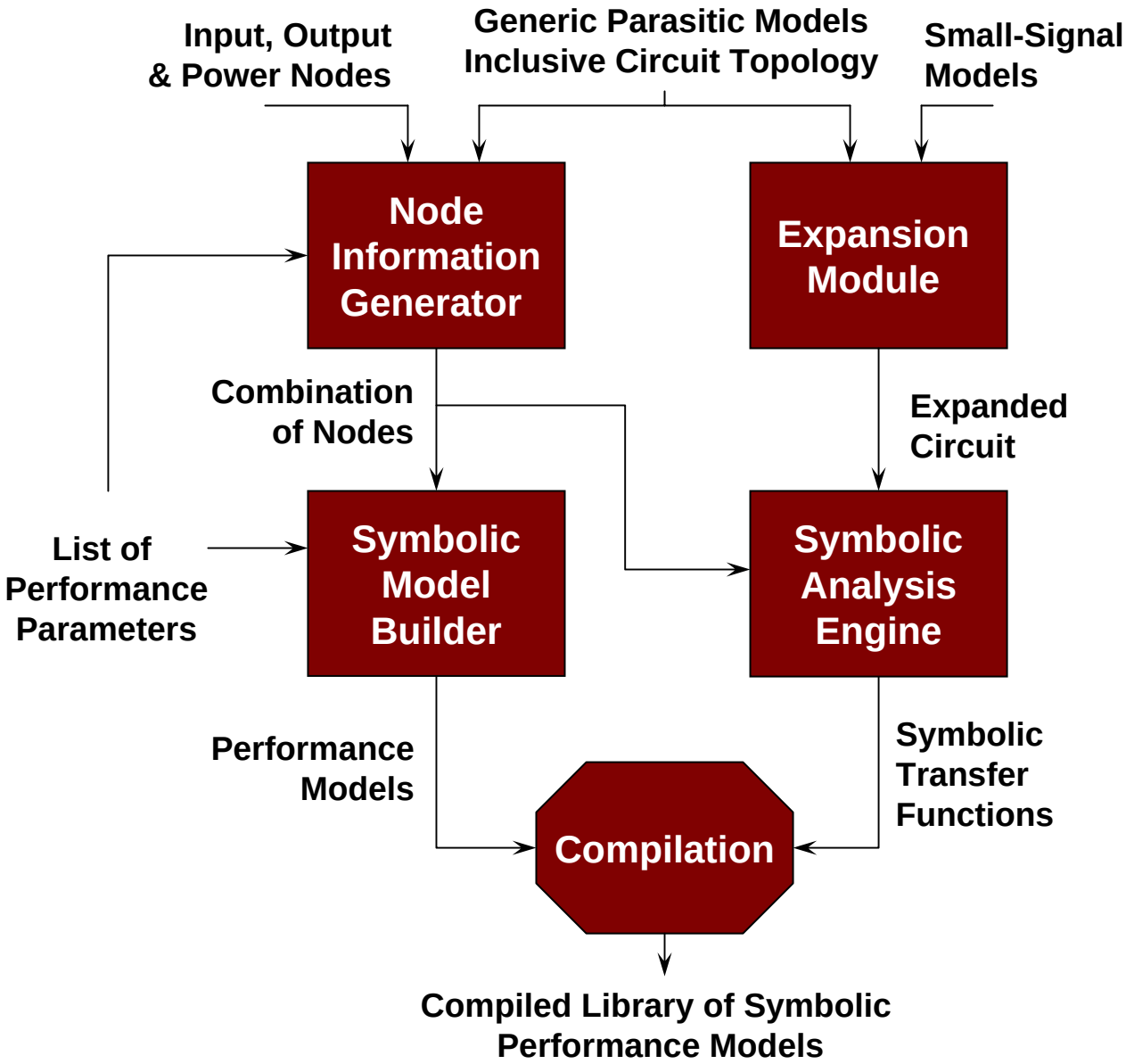
Post-Processing of Extracted Netlist

Netlist Sorting & Compaction

- **Netlist extracted by VPEC**
  - **VRL segments for each net-segment & via.**
  - **Nets jumbled up, no definite order for extracted segments. Need to be arranged according to nets for proper extraction of parasitic values**
  - **Explosion in number of circuit. Creates a problem due to size limitation on symbolic analysis.**
  - **The more the number of segment more difficult it is to create a general inclusion model.**
- **Voltages sources unwanted; hence removed.**
- **Several elements in series merged**
- **Power nodes & terminal nodes of modules are preserved.**
- **Stored as graph for easy generation of extracted netlist and correct extraction of parasitic values for plugging into the SPMs**

Symbolic Performance Modeling

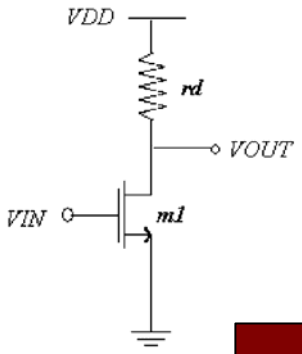
Framework


Input, Output & Power Nodes
Generic Parasitic Models Inclusive Circuit Topology
Small-Signal Models
Node Information Generator
Expansion Module
Combination of Nodes
Expanded Circuit
List of Performance Parameters
Symbolic Model Builder
Symbolic Analysis Engine
Performance Models
Symbolic Transfer Functions
Compilation
Compiled Library of Symbolic Performance Models

Symbolic Analysis

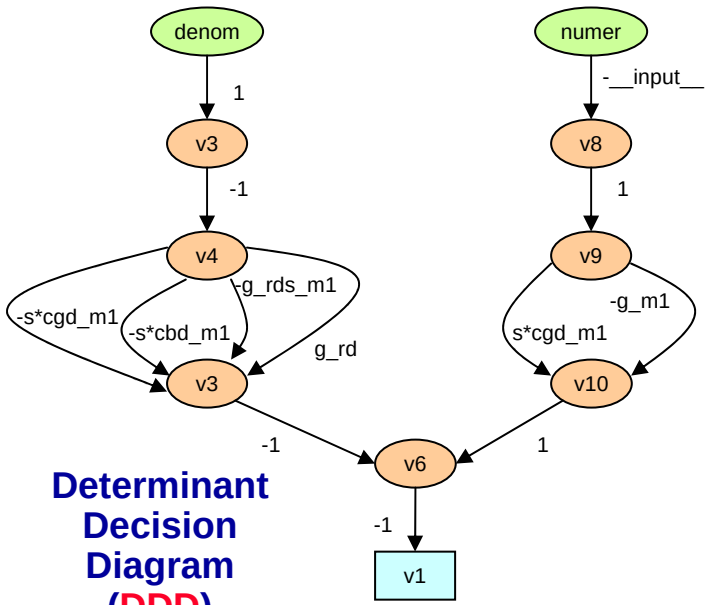
- **Core of SPM generation is Symbolic Analysis**
- **Symbolic Analysis:**
  - **Formal technique to obtain transfer functions.**
  - **Transfer Function in term of:**
    - **symbolic circuit parameters**
    - **independent variables like frequency**
- **Element Coefficient Diagrams (ECDs)**
  - **Represent the transfer functions.**
  - **Fast to evaluate**
  - **Easy to store in the s-polynomial format**
  - **Require low memory**
  - **No approximation**

Element Coefficient Diagrams

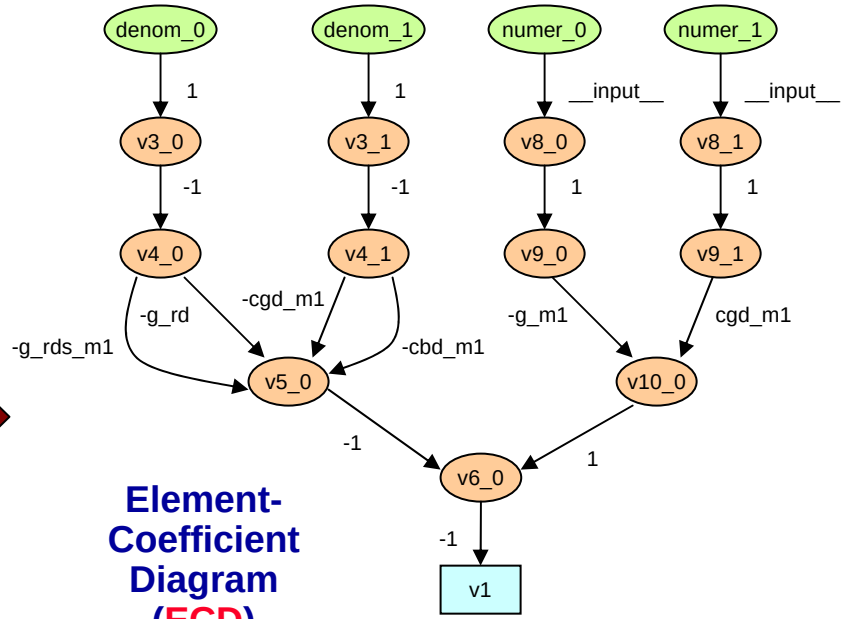



```
Evaluate ECD (SSV)
        v1     = 1;
        v6_0   = -1*v1;
        v10_0  = 1*v6_0;
        v9_0   = -SSV.gm_m1 * v10_0;
        v8_0   = 1*v9_0;
        v9_1   = SSV.cgd_m1 * v10_0;
        v8_1   = 1*v9_1;
        v5_0   = 1*v6_0;
        v4_0   = -SSV.g_rds_m1*v5_0 + -SSV.g_rd *v5_0;
        v3_0   = -1*v4_0;
        v4_1   = -SSV.cgd m1*v5_0 + -SSV.cbd m1*v5_0;
        v3_1   = -1*v4_1;
        numer_0 = - input * v8_0;
        numer_1 = - input * v8_1;
        denom_0 = 1*v3 0;
        denom_1 = 1*v3 1;
end Evaluate ECD
```

Compiled



Determinant Decision Diagram (DDD)



Element-Coefficient Diagram (ECD)

SPM for Noise Figure

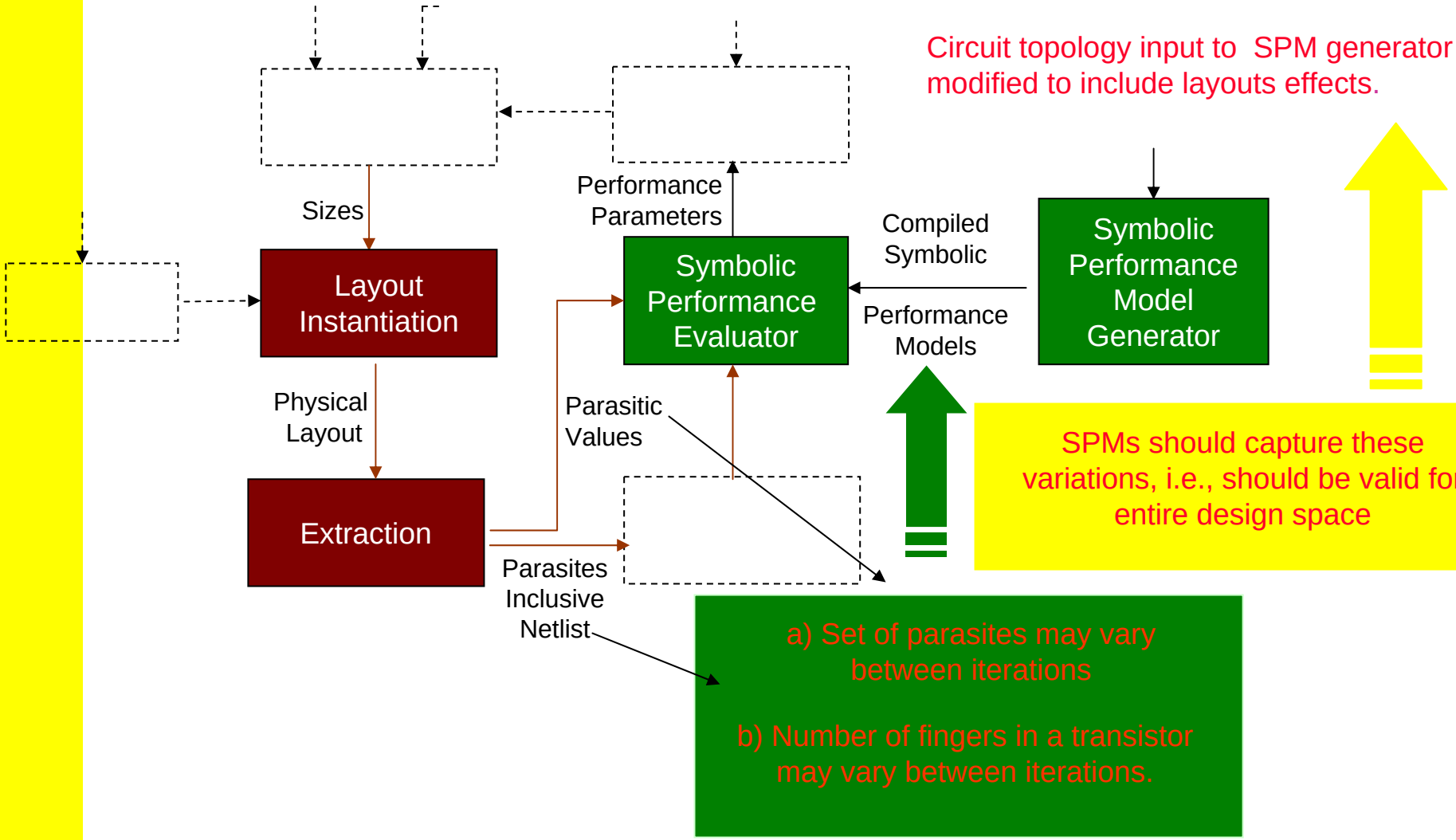
- Similar to technique proposed by Tan et. al.
- Noise Figure = Total Output Noise/ Part of the Output Noise due to the Source resistance
- All noise sources are independent of each other
- Total output noise is the sum of noise at the output from each individual noise source
- Each noise source considered as sinusoidal current generator with rms value equal to rms value of noise current source
- Contribution of each noise source obtained as a transfer function and then combined.

SPM for Distortion Modules

- **Volterra Series based method proposed by Wambacq et. al.**
- **Non-Linear Circuit elements described as a truncated Taylor Series**
- **Circuit is decomposed into a number of circuits, each of which model the behavior at a frequency which is a linear combination of input frequencies.**
- **Each non-linearity is modeled by a non-linear current source and a linearized element**
- **Linear Transfer functions are generated for each circuit and stored as ECDs**
- **SPM is a function which combines the linear transfer functions and non-linearity coeffcients**

Inclusion of Layout Effects

Why Include Layout Effects in SPMs?



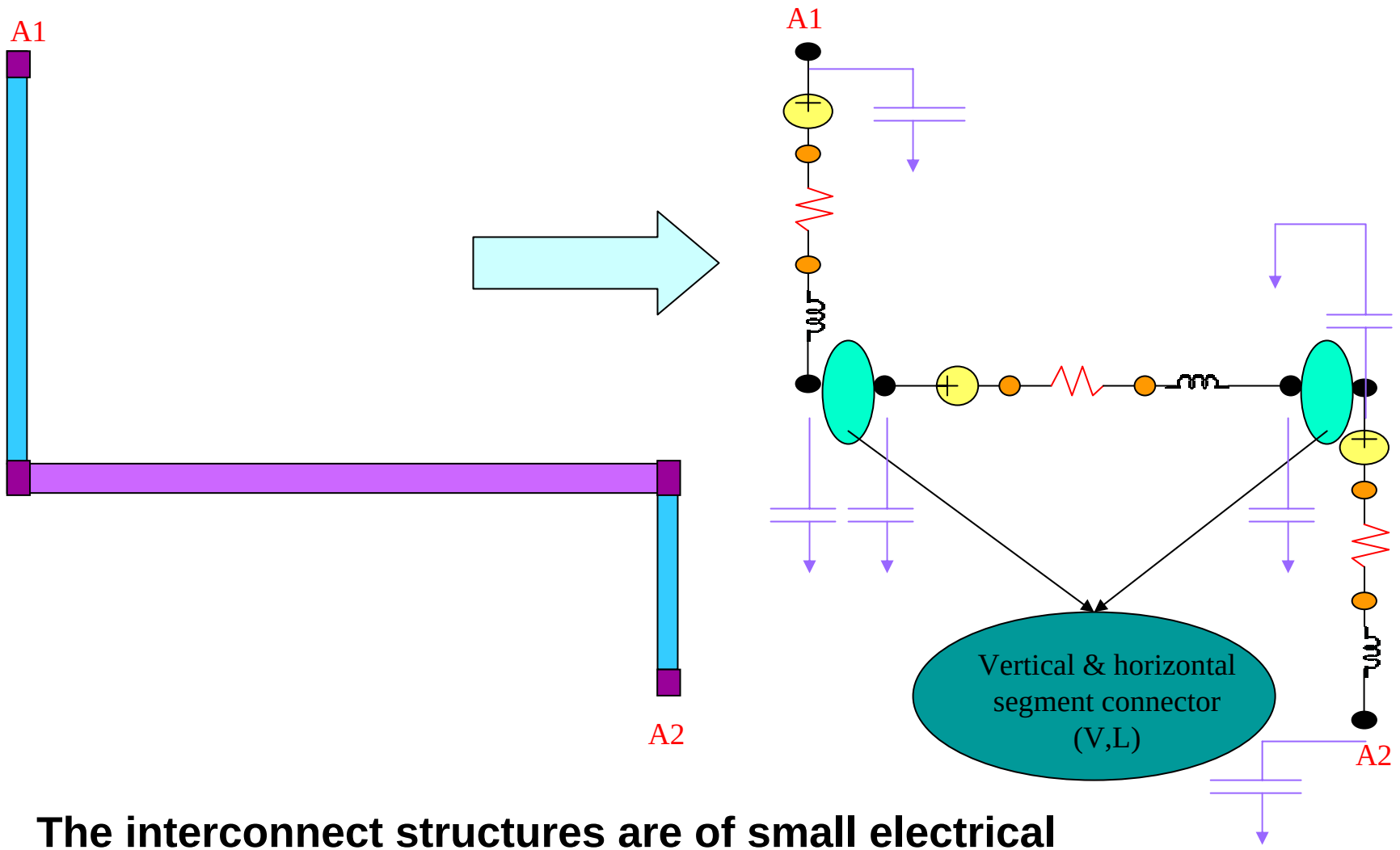
Circuit topology input to SPM generator modified to include layouts effects.

SPMs should capture these variations, i.e., should be valid for entire design space

a) Set of parasites may vary between iterations

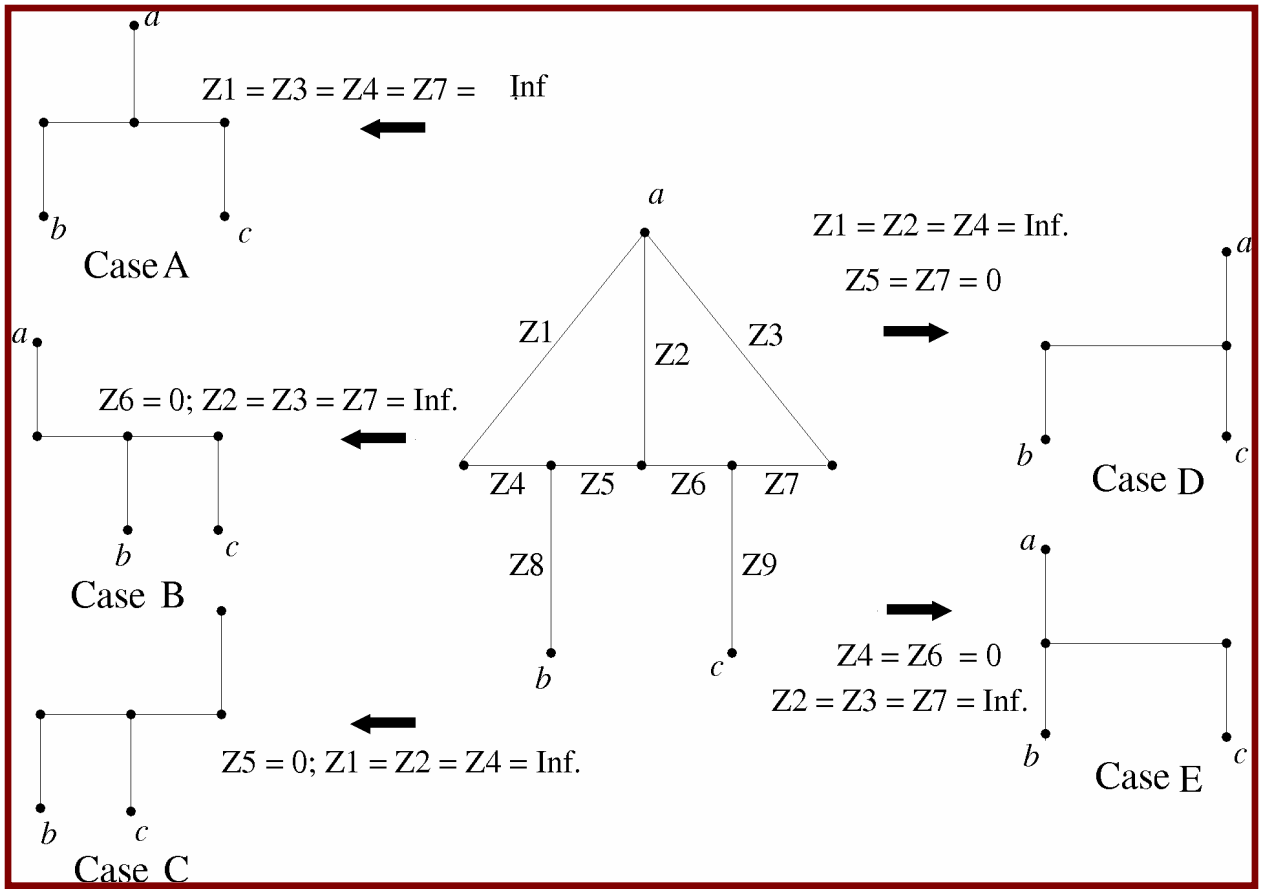
b) Number of fingers in a transistor may vary between iterations.

VPEC: Extraction Technique



- **The interconnect structures are of small electrical length, hence in the frequency range of 1-4 GHz, PEEC model is considered.**

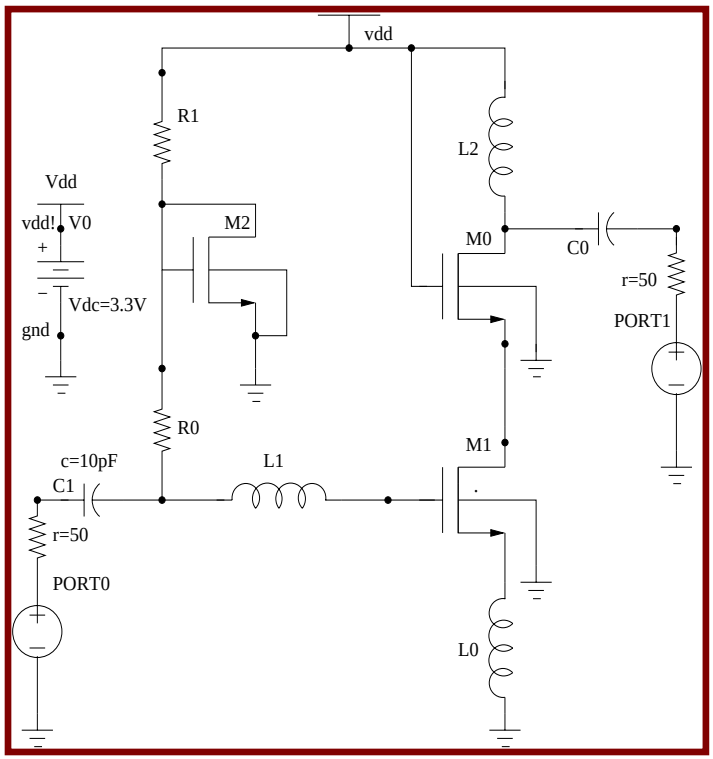
Illustration of Parasitic Inclusion



Five possible cases for a 3-Terminal net and its complete parasitic model in the center, which is included in the circuit topology used to generate the SPMs. Based on good channel routing & complete extraction of PEEC Model

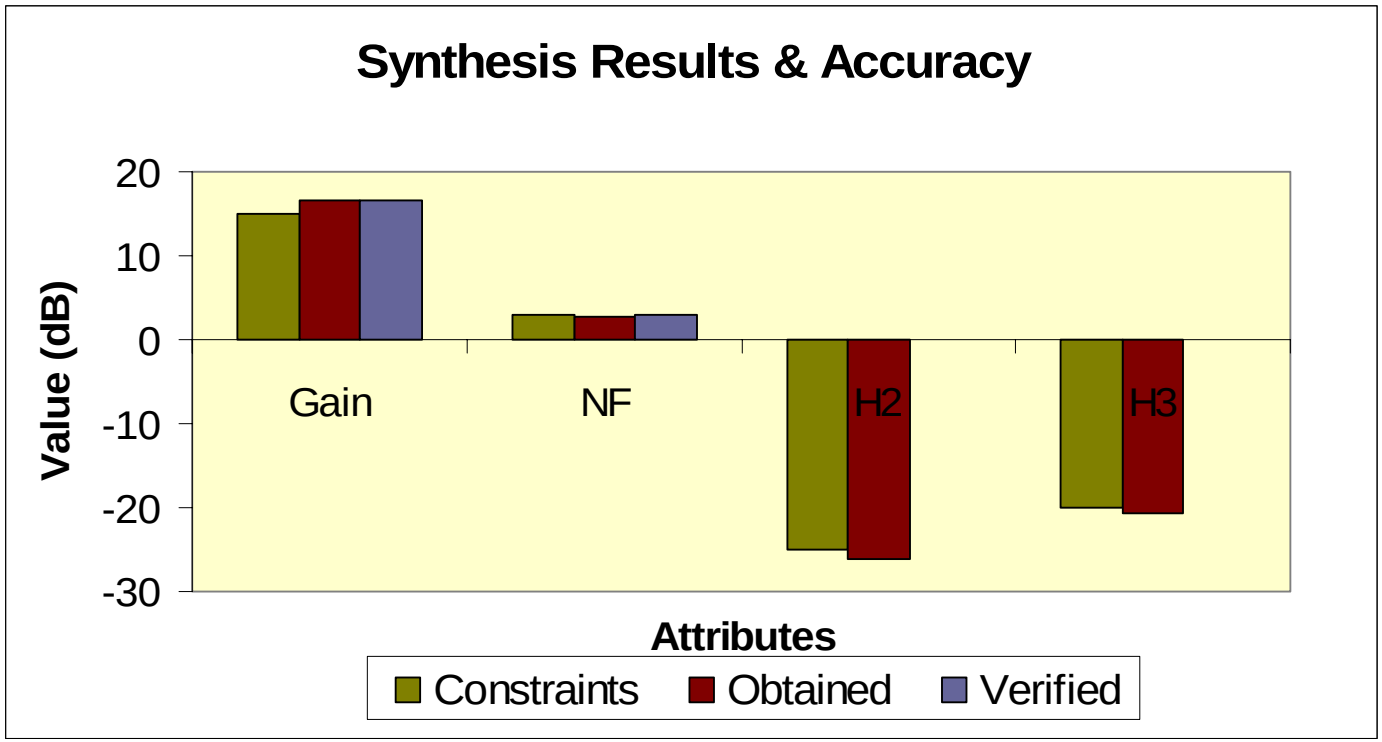
Experimental Results

Benchmark Setup



- **M0.W = M1.W; Enables merging drain of M0 with source of M1; Reduces internal noise of cascode transistor M1 & facilitates input matching.**
- **M0.W = 0.1 * M1.W (M0 forms a current mirror with M1); Minimizes power consumption in bias circuit.**
- **Large input blocking capacitance is off-chip; Fixed at 10pF.**
- **SA-based optimizer explores search space for design variables: M1.W, L0, L1, L2, R0, R1 and C0.**
- **TSMC 0.18μ technology; All simulations run on SunBlade1000 with 2GB RAM.**

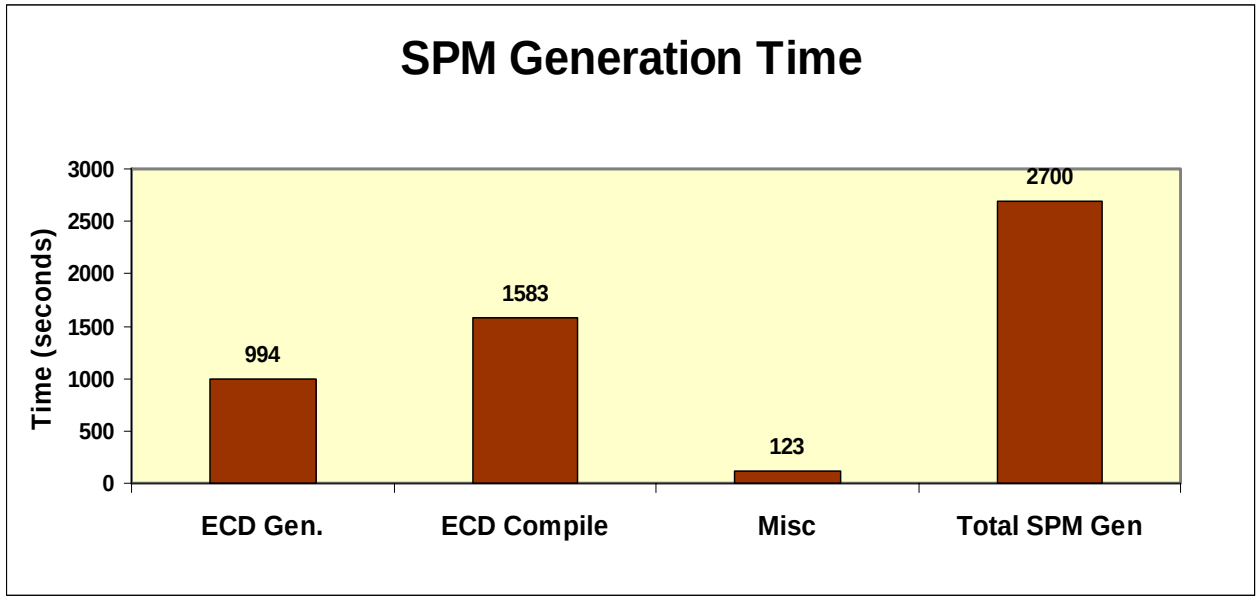
Synthesis Results & Accuracy



Attribute	Constraints	Obtained	Verified	Error
Gain	>15	16.565	16.548	0.10%
NF	>3	2.754	2.9	5.03%
H2	<-25	-26.239	-	-
H3	<-20	-20.782	-	-

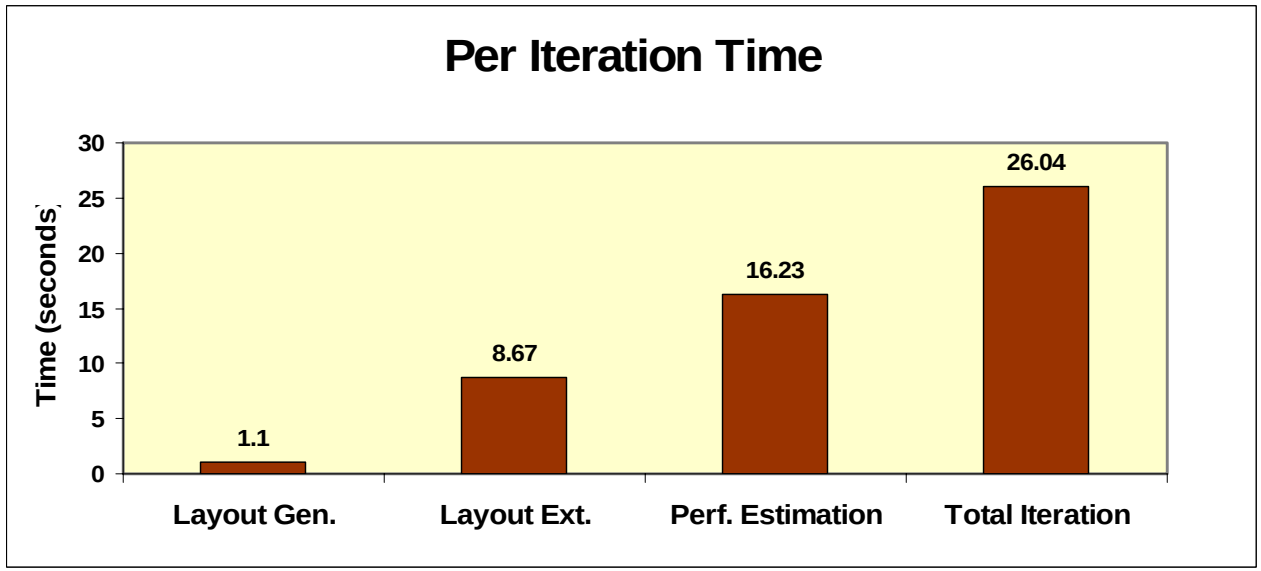
Frequency = 2.1 GHz

Time Results



Total Number of ECDs = 49

A_0= 1
NF = 8
H2 = 9
H3 = 31



Total Synthesis Time
~13 hours

# of Iterations
~1800

Conclusions

Conclusions

- **Contributions**
  - **Use of SPMs in Layout-Inclusive RF LNA Synthesis**
  - **Compilation of ECDs for faster evaluation**
  - **Use of MSL for layout generation and evaluation**
  - **Parasitic Inclusion techniques for high frequency effects**
- **Future Work**
  - **Development of SPMs for Intermodulation**
  - **Model equations for non-linearity coefficients**