A Methodology for Modeling Lateral Parasitic Transistors in Smart Power ICs

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ABSTRACT

Switching of power stages in smart power ICs, which drive an inductive load, turns on parasitic bipolar transistors and injects minority carriers into the substrate, which can affect the functionality of the chip. In order to evaluate protection measures, these parasitic transistors have to be included into a post layout simulation. In this paper, we present a methodology for automatically generating Verilog-A models for these parasites from layout data. As these models have to account for high injection effects and a distributed current flow, the convergence behavior of this models will be worse than that of classical bipolar models. We found a reasonable trade-off between convergence behavior and accuracy of the model.

1. INTRODUCTION

A major challenge in today's chip design is to integrate analog and digital circuitry on one chip. Thereby, parasitic structures arise, which might affect the functionality. One of these parasitic structures, which arise due to the integration of different technologies on one chip, is the lateral parasitic bipolar transistor in smart power ICs ([1]–[3]). The parasite is activated, when negative voltages (down to -1.5 V) occur e.g. in power stages for motor control. This happens even during normal operation and causes the injection of minority carriers into the substrate, leading to minority carrier collection by sensitive n-tubs in I/O and analog cells, which in turn causes potential failures.

The parasitic bipolar transistor is formed by multiple components (Fig. 1). The n-regions of the injecting LDMOS act as an emitter and the substrate acts as a base. Each substrate contact and the backside of the chip form base contacts. N-regions with a positive potential (such as the drain of other LDMOS and n-tubs) act as collectors. The parasitic transistor is characterized by a strongly inhomogeneous current flow and a base width of up to a few hundred μm. More than 90% of the injected current flows through substrate contacts, the backside of the chip and the drain regions of other LDMOS. However, as up to a few hundred milliampere might be injected into the substrate, a current gain of less than 0.001 can still be sufficient to cause failures.

Many protection strategies have been reported (e.g.[4]–[9]), however, post layout simulation including these parasitic effects has only rarely been done. The only known method is the integration of device simulations into the design flow [10],

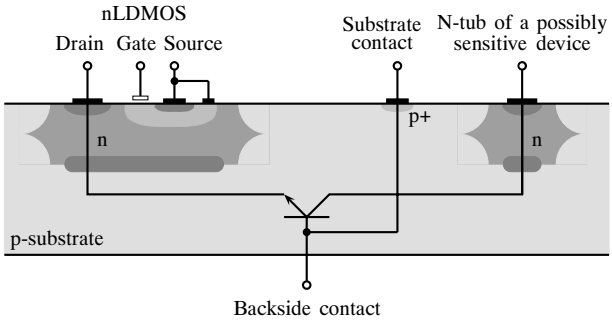

Fig. 1. Simplified cross section of a smart power IC showing the parasitic transistor.

which is very time-consuming. Existing BJT models for circuit simulations are not suited due to the complex structure of the parasitic transistor. Therefore, a new compact model for these parasites is required, whose accuracy is sufficient for indicating inadmissible substrate currents.

In [11], we presented the physical equations which are required to describe the behavior of the parasitic transistor. In this paper, we will first introduce these equations and then describe, how they can be put together in order to build a Verilog-A model for circuit simulations with an acceptable convergence behavior. Furthermore, we will present some convergence aids, which are necessary to run simulations and to speed up the simulation.

2. MODELING THE PARASITIC TRANSISTOR

We assume quasineutrality in the substrate, which is not exactly true as the divergence of the electric field is not zero, especially in the region around the injecting LDMOS and the nearest substrate contacts, where minority carrier densities might exceed the substrate doping.

From quasineutrality it follows, that the hole density p in a p-substrate equals the sum of the electron density n and the substrate doping N_A ($p = n + N_A$). Hence, the gradients of both charge carrier densities are equal ($\nabla n = \nabla p$).

The physical behavior of the parasitic transistor can be described by the following equations (for a p-substrate):

- Current transport equations relate the current densities to electron densities and the electric field. The transport

equations under quasineutral conditions are

$$j_n = q\mu_n(n)V_T\nabla n + q\mu_n(n)nE, \quad (1)$$
$$j_p = -q\mu_p(n)V_T\nabla n + q\mu_p(n)\left(n + N_A\right)E, \quad (2)$$

where q is the electron charge, $\mu_{n,p}$ are the mobilities for electrons and holes, E is the electric field and V_T is the thermal voltage.

- If the minority carrier density reaches or exceeds the substrate doping, the mobilities are reduced due to carrier-carrier scattering. This is modeled according to the Conwell-Weisskopf screening theory [12] by

$$\frac{1}{\mu_{n,p}} = \frac{1}{\mu_{n,p_0}} + \frac{1}{\mu_{CW}} \quad (3)$$

with

$$\mu_{CW} = \frac{1.0410^{21}\frac{1}{cmVs}}{\sqrt{n(n+N_A)}\ln\left(1+7.45210^{13}cm^{-2}(n(n+N_A))^{-\frac{1}{3}}\right)}, \quad (4)$$

where μ_{n,p_0} are the intrinsic electron and hole mobilities respectively.

- The density of the injected electrons n_E at the p-side of the pn junction of the injecting LDMOS and the substrate depends on the corresponding junction voltage V_{PN}. Fletcher boundary conditions (derived from [13]) are applied, which are valid for all injection levels. This yields

$$V_{PN} = V_T \ln\left(\frac{\left(-1+sqrt\left(1+4\frac{n_E^2}{N_D^2}+\frac{4n_EN_A}{N_D^2}\right)\right)N_D^2N_A}{2(n_E+N_A)n_i^2}\right), \quad (5)$$

where N_D is the buried layer doping of the LDMOS and n_i is the intrinsic carrier concentration.

- The electron density n_{SC} at the p-side of the pp+ junction of the substrate contact nearest to the injecting LDMOS depends on the corresponding junction voltage V_{HL}. Due to accumulation at the pp+ junction, the electron density increases and might even exceed the electron density at the injecting LDMOS. This results in

$$V_{HL} = V_T \ln\left(\frac{\left(-1+sqrt\left(1+4\frac{n_{SC}^2}{N_{A+}^2}+\frac{4n_{SC}N_A}{N_{A+}^2}\right)\right)N_{A+}^2}{2n_{SC}N_A}\right), \quad (6)$$

where N_{A+} is the doping of the p+-diffusion.

- pp+ junctions are characterized by the surface recombination velocity S, which relates the electron current density $j_{n_{SC}}$ to the electron density n_{SC} for all injection levels [14]. We find

$$j_{n_{SC}} = qS\left(\frac{n_{SC}\left(n_{SC}+N_A\right)}{N_A} - n_0\right). \quad (7)$$

- At n-tubs at a positive potential (reverse biased pn junctions), the electron density n_C at the p-side of the junction increases due to a finite drift velocity v_D depending on the current density j_{n_C}. Furthermore, the current densities include the generation current density of the space charge region as a lower bound [15] resulting in

$$j_{n_C} = qv_D\left(n_C - n_0\right) + q\frac{w}{\tau_n}n_i, \quad (8)$$

where w is the space charge width, which is assumed to be constant.

- The backside of the chip forms a Schottky-like contact, where the electron current density $j_{n_{BS}}$ is related to the electron density n_{BS} by the thermionic emission velocity v_n as

$$n_{BS} - n_0^{BS} = \frac{j_{n_{BS}}}{qv_n}. \quad (9)$$

n_0^B is the equilibrium electron density at the Schottky contact depending on the barrier height.

- The recombination current in the substrate can be related to the hole currents through substrate contacts as

$$I_{hole,SC_\nu} = \int qRdV, \quad (10)$$

where R is the recombination rate.
Here, only SRH-recombination for electron densities above the substrate doping (11) is considered. Auger-recombination is neglected as it has only a minor influence on the results and seriously degrades the convergence behavior. The general expression for SRH-recombination worsens the convergence behavior as well. We find R to be

$$R = \frac{n}{(\tau_n + \tau_p)}, \quad (11)$$

where $\tau_{n/p}$ are the electron and hole lifetimes.

- Kirchhoffs voltage law is applied to the path including the pn junction of the injecting LDMOS, the high-low junction of the substrate contact nearest to this LDMOS, the voltage drop V_{Bi} in the substrate and the potentials of the corresponding contacts (V_D at the drain of injecting LDMOS and V_{SC} at the nearest substrate contact) as follows

$$-V_{SC} + V_{HL} + V_{Bi} + V_{PN} + V_D = 0. \quad (12)$$

V_{Bi} is calculated by multiplying the distance d between the emitter and the substrate contact diffusion region by an average value for the electric field (13) as

$$V_{Bi} = d \cdot \overline{E}. \quad (13)$$

Two different average values are considered. For low voltages, it is assumed that the electric field decreases with the distance to the diffusion regions ($E(r) \sim \frac{1}{r}$ or $E(r) \sim \frac{1}{r^2}$, depending on the structure and according to Poisson's equation in a neutral base region ($\nabla E = 0$)). For high voltages (above the built-in junction voltage), it is assumed, that the electric field is nearly constant between the two regions due to accumulation at the substrate contact. The increase of the electron density at the substrate contact forces the diffusion current from the emitter to flow as a drift current to the substrate contact, amplifying the electric field between the two regions. The transition from low to high voltages has been modeled depending on V_D and not on the electron densities, which would be necessary in order to detect accumulation.

Fig. 2. Approaching the relevant geometry of an LDMOS by half spheres. The relevant diffusion regions of the LDMOS are treated as a single diffusion region.

Otherwise, the convergence behavior is much worse. Therefore, accumulation is not detected but assumed for certain voltages, which decreases the accuracy of the model for intermediate voltages. Equation (13) is a trade-off between minimizing numerical problems and raising accuracy.

Input to the model are the potentials V_D at the drain of the injecting LDMOS and V_{SC} at the substrate contact nearest to this LDMOS and output are the currents through the LDMOS, the substrate contacts, the backside contact and the n-tubs.

3. APPROACH FOR THE ELECTRON DENSITY

Usually, the electron density is calculated by solving the Shockley equations [13], which build a set of nonlinear, coupled, partial differential equations. As it is not possible to solve these equations analytically in three dimensions, we neglect the influence of the electric field on the electron density distribution and solve the static diffusion equation [13] in spherical coordinates. In order to apply the solution for our problem, we consider the relevant components of the parasitic transistor (LDMOS, substrate contacts, n-tubs) as constantly doped diffusion regions whose geometry is approached by half spheres (Fig. 2).

This allows us to superpose the solution for each sphere, yielding the electron density in the substrate as

$$n\left(x,y,z\right) = \sum_{i=1}^{m} N_i \frac{e^{-\frac{r_i}{\sqrt{D_n \tau_n}}}}{r_i}. \tag{14}$$

N_i are variable coefficients and r_i are the distances to the centers of the half spheres.

After inserting layout and technology data, the exponential terms in (14) reduce to numbers and the electron density and its gradient become

$$n\left(x,y,z\right) = \sum_{i=1}^{m} a_i N_i, \tag{15}$$

$$\nabla n\left(x,y,z\right) = \sum_{i=1}^{m} b_i N_i. \tag{16}$$

where a_i and b_i are layout-dependent coefficients.

There is no such function for the electric field. Therefore, we introduce the variables E_α, which represent the electric field at half spheres. At n-tubs, E_α is set to zero, i.e. electrons reach n-tubs solely by diffusion.

Then, the current densities (1,2) at half sphere α are described by the variables E_α and N_i as

$$j_{n_\alpha} = \sum_{i=1}^{m} c_i N_i + \sum_{i=1}^{m} d_i N_i E_\alpha, \tag{17}$$

$$j_{p_\alpha} = \sum_{i=1}^{m} e_i N_i + \sum_{i=1}^{m} f_i N_i E_\alpha, \tag{18}$$

where c_i, d_i, e_i, f_i are layout-dependent coefficients.

Equations (15, 16, 17, 18) are inserted in (4, 5, 6, 7, 8, 9, 10, 11). Therefore, once the layout data is known, the unknowns of the equation system are N_i, E_α, V_{PN} and V_{HL}. There is one N_i for each half sphere and one E_α for each substrate contact and the backside contact.

Furthermore, we assume a constant electron density at all half spheres belonging to the same diffusion region. For such two half spheres applies the following equalities apply

$$n\left(x_1,y_1,z_1\right) = n\left(x_2,y_2,z_2\right) \tag{19}$$

$$\Rightarrow \sum_{i=1}^{m} g_i N_i = \sum_{i=1}^{m} h_i N_i. \tag{20}$$

The backside of the chip is modeled by half spheres as well.

4. AUTOMATED MODEL GENERATION

At first, all diffusion regions and the backside are transformed into half spheres. The lowest point of each half sphere is a reference point, where the boundary conditions have to be fulfilled and where the current densities are taken as average values for the calculation of the terminal currents. The reference points of half spheres belonging to the backside are on the backside.

Then, the mobility equations are set up for each diffusion region. Equation (3) is set up for all diffusion regions, where a significant mobility reduction can be expected, i.e. for the injecting LDMOS and for all substrate contacts. A constant mobility ($\mu_{n,p} = \mu_{n,p_0}$) is used for all n-tubs.

In the next step, the boundary conditions (5, 6, 7, 8, 9) are set up for only one half sphere of a diffusion region. For the others, a boundary condition in the form of (20) is setup. There are two boundary conditions for the high-low junctions of substrate contacts ((6) and (7)). Equation (7) is used for each substrate contact and (6) only once for the substrate contact nearest to the injecting LDMOS.

The substrate is discretized in order to apply (10). A recombination current is calculated for each volume element (21) and assigned to the nearest substrate contact.

$$I_{rec_i} = \frac{q}{(\tau_n + \tau_p)} \bar{n} \Delta x \Delta y \Delta z. \tag{21}$$

The hole current through a substrate contact equals the sum of the corresponding recombination currents.

$$I_{hole,SC_\nu} = \sum I_{rec_i}. \tag{22}$$

Then, Kirchhoffs voltage law (12) is set up.

The last equations to be set up are the current equations for each terminal. The current density at the reference point of a half sphere is used as an average value and multiplied by the surface area of the half sphere, yielding the current through a half sphere. In order to get the terminal currents, all currents through half spheres belonging to one terminal are summed up

$$I_i = \sum \left(\bar{j_n} + \bar{j_p}\right) A. \tag{23}$$

For n-tubs, only the electron currents are summed up:

$$I_{n-tub_i} = \sum \bar{j_n} A. \tag{24}$$

Finally, this set of equations is reduced by substituting certain variables. In each linear equation (8, 9, 20), the coefficient N_i of the corresponding half sphere is isolated, substituted by this equation in all other equations and the equation is removed from the set of equations. In each equation of the kind of (22), the variable E_α is isolated and removed from the set of equations in the same way.

The mobility equations (3) and the equations for the junction voltages (5, 6) could be eliminated as well, but we keep these equations as they allow the user to see, whether the results are reasonable or not. Furthermore, intermediate variables for the electron densities at the reference points of the half spheres and their gradients are introduced for debugging purposes.

Kirchhoffs voltage law (12) and equations of the form of (7) remain as simultaneous equations. It is always a good idea to have as less simultaneous equations as possible leading to a compact description like simulator built-in transistor models. In our case we reduce the number of simultaneous equations to the minimum we could figure out. Experimental results with more simultaneous equations result in further convergence problems. In order to use the indirect simultaneous formulation using node equations in Verilog-A, (7), a current density equation, and (12), Kirchhoffs's voltage law, have to be adjusted to properly reflect the tolerance group and accuracy of currents. Equation (12) is scaled by a factor of 10^{-5} and (7) by 10^{-3}. Then, both equations are written as

$$10^{-3} j_{n_{SC}} - 10^{-3} qS \left(\frac{n_{SC}\left(n_{SC} + N_A\right)}{N_A} - n_0 \right) = 0, \tag{25}$$

$$-10^{-5} V_{SC} + 10^{-5} V_{HL} + 10^{-5} V_{Bi} + 10^{-5} V_{PN} + 10^{-5} V_D = 0. \tag{26}$$

Except for the terminal current equations, the size of the model depends only on the number of substrate contacts and not on the number of n-tubs or on the number of half spheres, in which the diffusion regions are partitioned.

The behavioral model is implemented in Verilog-A and simulated with Spectre® [16]. Due to the intermediate variables it consists mostly of procedural and a few simultaneous equations. It is directly useable in circuit simulations, because all contacts are electrical terminals of the module. The use of a simulator/language with proper support of procedural equations is mandatory due to better convergence and shorter runtimes. Hence, Verilog-A, which is more directed to procedural equations – simultaneous equations have to be indirectly formulated by using node equations – is well suited.

Listing 1 Approximation for $-1 + sqrt(1 + x)$

```
analog function real special_sqrt;
  input x;
  real  x;
  if (x >= 1e-3)
    special_sqrt = -1+sqrt(1+x);
  else
    special_sqrt = 0.5*x-0.12493754*pow(x,2);
endfunction
```

Listing 2 Extension of $sqrt(x)$, $ln(x)$ and $pow(x, -0.33)$

```
    analog function real ext_sqrt;
      input x;
      real  x;
      if (x > 0)
        extsqrt = sqrt(x);
      else
        ext_sqrt = 0;
    endfunction
    analog function real ext_ln;
      input x;
      real  x;
      if (x >= 1)
        ext_ln = ln(x);
      else
        ext_ln = x-1;
    endfunction
    analog function real ext_pow;
      input x;
      real  x;
      if (x >1e-3)
        ext_pow = pow(x,-0.33);
      else
        ext_pow = 10;
    endfunction
```

5. CONVERGENCE AIDS

In order to improve the convergence behavior of the generated model, a few aids have been implemented. One problem occurs in the equations (5) and (6), as they contain a sum of numbers of different orders of magnitude. The core of the problem is the expression $ln\left(k\left(-1+\sqrt{1+x}\right)\right)$, where x ranges from 0 to about 1. If x is too small, the expression $1+x$ yields 1 and the expression $-1+\sqrt{1+x}$ yields 0 and the total expression yields a singularity. Therefore, we approximate the expression $-1+\sqrt{1+x}$ by a taylor series for very small x. The term $\sqrt{1+x}$ can be developed, resulting in $1+\frac{x}{2}-\frac{x^2}{8}+\ldots$. In order to gain a smooth transition from the taylor series to the original function, we adjust the second coefficient. Therefore, we approximate $-1+\sqrt{1+x}$ by $\frac{x}{2}-\frac{x^2}{8.004}$ (see Listing 1).

Another problem during the iterations is that the argument of the square root and the logarithm becomes negative. Therefore, the domain is extended to all real numbers (see Fig. 3, 4, 5 and Listing 2).

The extended square root function is the original square root function for positive numbers and zero for negative numbers.

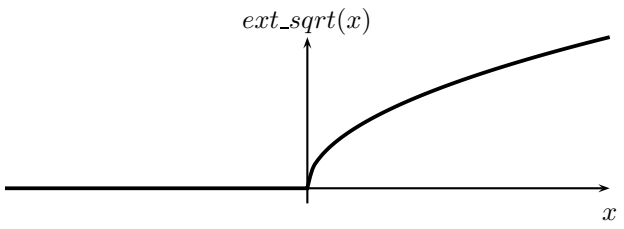

Fig. 3. Extended square root function

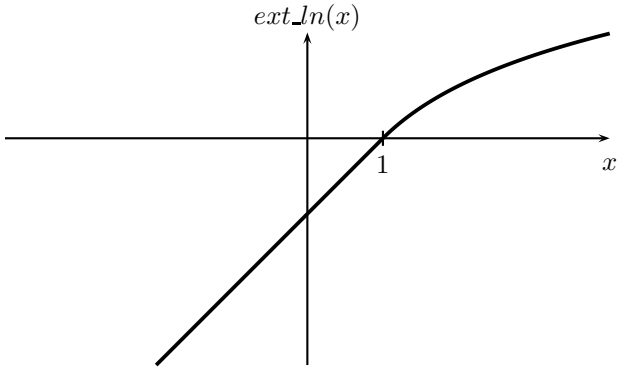

Fig. 4. Extended logarithm function

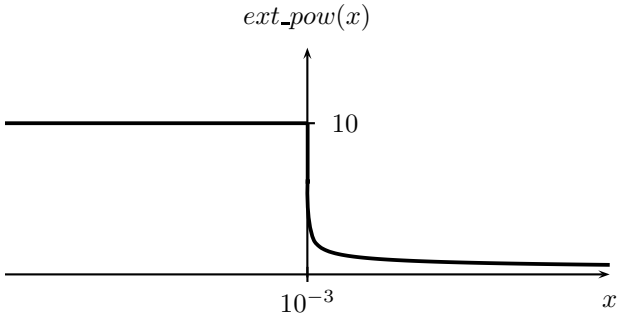

Fig. 5. Extended pow(x,-0.33) function

Simulations have shown, that a more elegant extension with a smooth derivative slows down the simulation time.

The logarithm function is extended by a linear function for values below 1, such that the derivative of the extended function is smooth.

For (4), the power function $x^{-\frac{1}{3}}$ has to be extended. The extended function returns 10 for values below 10^{-3} and $x^{-\frac{1}{3}}$ otherwise.

6. RESULTS

To show the feasibility of our approach we have generated a model and simulated it for the structure shown in Fig. 6. We compare circuit simulation results employing the new model with device simulation results. In order to use device simulations, we applied the topology reduction method as presented in [2].

The structure consists of one large $500\,\mu m\,x\,500\,\mu m$ n+ diffusion L_2 representing the drain regions of an nLDMOS, whose

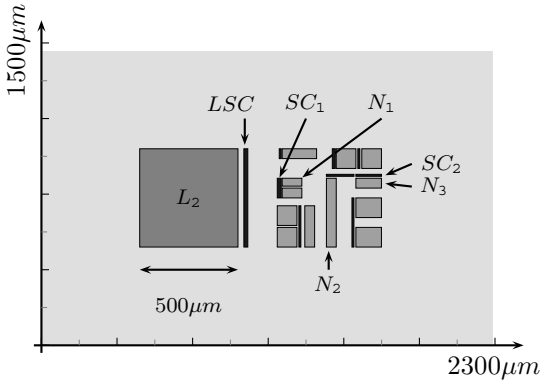

Fig. 6. Modeled and simulated structure

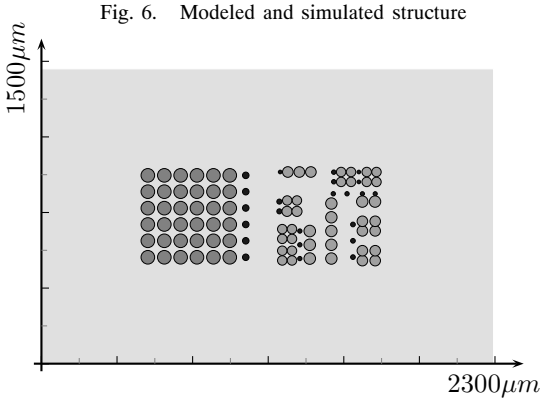

Fig. 7. Top view of the modeled structure.

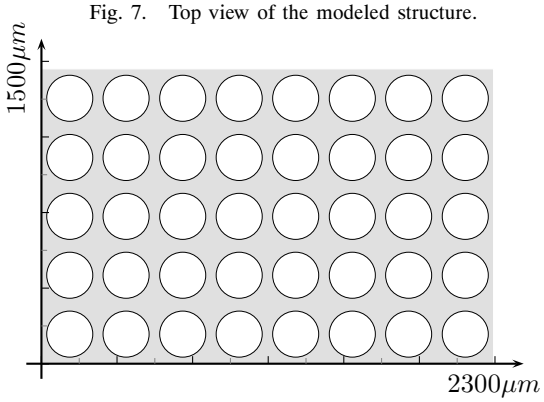

Fig. 8. Backside of the modeled structure.

voltage drops down to -1.5 V. The 9 dark gray rectangles are grounded p+ diffusion regions acting as substrate contacts and the 12 gray rectangles are n-tubs at 5 V. The substrate doping is $N_A = 1e16cm^{-3}$ and the substrate thickness is 375 μm.

Fig. 7 and 8 shows the transformation of the diffusion regions into half spheres. The large n+ diffusion is transformed into 6x6 half spheres and the backside into 8x5 half spheres.

The model consists of about 90 procedural and 10 simultaneous equations. The average time required for the dc analysis is about 1.1 s and the average CPU time is about 30 s on a Sun-Fire-480R with 1.2 GHz. In contrast to the circuit simulation, the device simulation runs about 3 weeks ($\sim$ 220 000 grid points). The results for some selected currents are shown in Fig. 9 and Fig. 10. They are in good agreement with device

simulation results. The accuracy of the modeled n-tub currents is within a factor of 2.5, which is sufficient to detect inadmissible parasitic currents. The substrate contact current I_{SC_2} shows a larger error. This is due the simplifications in (11), but does not affect the accuracy of the n-tub currents. In (11), high electron densities have been assumed. This is not the case for substrate contact SC_2, which is more than 600 μm away from the injecting LDMOS. This simplification is justified since substrate contacts, where the electron densities are below the substrate doping, do not significantly affect the electron propagation. Therefore, n-tub currents are also sufficiently modeled in far distant regions.

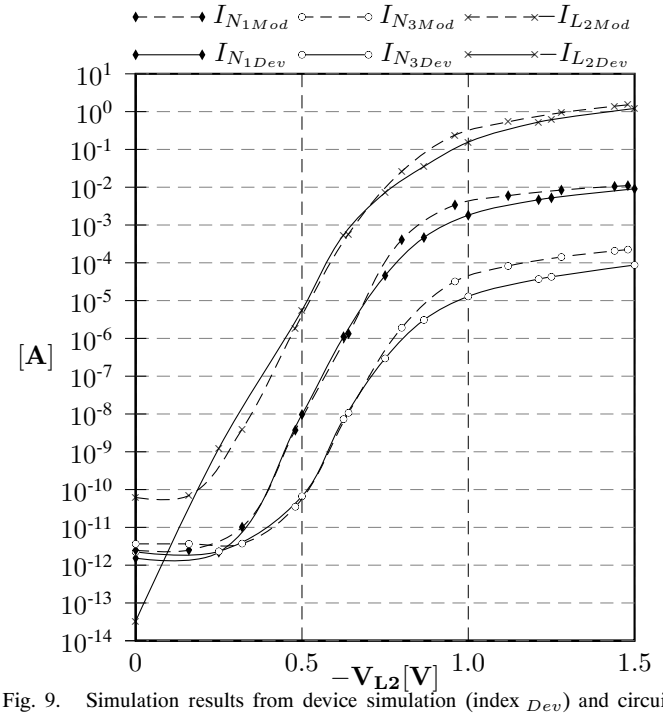

Fig. 9. Simulation results from device simulation (index $_{Dev}$) and circuit simulation employing the new model (index $_{Mod}$).

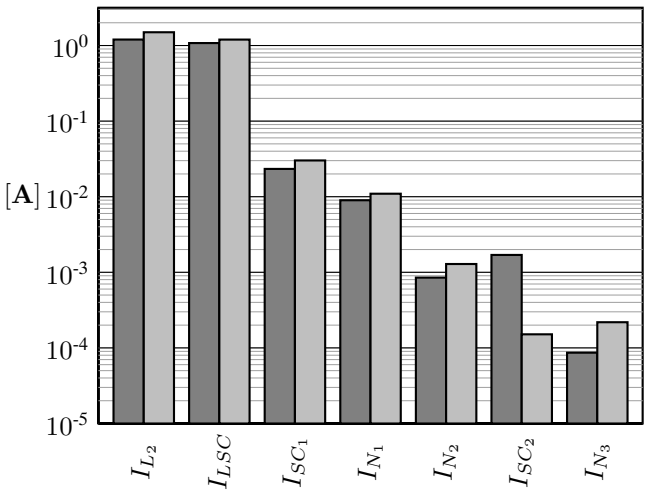

Fig. 10. Further simulation results of the structure in Fig. 6 for $V_{L_2} = -1.5V$ showing selected currents from device simulation (gray bars) and circuit simulation (lightgray bars).

7. CONCLUSIONS

We have presented a methodology for automatically generating models for parasitic transistors in smart power ICs for circuit simulation. We made a compromise between minimizing numerical problems and raising the accuracy of the model. The simulation time is sufficiently short and the accuracy of the model is sufficient to indicate inadmissible substrate currents. The accuracy decreases if there are too few substrate contacts near the injecting LDMOS as the impact of the electric field on the electron density distribution is neglected. In future work, we will extend our model for p++ substrates with a p- epitaxy and for active protection measures, where n-tubs are shorted with p+ diffusions.

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