Processor Architecture Laboratory
Laboratoire d'Architecture des Processeurs

School of Computer and Communication Sciences

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Reduced Order Models of Integrated RF Spiral Inductors with Geometrical and Technological Automatic Parameterization

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Motivation

- Advancement in Wireless Communication Industry:
  - Smaller, Cheaper transceivers in Gigahertz Range.
  - On-Chip Inductive elements address both these requirements.

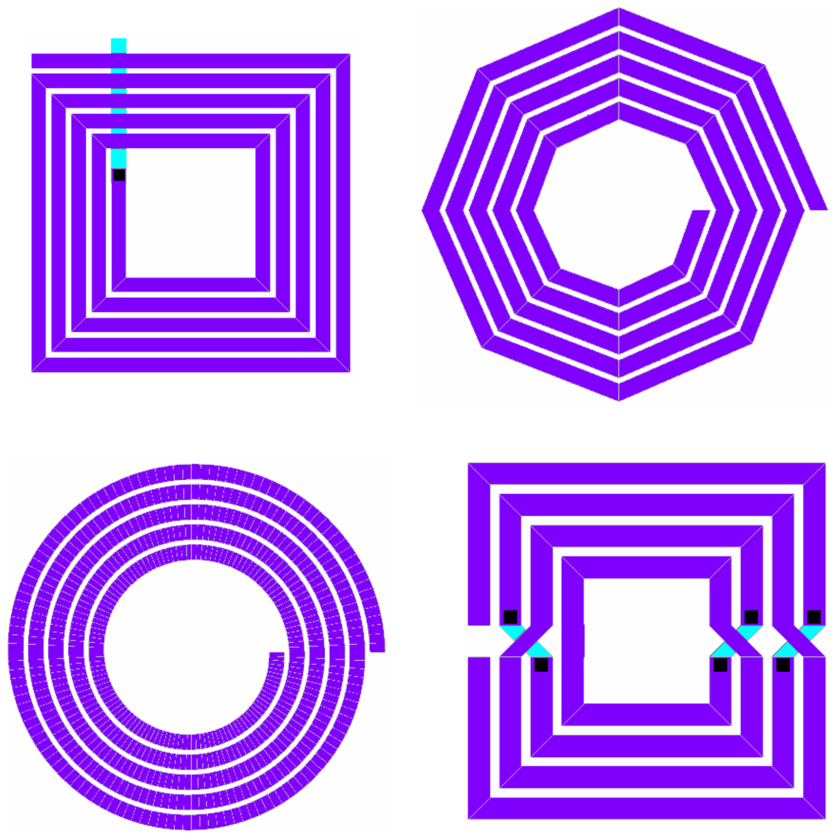
- Accurate tools for predicting and optimizing the characteristics of on-chip Inductive elements.

Spiral RF Inductors

- Inductance, L.
- Quality of Inductor, Q.

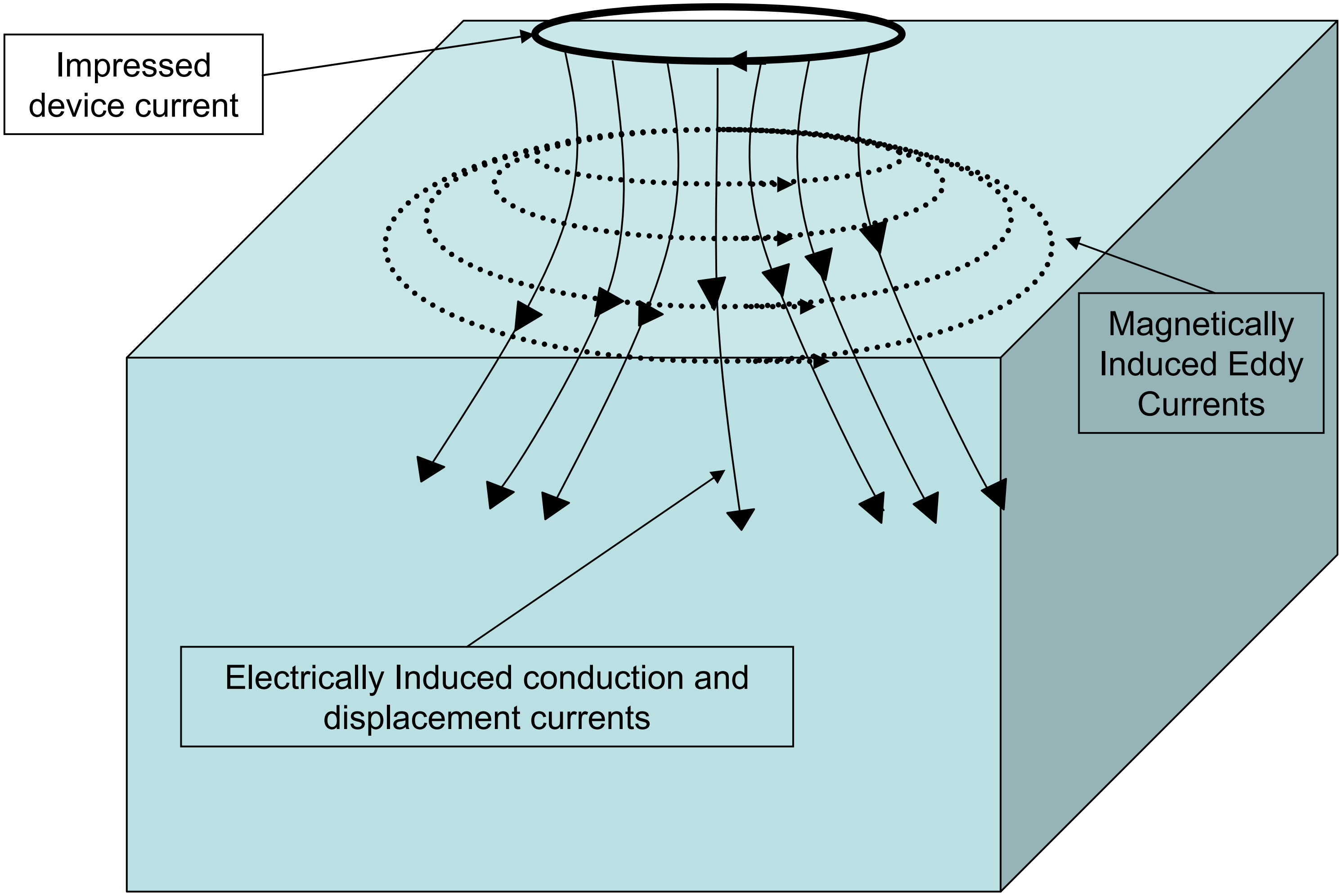
$$Q \propto \frac{E_{stored}}{E_{dissipated}}$$

- Energy Dissipation
  - Displacement Current
  - Eddy Current



A Square Spiral Inductor

Parasitic Losses



Typical parasitic Losses in Spiral Inductors

Timeline

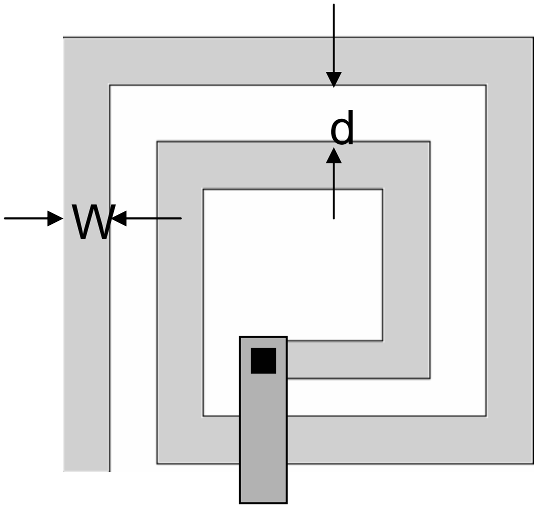
- Ruehli et al, 1974
  - Concept of PEEC.
- Pettenpaul et al, 1988
  - Model each spiral segment individually.
- Niknejad , PhD Dissertation 2000.
  - Model the Substrate & Eddy Current losses.
  - Based on full simulation of Spiral using PEEC.
- Daniel et al., 2003 proposed geometrical parameterization technique for Spiral inductors.
  - Can’t model the substrate losses.

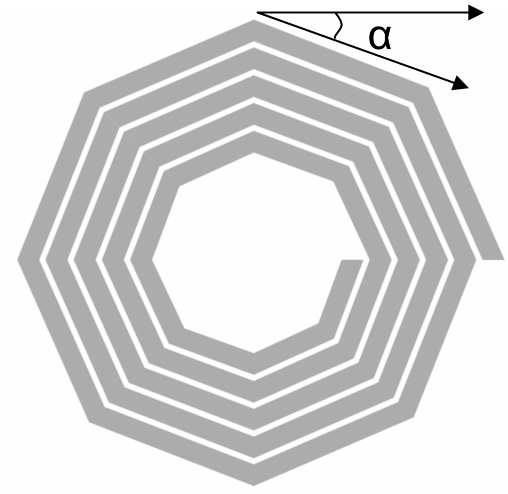
Contribution

- In this paper : Substrate Aware Geometrical Parameterization for Spiral Inductors.
  - Model Substrate Losses
  - Parameterized
  - More accurate
  - Extendable

Parameterization

- Design Parameters
  - ✓ Width of Wire, w.
  - ✓ Separation between turns, d.
  - ✓ Frequency of operation.
  - ❑ Height of Inductor from substrate.
  - ❑ Number of turns.
  - ❑ Number of sides, or angle of turn, α.





Outline

- Theoretical Background
  - Volume Integral Equations
  - PEEC Technique
- Substrate Modeling
- Parameterization & Model Reduction
- Results
- Conclusions & Future Work

Volume Integral Equations

- Current-Voltage relation

$$\frac{J(r)}{\sigma} + j\omega\frac{\mu}{4\pi}\int_V \frac{J(r')}{|r-r'|}dr' = -\nabla\phi,$$

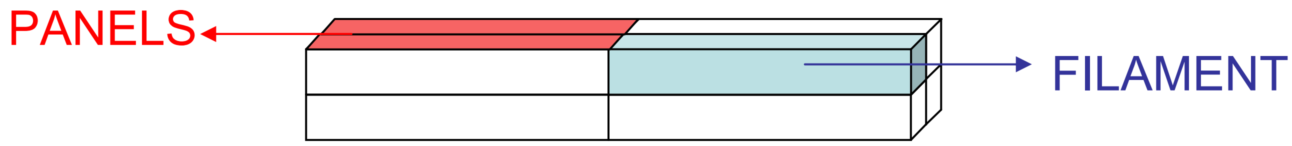
- Charge-Voltage relation

$$\frac{1}{4\pi\varepsilon}\int_S \frac{\rho(r')}{|r-r'|}dr' = \phi(r'),$$

- Charge and current conservation

$$\hat{n}\cdot J(r) = j\omega\rho(r) \qquad \nabla\cdot J(r) = 0$$

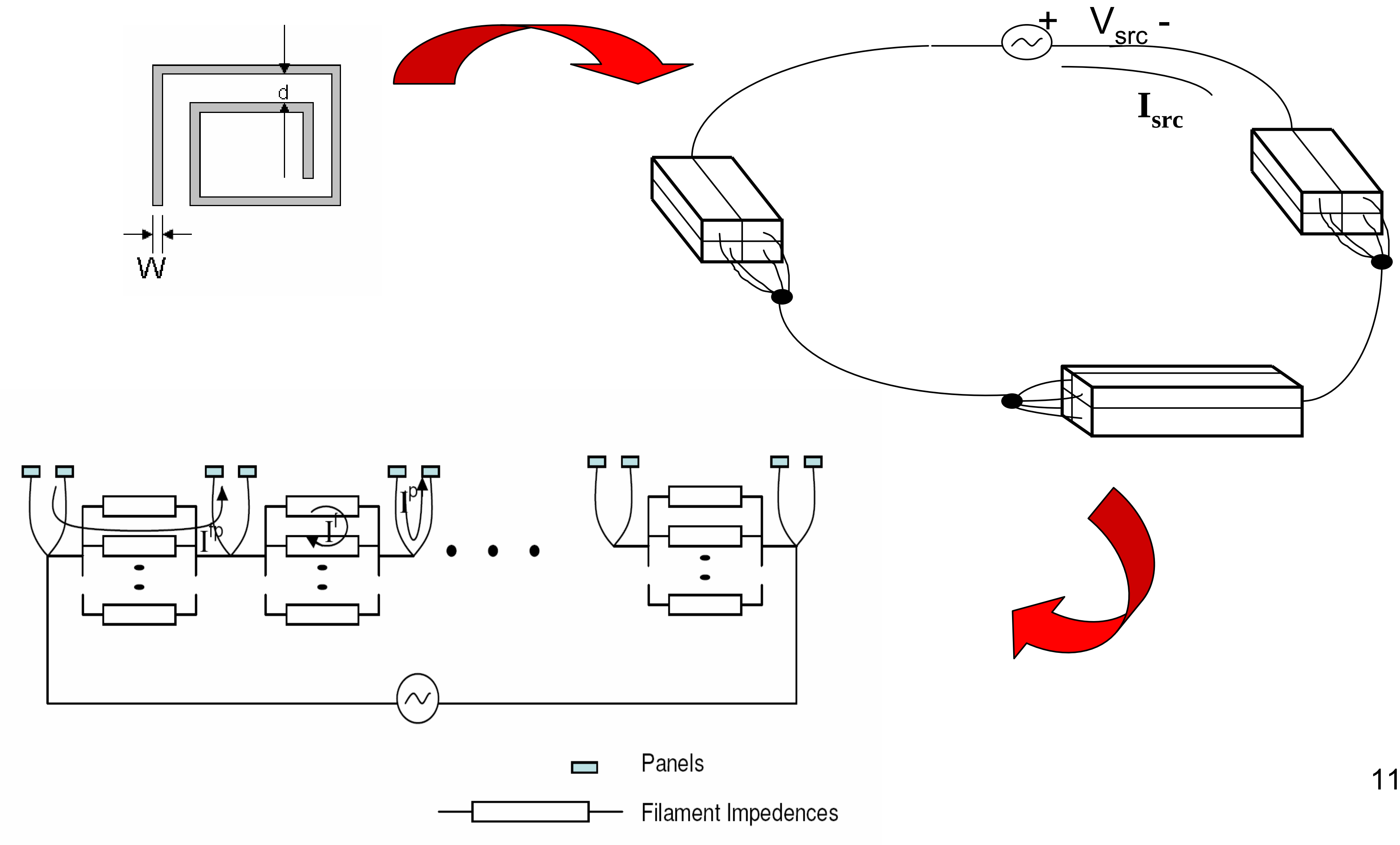
PEEC Technique [Ruehli 74]



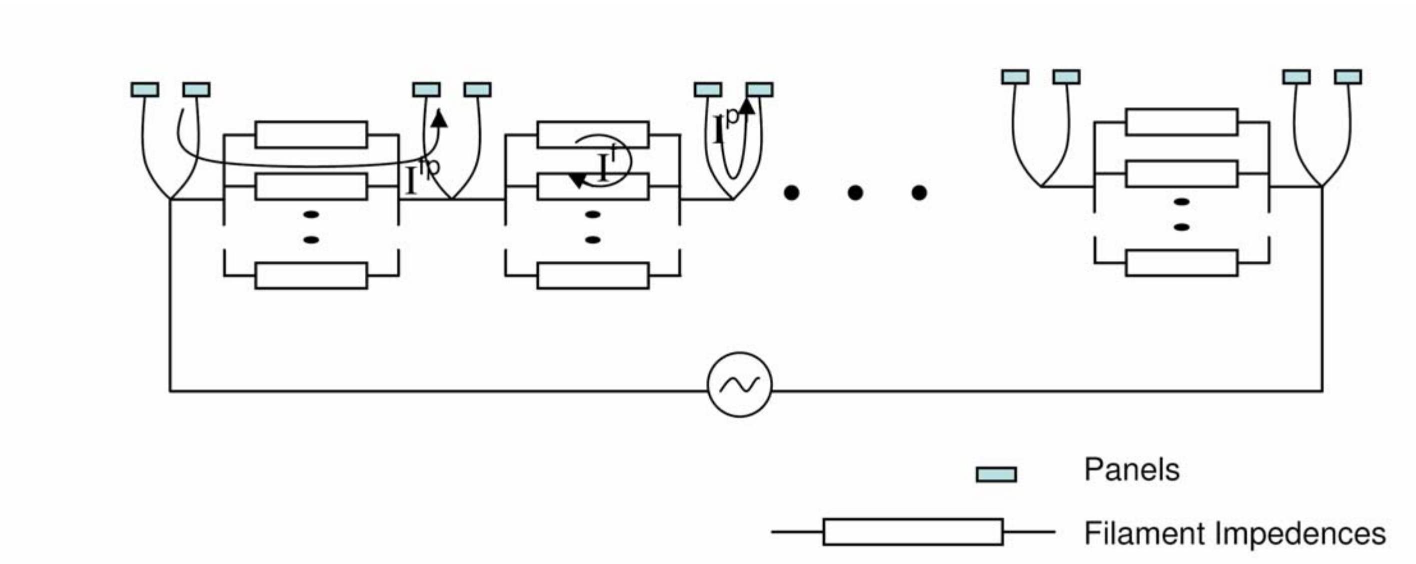
Discretization of the Inductor

- Discretization
  - Meshed into 3D Filaments and 2D Panels.
  - Filaments capture the constant current density.
  - Panels capture the constant charge density on surface.
- Non-uniform discretization
  - Capture skin effects.
  - Boundary effects.

PEEC Construction



Modeling PEEC Circuit



$$s\begin{bmatrix} M_f L_f M_f^T & 0 \\ 0 & P^{-1} \end{bmatrix}\begin{bmatrix} I_m \\ \phi \end{bmatrix} = -\begin{bmatrix} M_f R_f M_f^T & M_p \\ -M_p^T & 0 \end{bmatrix}\begin{bmatrix} I_m \\ \phi \end{bmatrix} + \begin{bmatrix} V_{m,s} \\ 0 \end{bmatrix}$$

$$sLx = -Rx + BV_{src}$$

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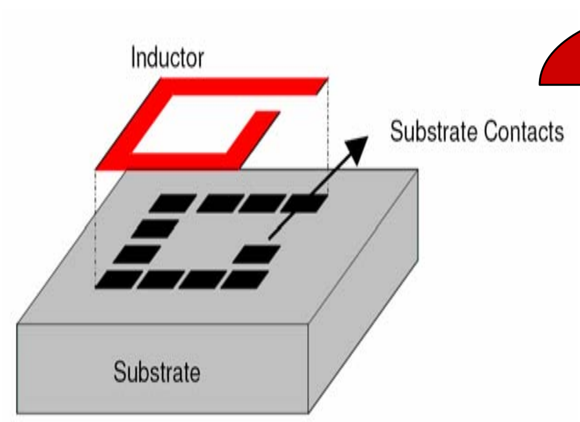
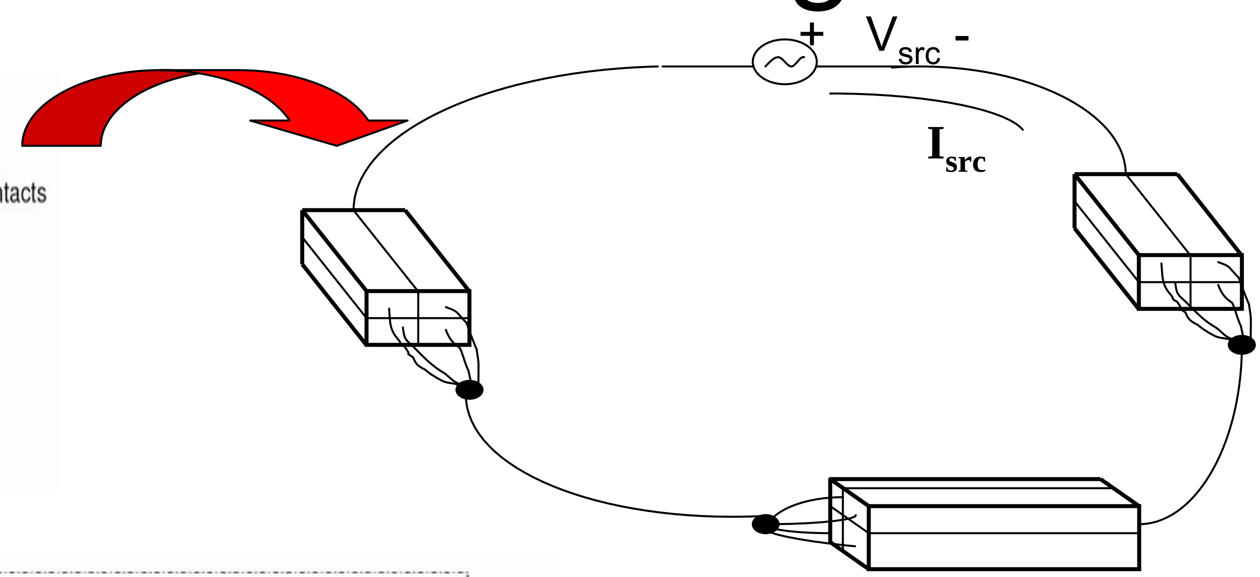
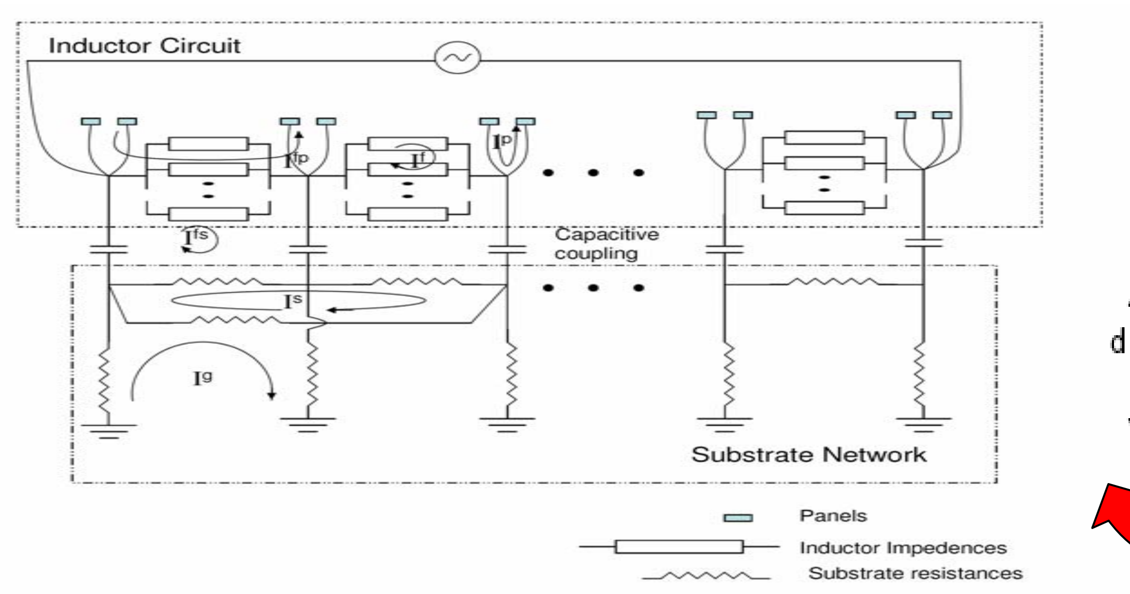
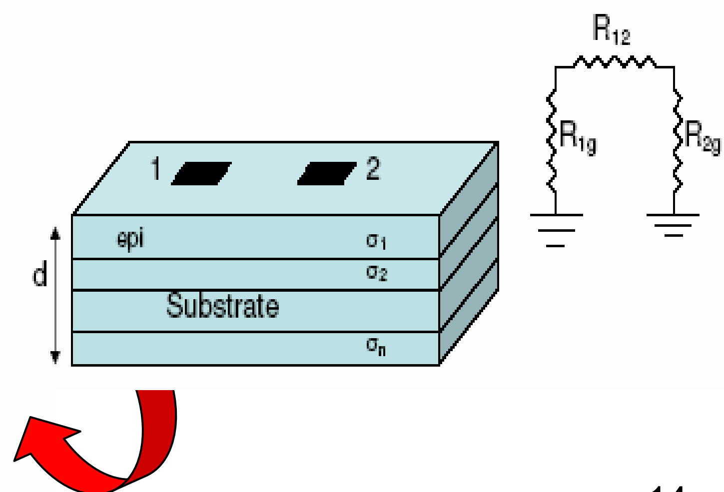
Substrate Modeling

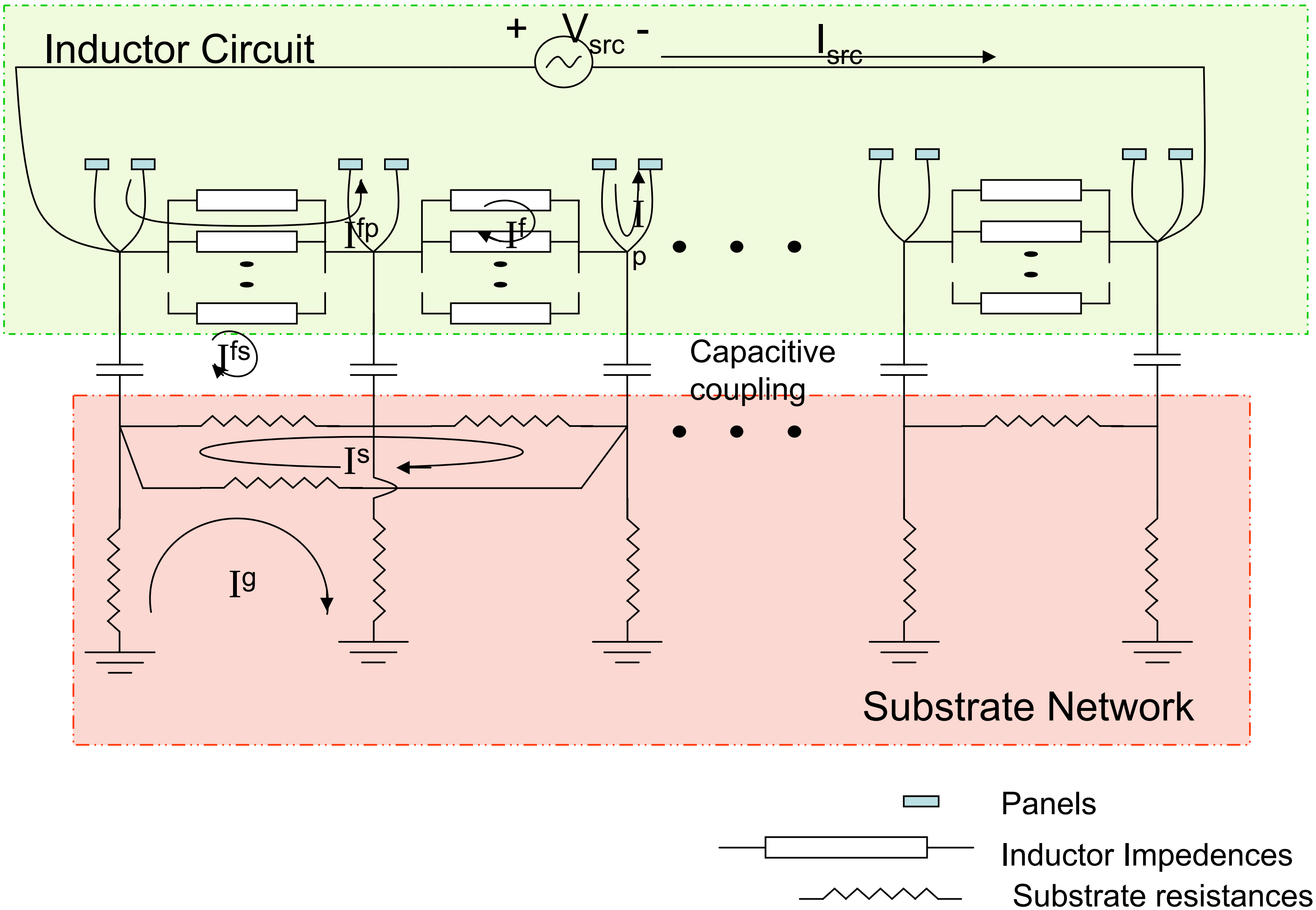








Substrate Modeling



Substrate Modelling

Green Function based FFT technique.

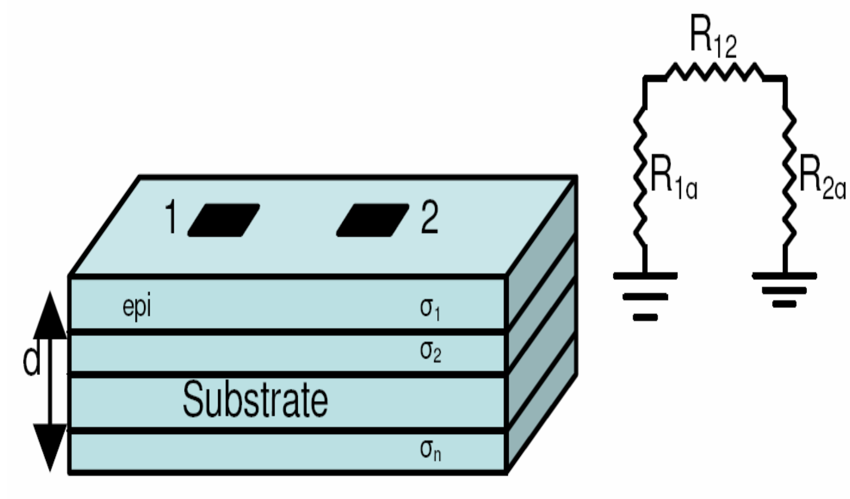
$$\phi(r) = \int_V \rho(r')G(r,r')d^3r'$$

$$[Q] = [c][\phi]$$

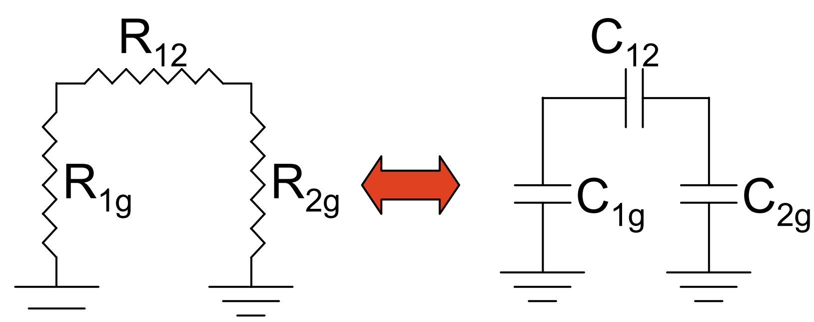
$$C_{ij} = -c_{ij}$$

$$C_{ig} = c_{ii} + \left(\sum_{j=1}^{N} c_{ij} \right)$$

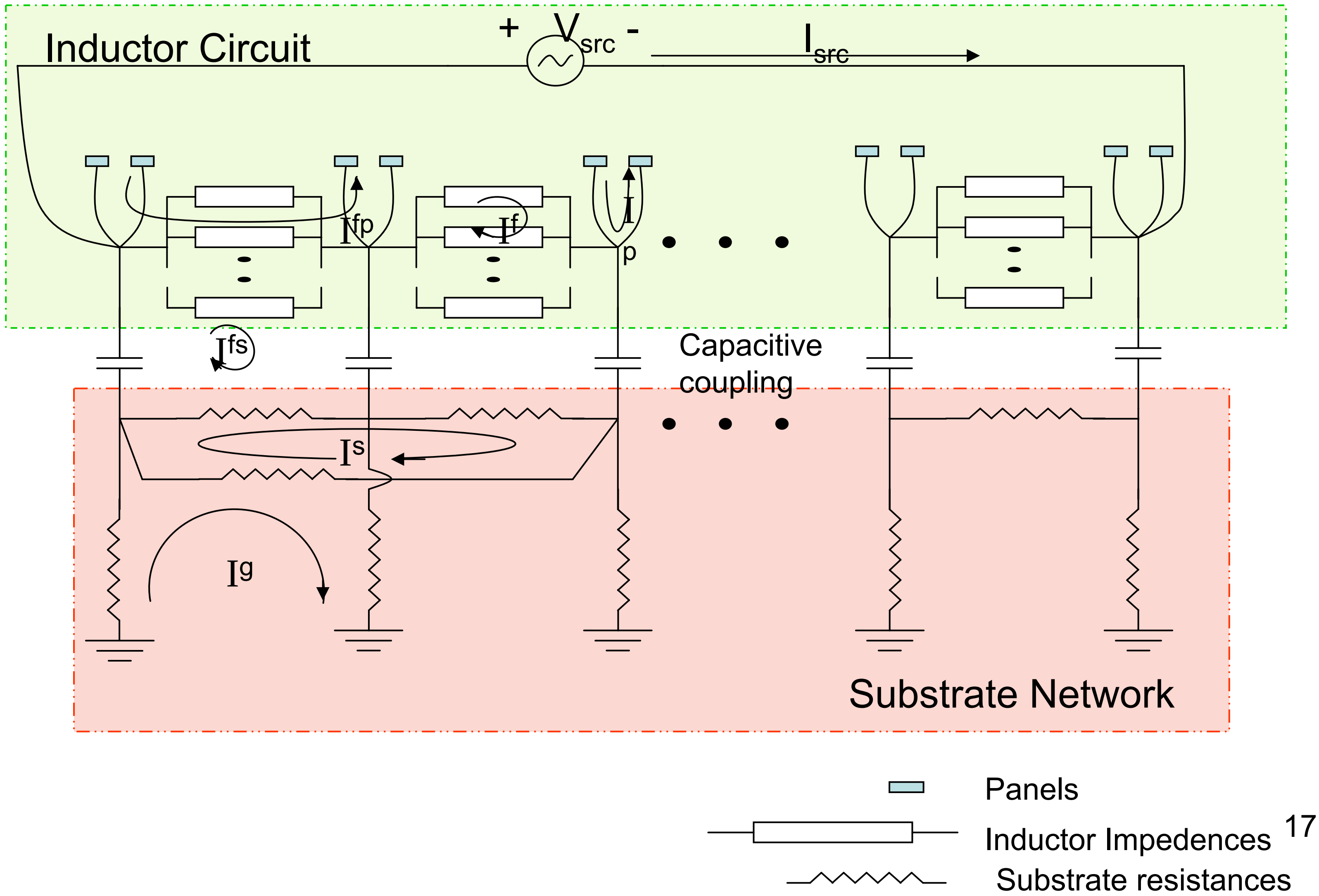
$$R_{ij} = \frac{1}{C_{ij}}$$



Substrate Contact Modelling



Substrate Modeling



Modeling Equations

$$
\begin{bmatrix}
Z_m^f & Z_m^{fp} & Z_m^{fp} & 0 & 0 & 0 & 0 & 0 \\
Z_m^{fp^T} & Z_m^p & Z_m^{fp} & 0 & 0 & 0 & M^{ps} & 0 \\
Z_m^{fp^T} & Z_m^p & Z_m^{fp} + Z_m^{fs} & -Z_m^{gs} & -Z_m^{fs} & 0 & 0 & M^{cs} \\
0 & 0 & -Z_m^{fs^T} & Z_m^g & Z_m^{fs} & 0 & 0 & 0 \\
0 & 0 & -Z_m^{fs^T} & Z_m^{fs^T} & Z_m^s & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & M^p & 0 \\
0 & -pM^{ps^T} & 0 & 0 & 0 & -pM^{p^T} & sI & 0 \\
0 & 0 & -p_c M^{c^T} & 0 & 0 & 0 & 0 & sI
\end{bmatrix}
\begin{bmatrix}
I_m^f \\ I_m^{fp} \\ I_m^{fs} \\ I_m^{sg} \\ I_m^s \\ I_m^p \\ V_b^p \\ V_b^c
\end{bmatrix}
=
\begin{bmatrix}
V_b^f \\ V_b^{fp} \\ V_b^{fs} \\ V_b^{sg} \\ V_b^s \\ V_b^p \\ 0 \\ 0
\end{bmatrix}
$$

$$sLx = -Rx + BV_{src}$$

PEEC CIRCUIT

$$sLx = -Rx + BV_{src}$$

- Let,

$$E = sL + R$$

$$\Rightarrow Ex = Bu$$

- Size of E can be prohibitively large.
- E is constructed from scratch in each iteration.
- Equation need to be solved every time configuration is changed.

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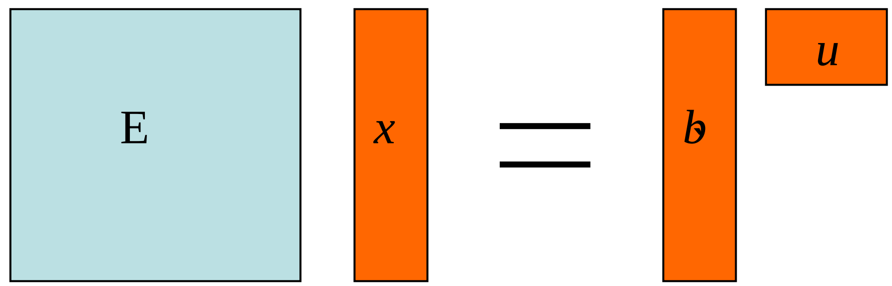
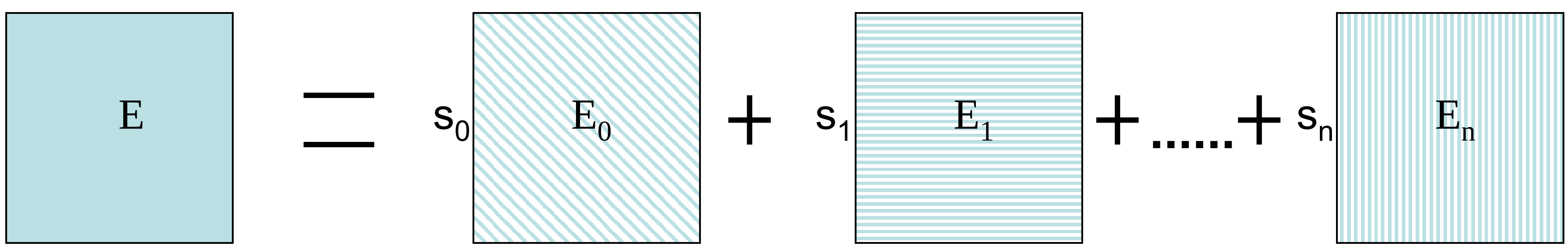
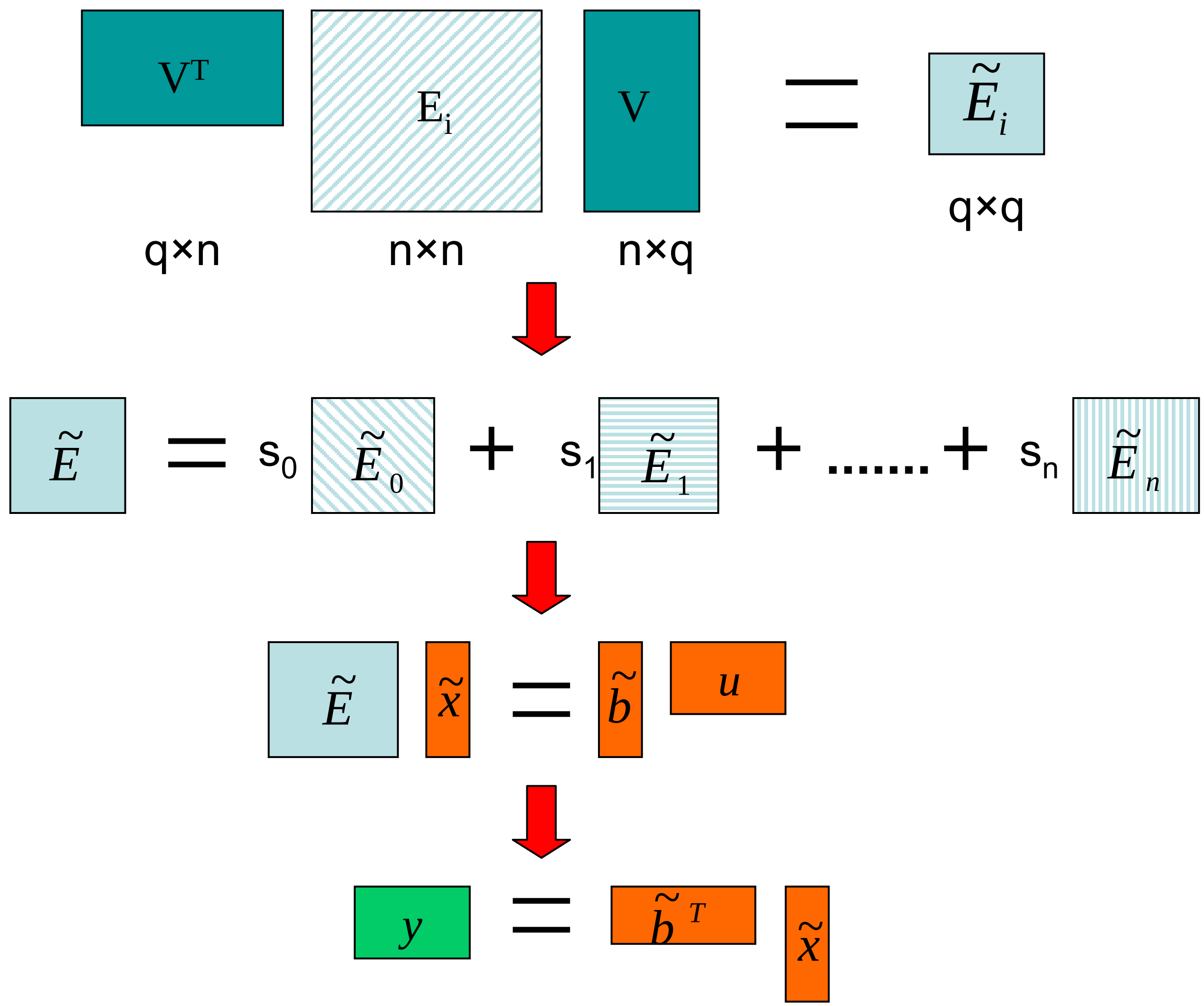
Parameterization



$$s_i = \{1, d, W, dW, d^2, W^2\}$$



Model Reduction



Control Flow

- Compute $\tilde{E}_i$ from a set of sample points (w_i, d_i).
- New configuration : $W_1 \longrightarrow W_2$, $d_1 \longrightarrow d_2$
  - s_i ε $\{1, d_2, W_2, d_2W_2, d_2^2, W_2^2, s, sd_2, sW_2, sd_2W_2, sd_2^2, sW_2^2\}$.
  - Compute new $\tilde{E}$:

$$\tilde{E} = s_0 \tilde{E}_0 + s_1 \tilde{E}_1 + \ldots\ldots + s_n \tilde{E}_n$$

  - Solve for *y*.

$$\tilde{E}\,\tilde{x} = \tilde{b}\,u$$

$$y = \tilde{b}^T \tilde{x}$$

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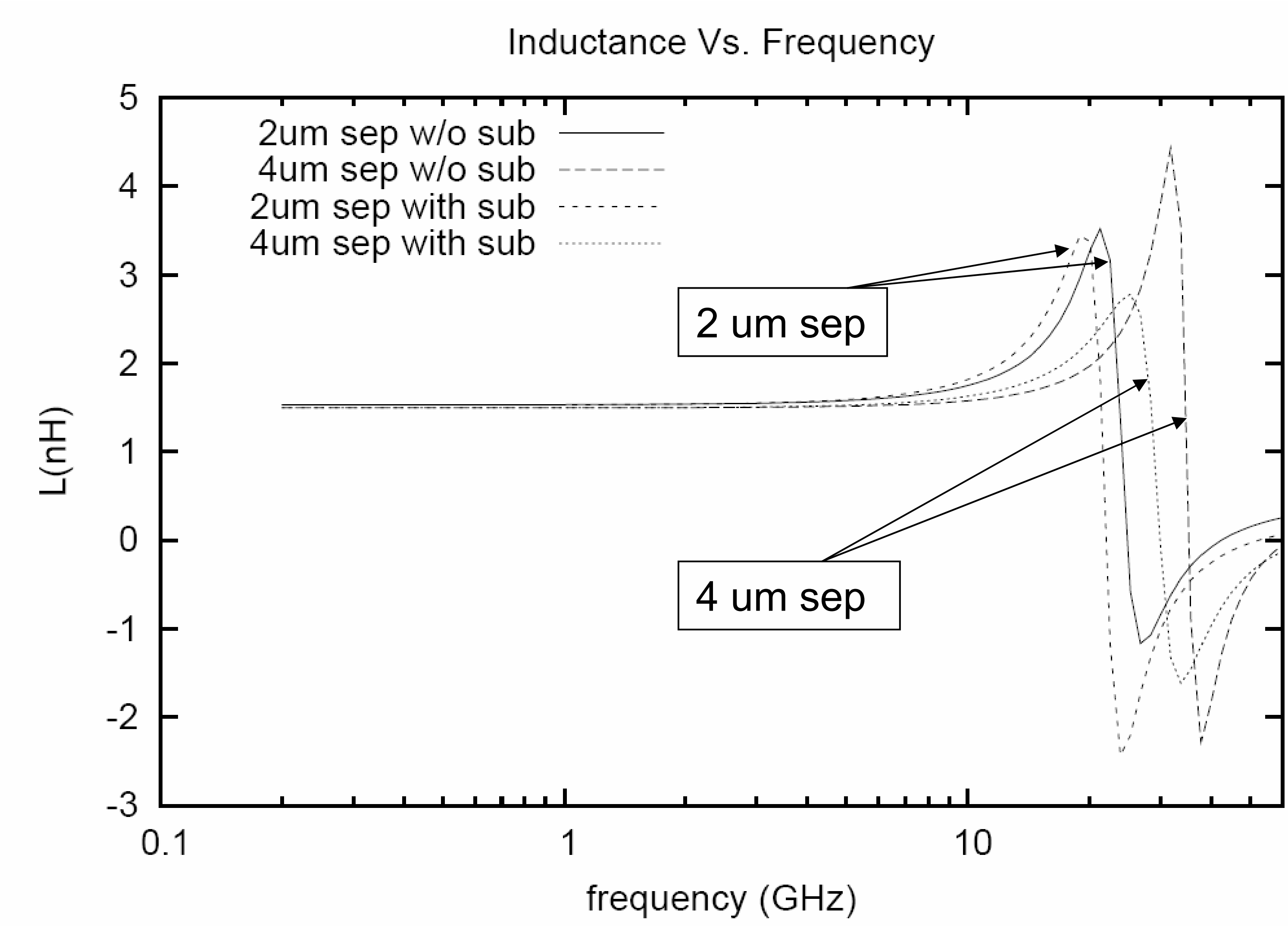
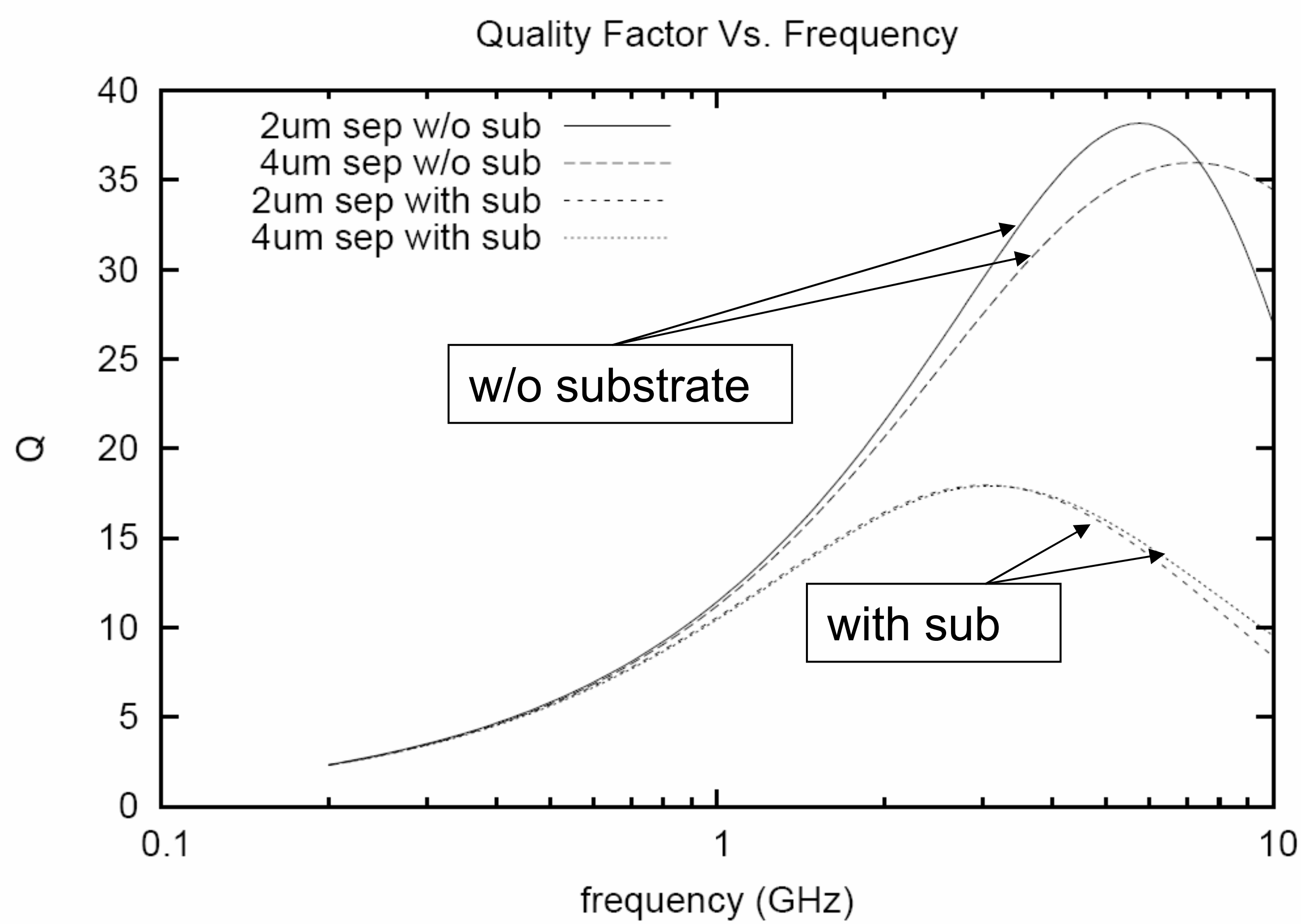
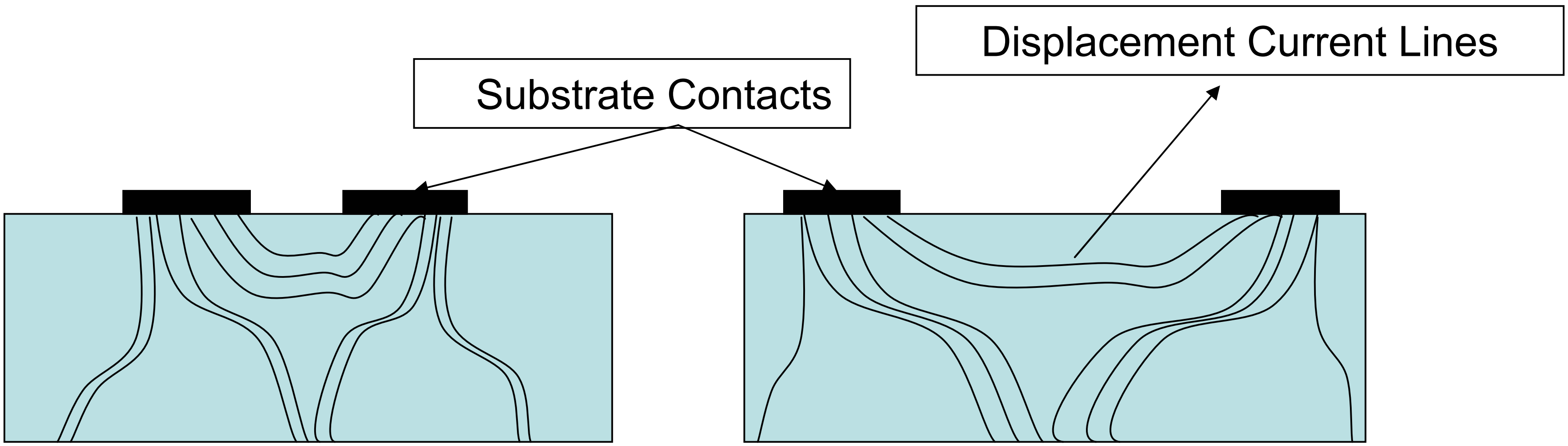
Results : Effects of Substrate on Inductance



Results : Effects of Substrate on Quality Factor

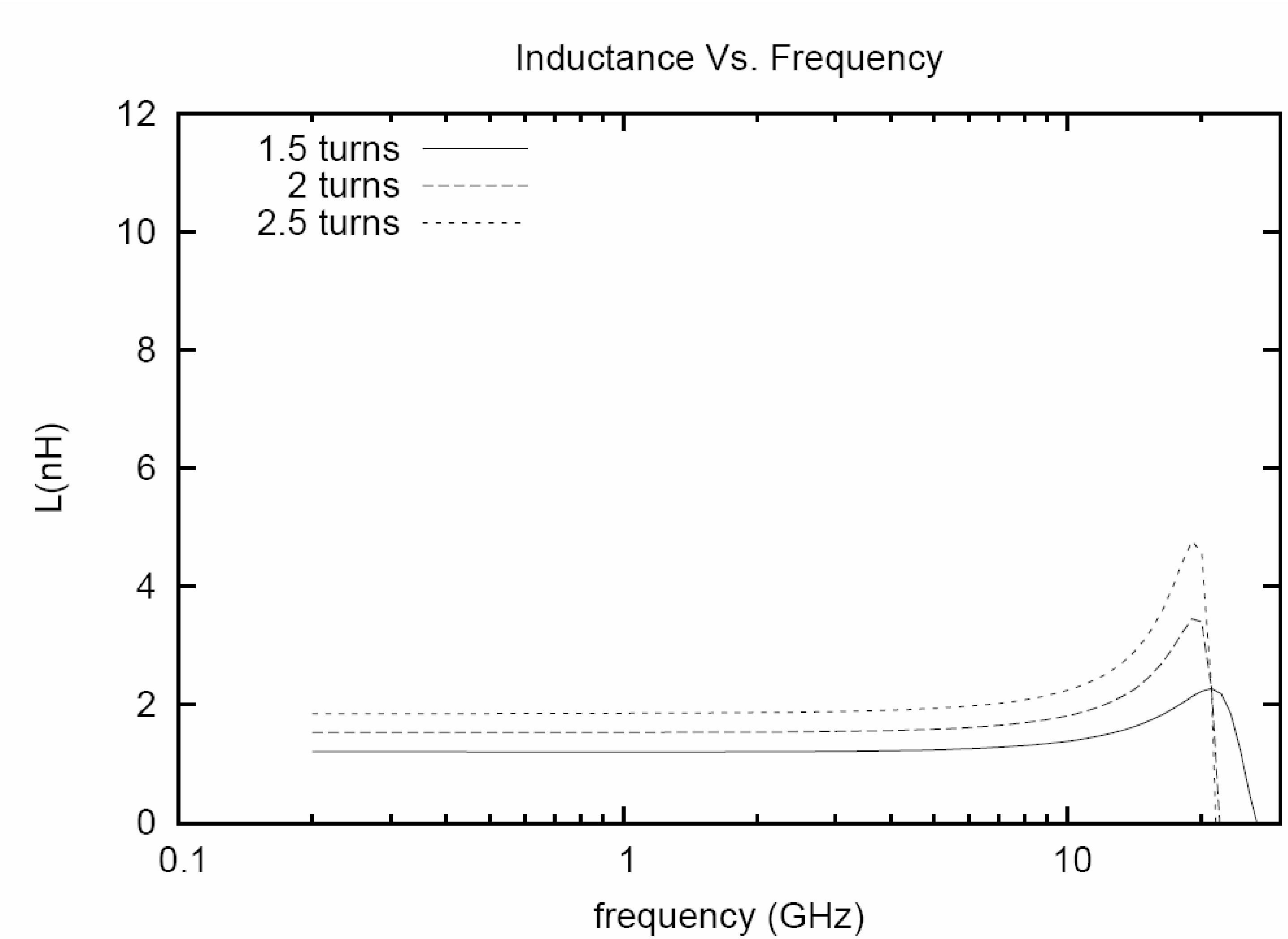


Effects of Separation B/W Turns

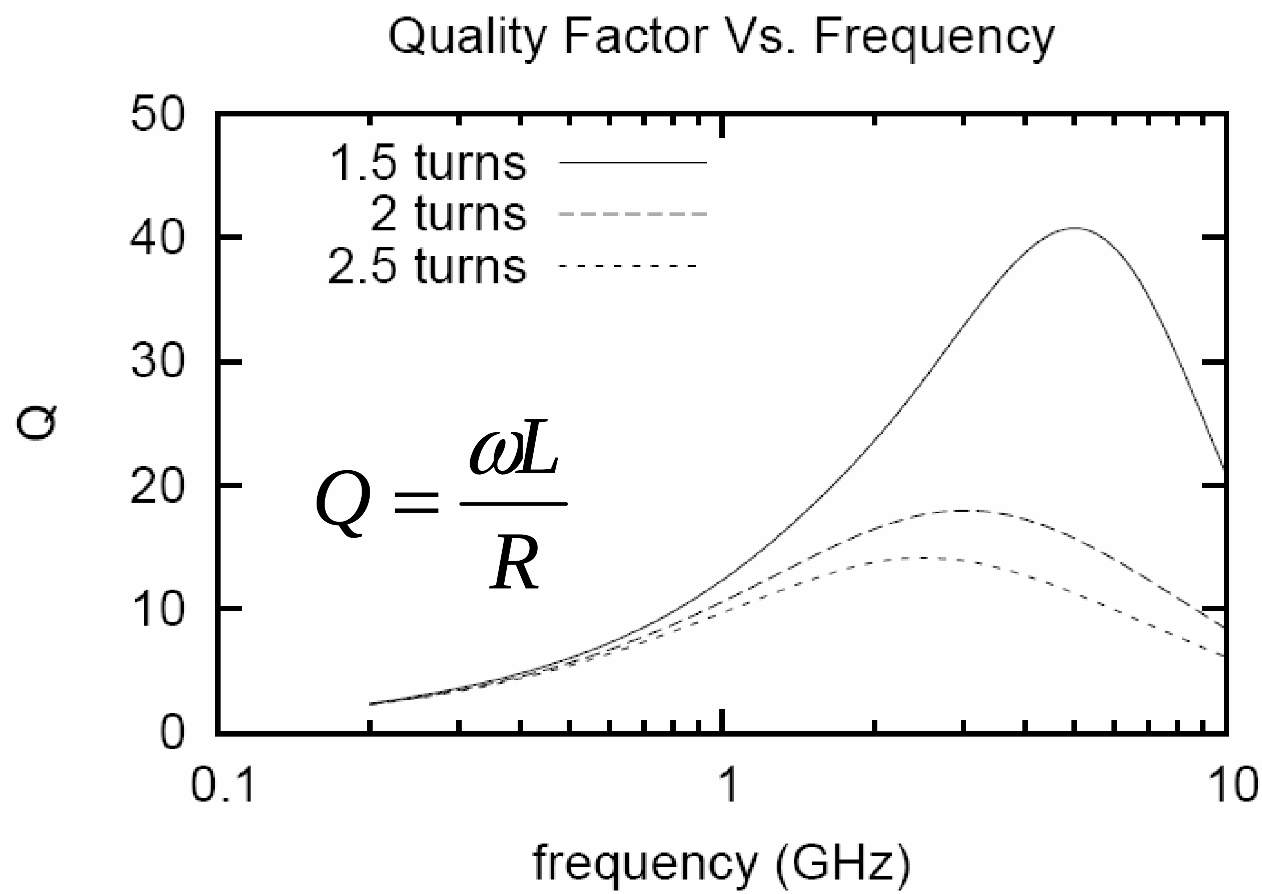


R_{sub_1} << R_{sub_2}

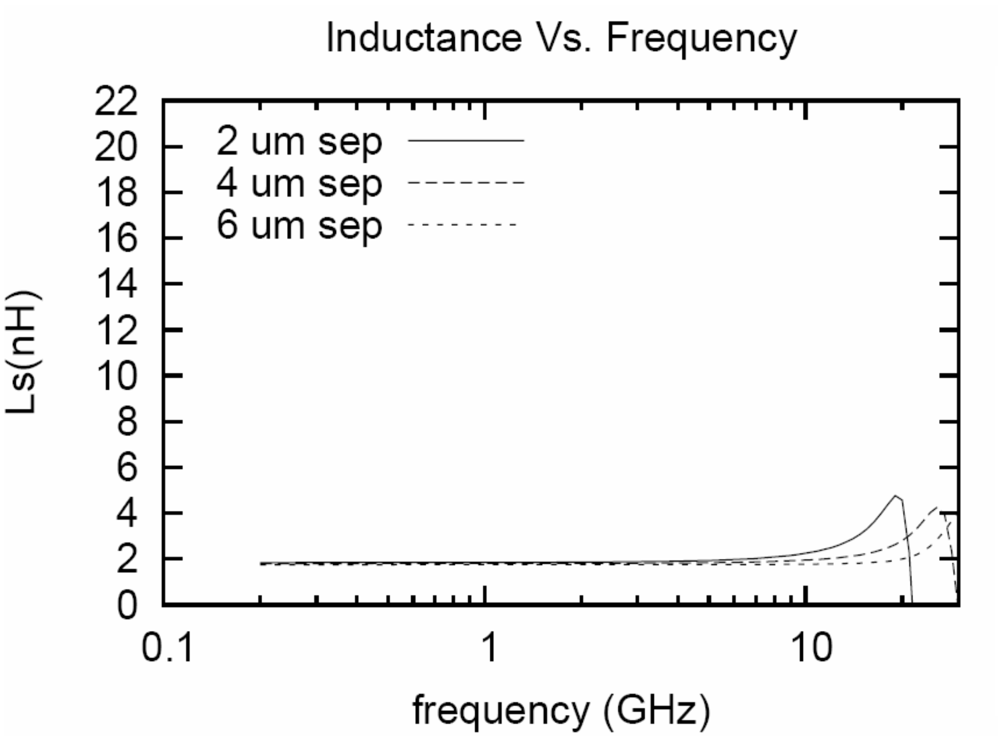
Results : Number of Turns



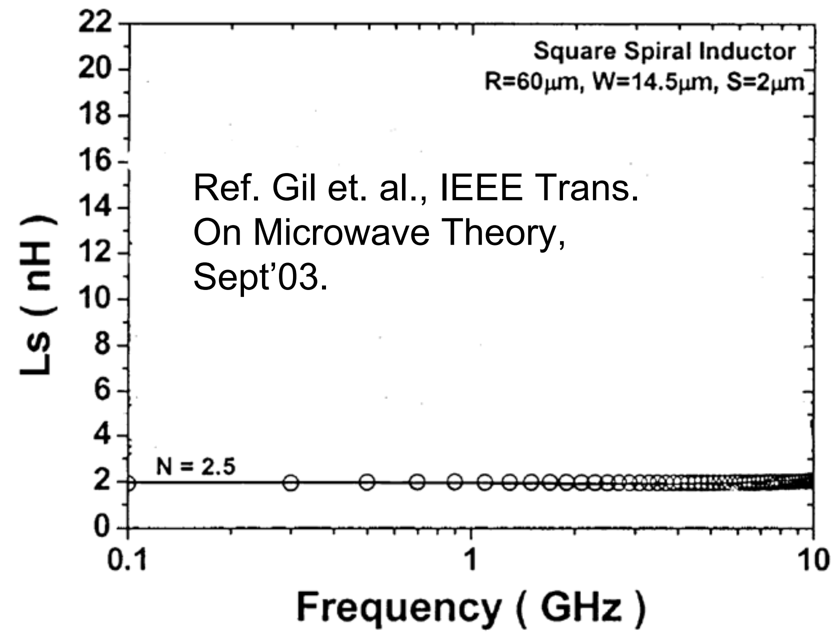
Results : Number of Turns



Results : Simulated Vs Measured Inductance

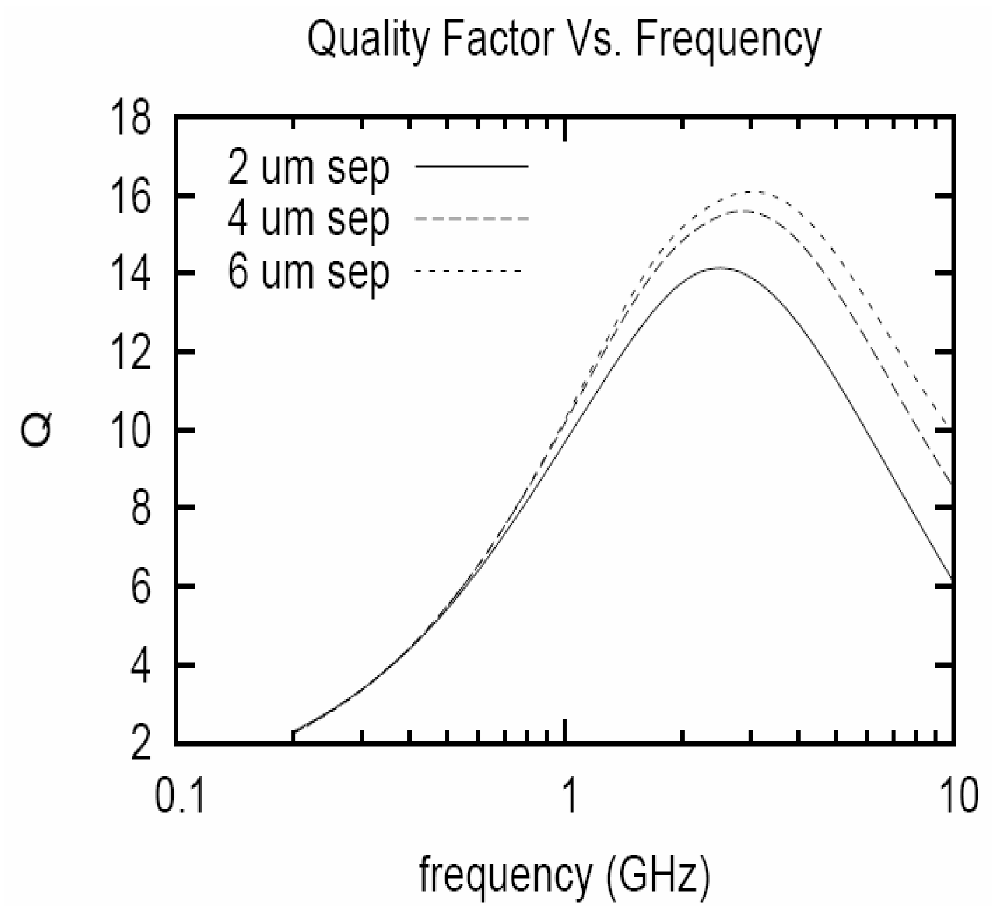


Simulated Inductance

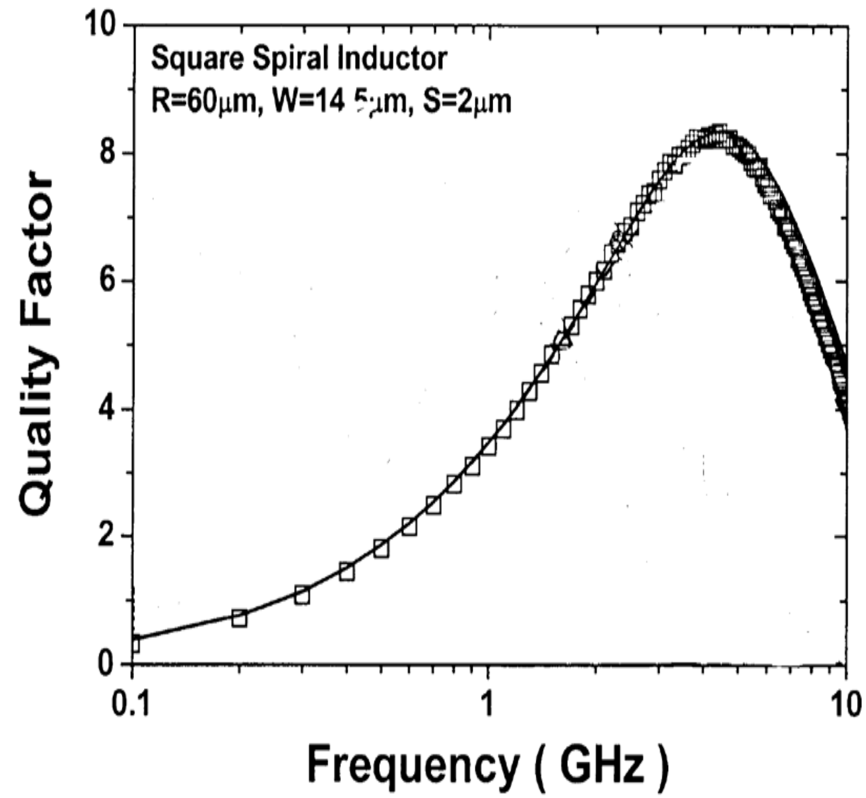


Measured Inductance

Results : Simulated Vs Measured Quality Factor



Simulated Q Values



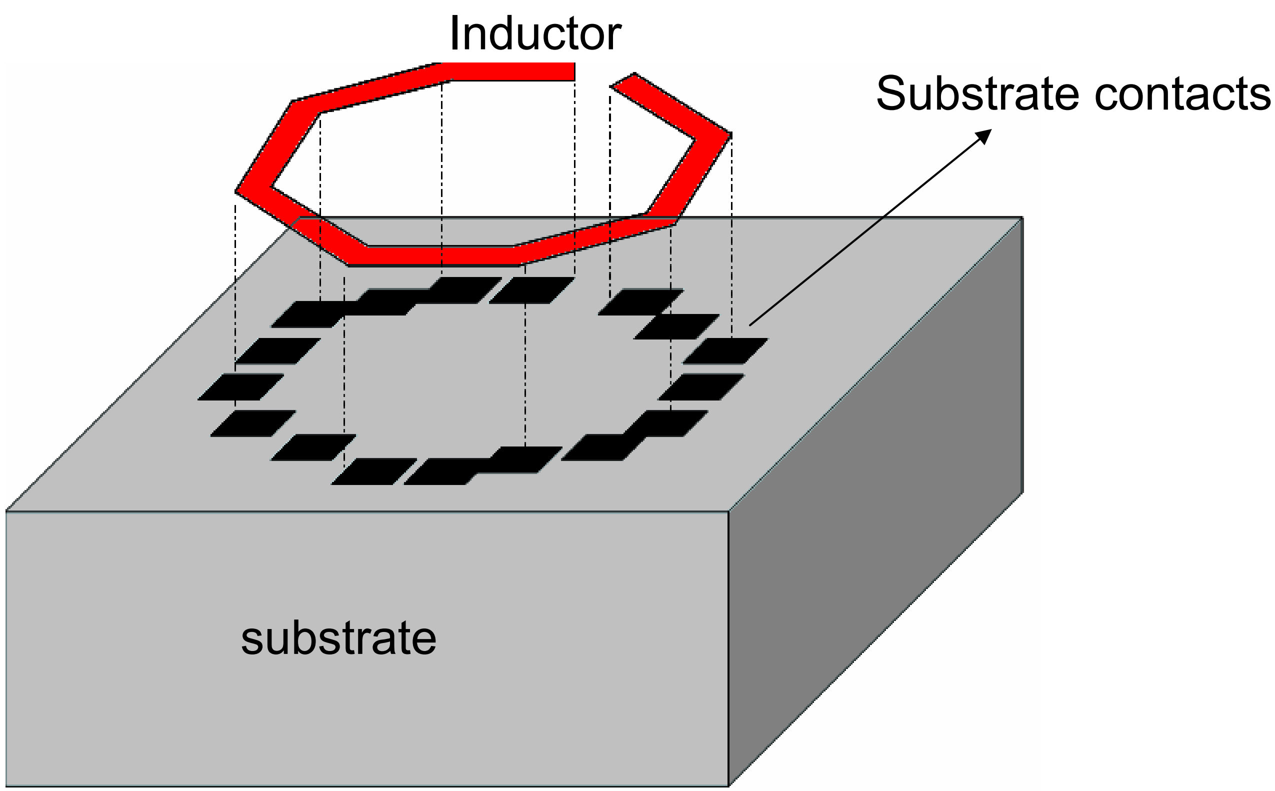
Measured Q Values

CPU Time

- 2 GHz Intel Pentium 4 processor
- 1 GB RAM

Configuration	**w/o param**	**with param**
1 turn (10 config)	15 min/config	15 min + 2 sec/config
2 turns (10 config)	35 min/config	35 min + 2 sec/config
2.5 turns (10 config)	50 min/config	60 min + 2 sec/config

Modeling Octagonal Shapes



Octagonal RF Inductor

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- Theoretical Background
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Conclusion

- A substrate aware parameterization technique has been proposed.
- The substrate has a significant impact on quality of RF inductors.
- The simulator accurately models the inductance.
- The small discrepancy in Q is due to inability to model via resistances.

Future Work

- Scheme to model “via” resistance.
- Include Eddy Current effects in model.
- Make the model efficient
  – Using standard sparse matrix packages.
  – Optimizing on matrix operations.

Thank You