Modeling and Simulation of Jitter in Phase-Locked Loops due to Substrate Noise

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Outline

- Introduction
- Substrate Noise Coupling Mechanism and Modeling Technique
- Comparison between Simulation Methodologies
- Period Histogram and Comparison with Measurements
- Conclusion

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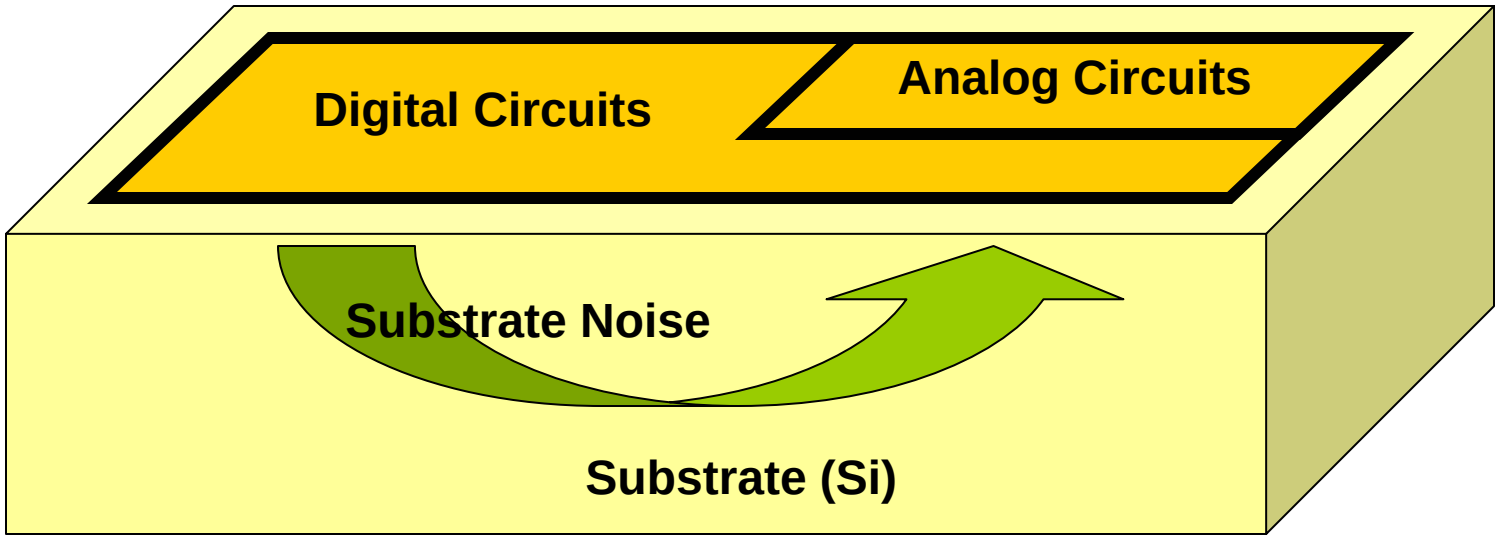
Substrate Noise in Systems-on-a-Chip (SoC)

- Demands for total system on same chip
- Mixed signal systems: substrate noise issue
- LNA, VCO, PA and DA/AD as victims

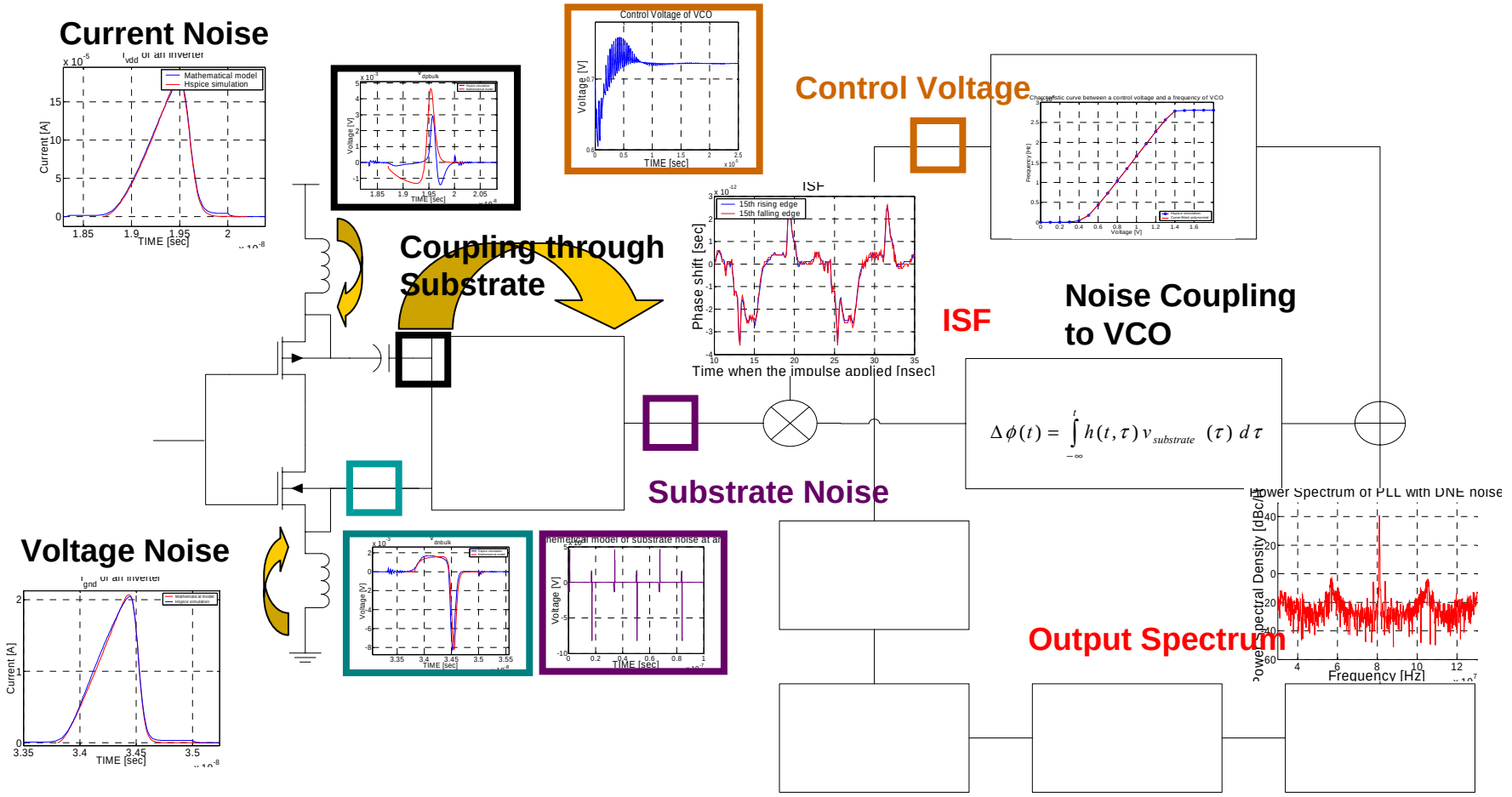


Simulations for Analog Systems under Substrate Noise Environment

- The simulations of substrate noise coupling to analog systems can be simple conceptually, but is definitely demanding in transistor-level and transient analysis mode.
- The blocks of an analog system are not equally sensitive to substrate noise. And substrate noise coupling mechanism itself is deterministic, thus allowing to abstract behavioral models.
- Considering these factors, simulations for PLL under substrate noise environment can be a challenging but good candidate.

Substrate Noise Coupling in SoC

- Block diagram of mixed signal system with PLL



Two Levels of Simulation

	Circuit level	System level
Target System	Digital Noise Emulator and PLL	
Tools	Hspice, Spectre	C++, Verilog-A
Purpose / Features	Verification Slow but accurate	Quick guide Fast but rough

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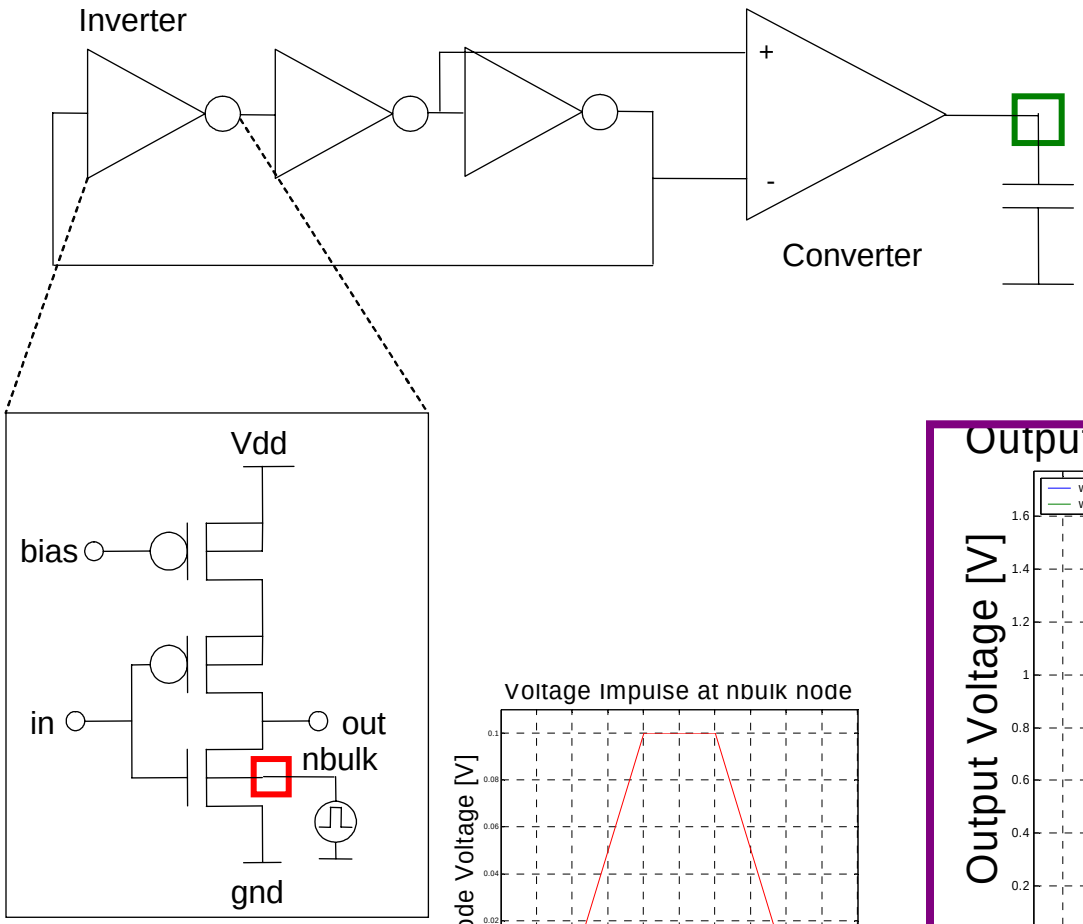
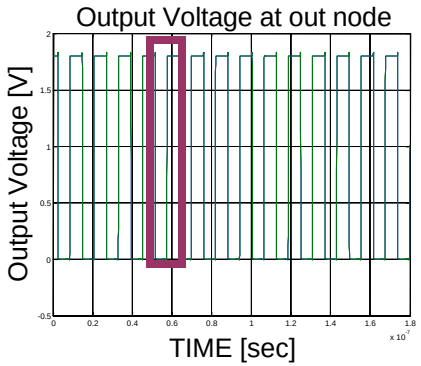
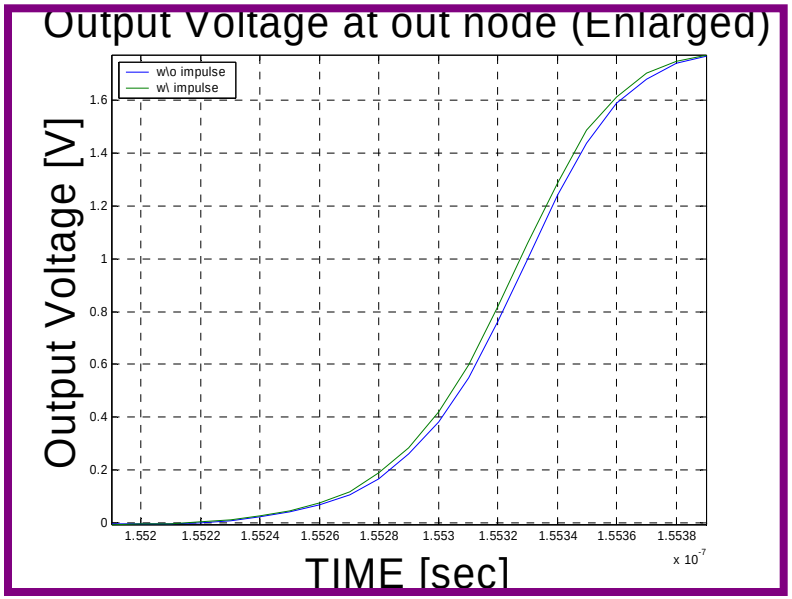
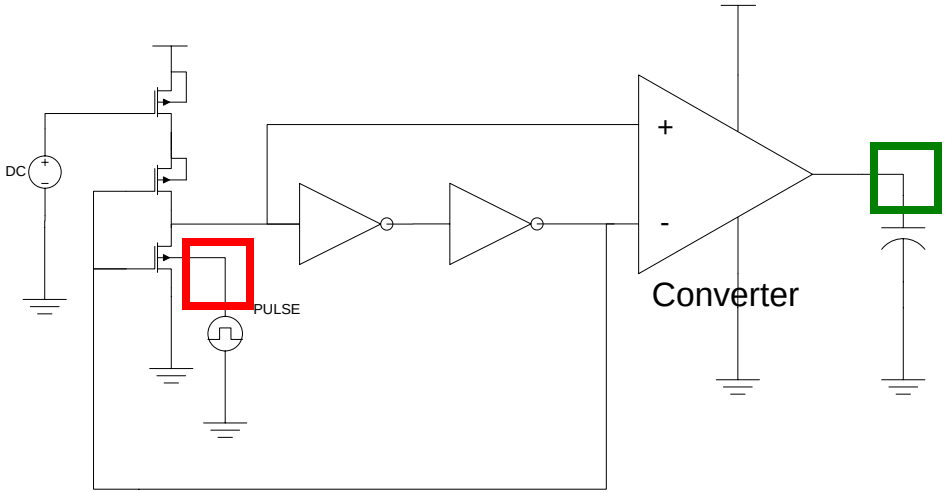
Substrate Noise Coupled to VCO

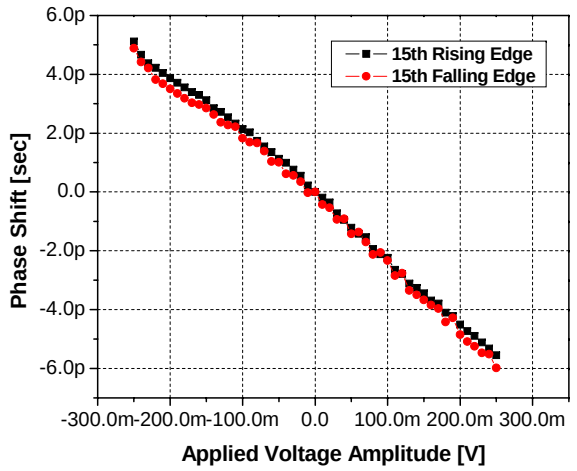


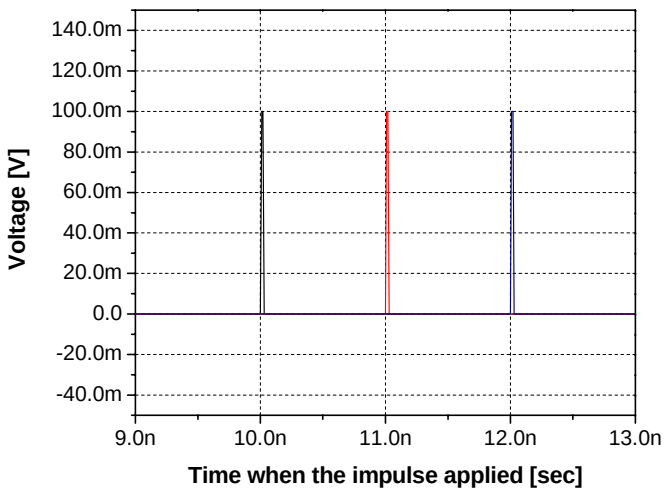


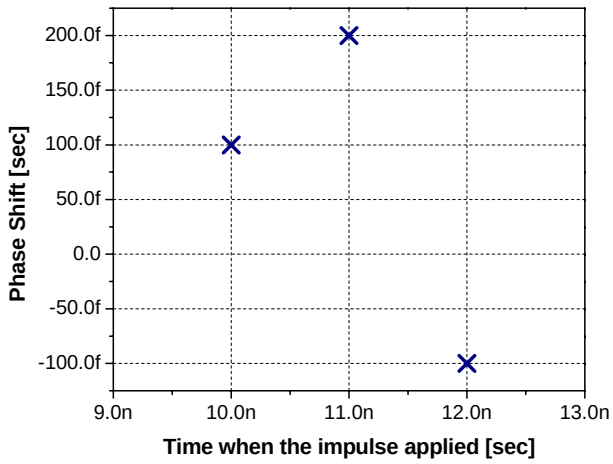


Substrate Noise Sensitivity Function of VCO



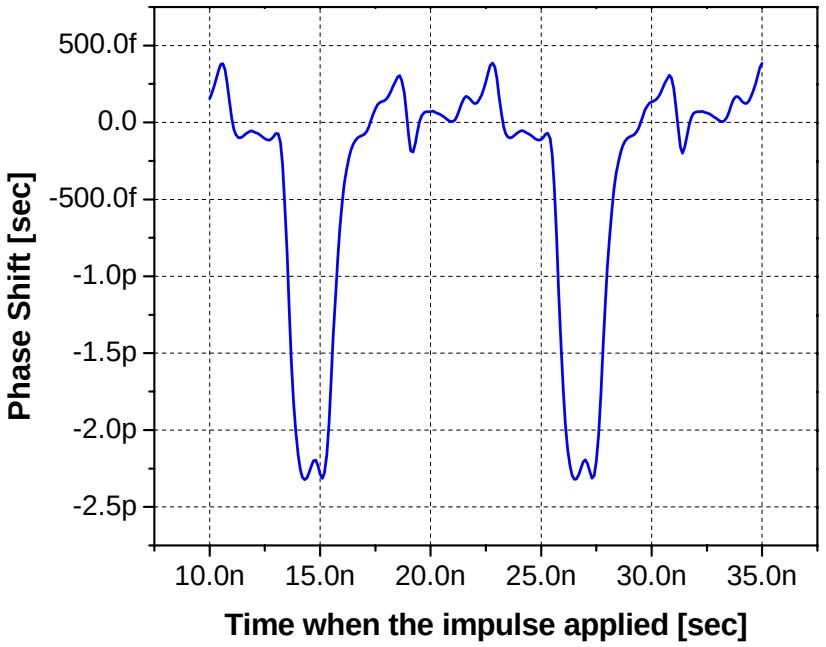


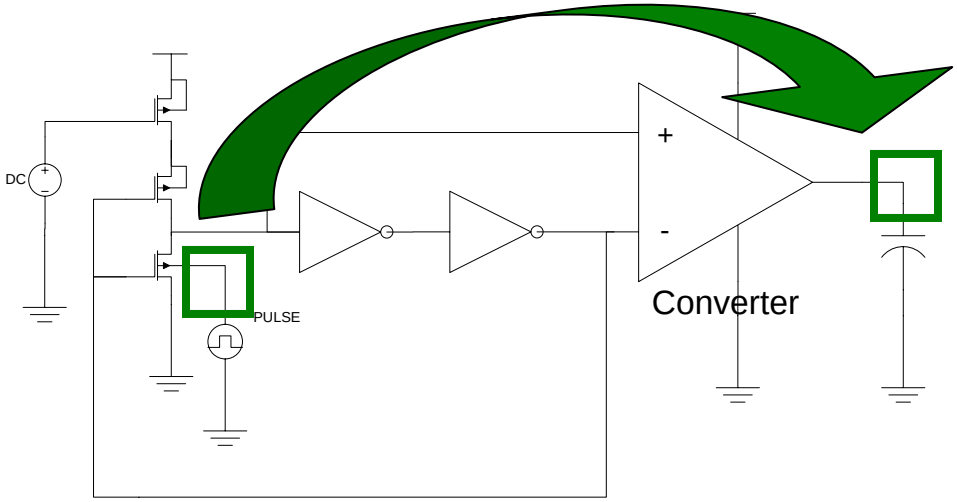




Behavioral Model
– Noise coupling equation

- ISF_V – Impulse Sensitivity Function between substrate noise and phase shift

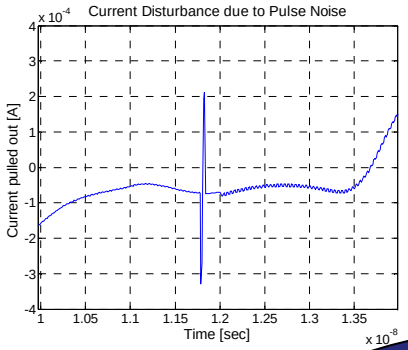




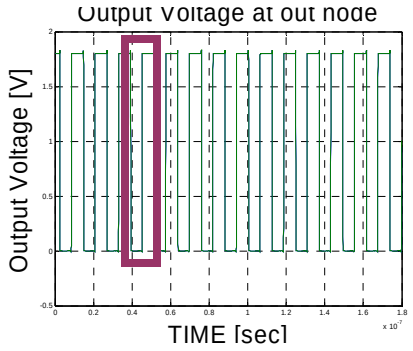
$$\Delta\Phi(t) = \int_0^t V_{\text{sub}}(\tau) ISF_{\text{v}}(\tau) d\tau$$

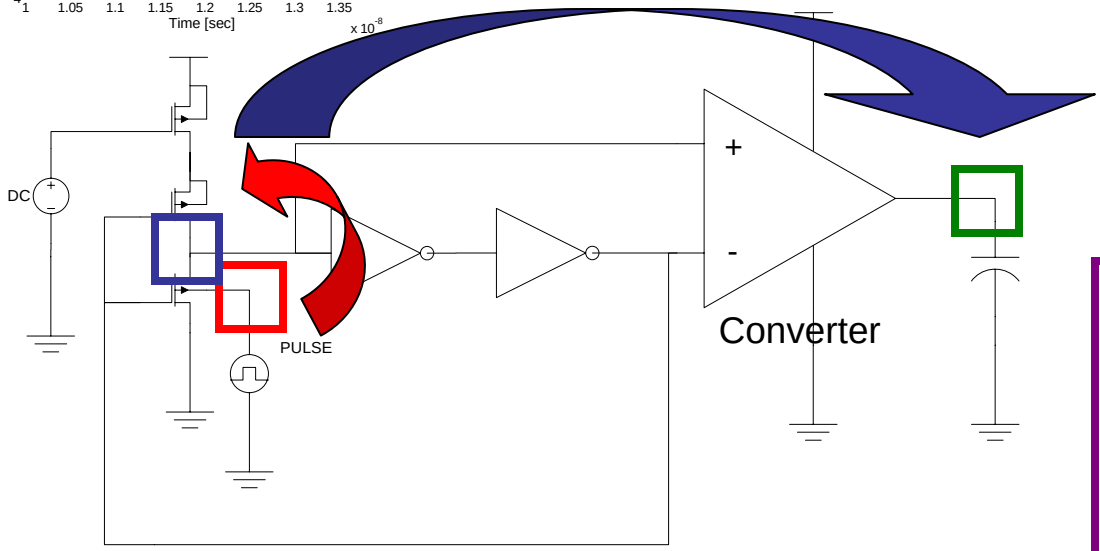
Analysis

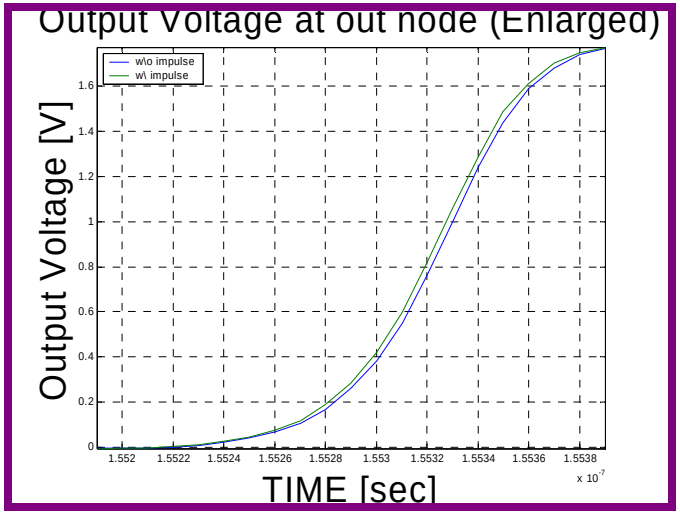
- Substrate noise coupling mechanism to VCO

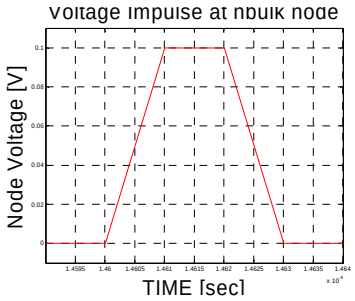


Current Disturbance to Phase Shift



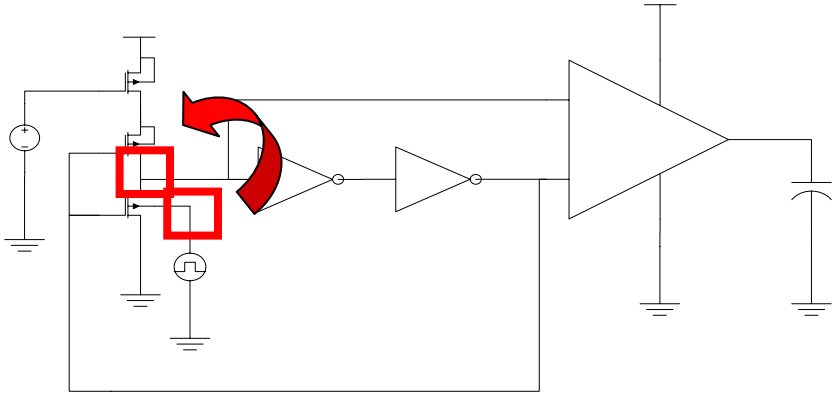


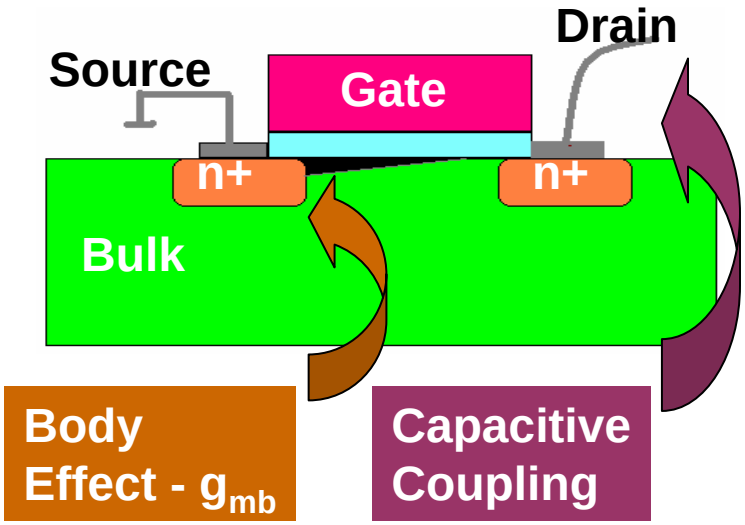




Substrate Noise to Current Disturbance

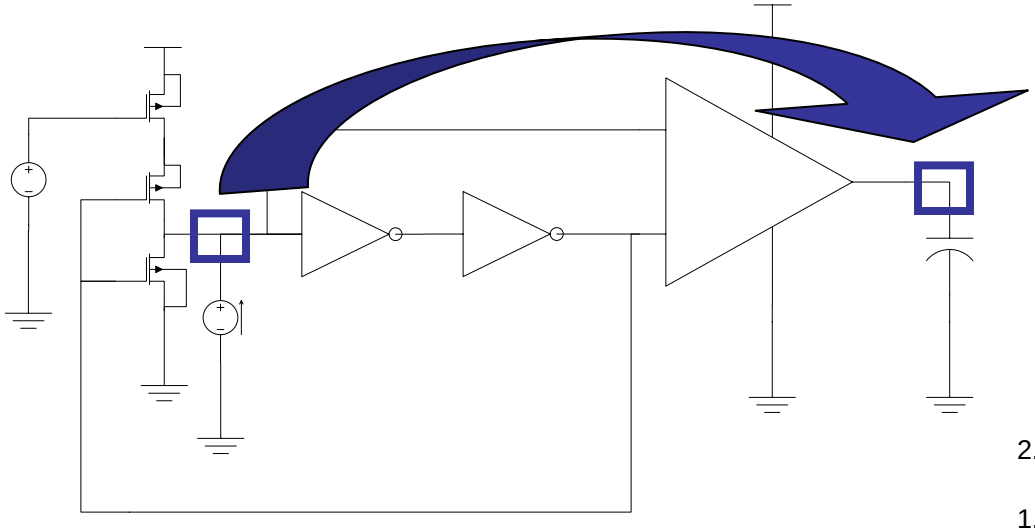
Analysis
- Substrate noise to current disturbance

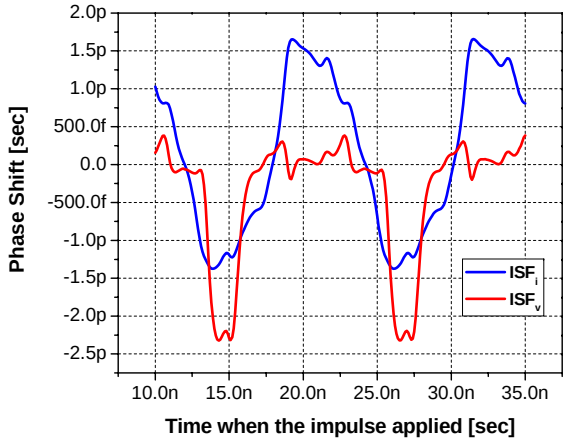




- Body effect
  - Linear parameter: g_{mb}
  - $\Delta I = g_{mb} V_{sub}$
- Capacitive coupling
  - Through pn+ junction capacitance
  - $\Delta I = C_j dV_{sub}/dt$
- Total current noise
  - $\Delta I = g_{mb} V_{sub} + C_j dV_{sub}/dt$

Analysis
- Current disturbance to phase noise: ISF_i



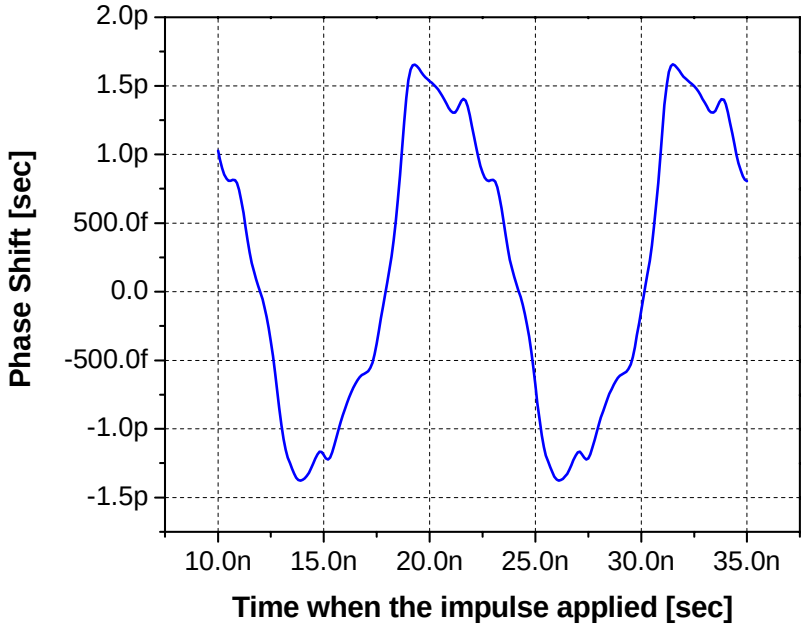


$$\Delta\Phi(t) = \int_0^t \Delta I(\tau) ISF_{\mathrm{i}}(\tau) d\tau$$

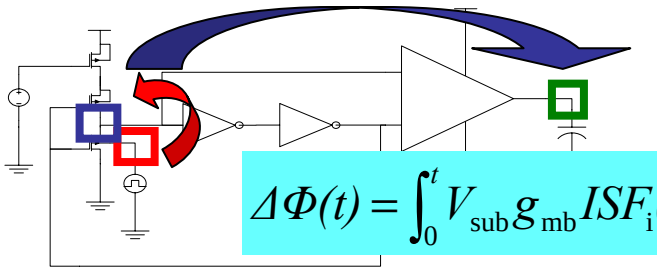
$$= \int_0^t V_{\mathrm{sub}} g_{\mathrm{mb}} ISF_{\mathrm{i}} + C_{\mathrm{j}} \frac{dV_{\mathrm{sub}}}{d\tau} ISF_{\mathrm{i}} d\tau$$

When V_{sub} is an impulse function ($\delta(t\text{-}t_0)$),

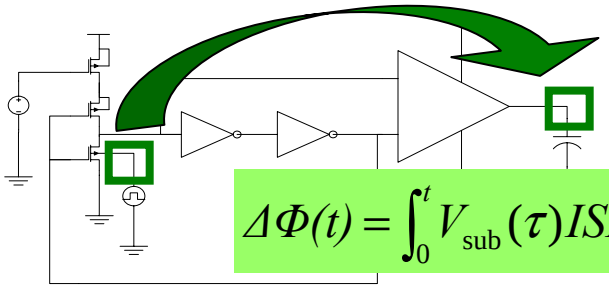
$$\int_0^t C_{\mathrm{j}} \frac{dV_{\mathrm{sub}}}{d\tau} ISF_i d\tau = C_{\mathrm{j}} ISF_{\mathrm{i}}(t_0) \int_0^t \frac{d\,\delta(\tau\text{-}t_0)}{d\tau} d\tau = 0$$



Behavioral Model
– Noise coupling equation based on analysis

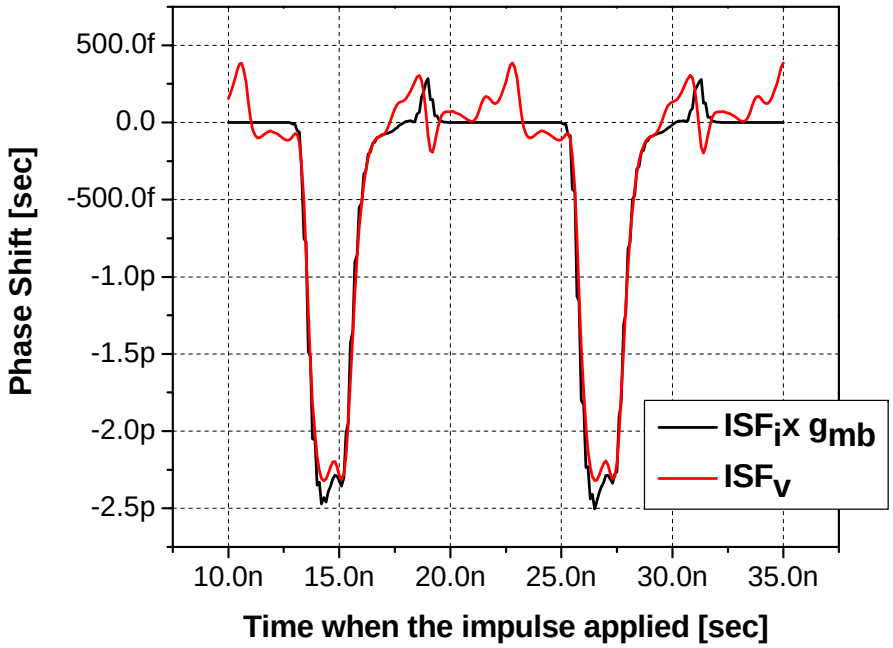


$$\Delta\Phi(t) = \int_0^t V_{\text{sub}} g_{\text{mb}} ISF_{\text{i}}(\tau) d\tau$$



$$\Delta\Phi(t) = \int_0^t V_{\text{sub}}(\tau) ISF_{\text{v}}(\tau) d\tau$$

$$ISF_{\text{v}} = g_{\text{mb}} ISF_{\text{i}}$$



$$\Delta\Phi(t) = \int_0^t (V_{\text{sub}} g_{\text{mb}} + C_{\text{j}} \frac{dV_{\text{sub}}}{d\tau}) ISF_i \, d\tau = \int_0^t (V_{\text{sub}} g_{\text{mb}} ISF_{\text{i}} + C_{\text{j}} \frac{dV_{\text{sub}}}{d\tau} ISF_{\text{i}}) d\tau$$

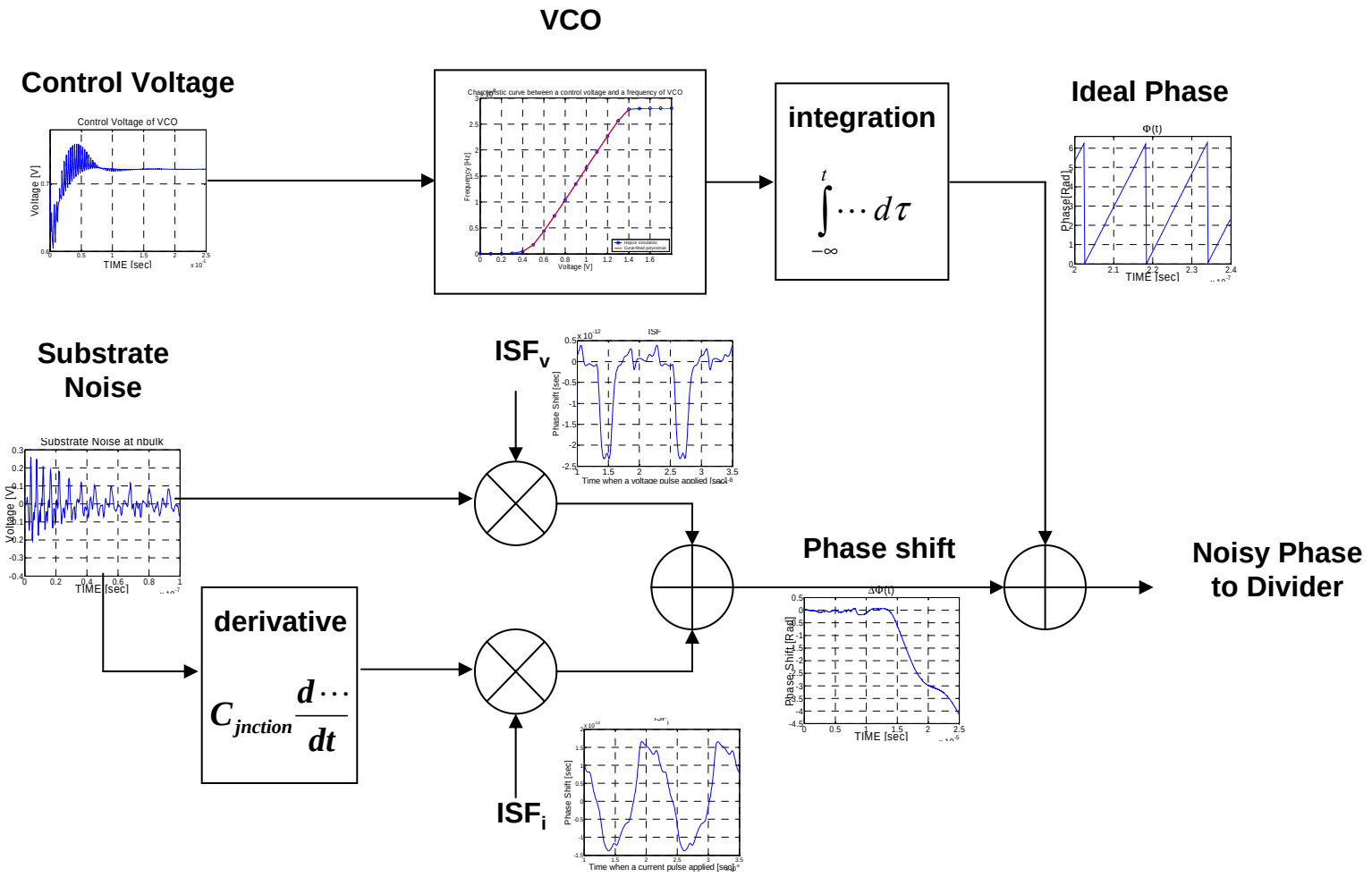
$$= \int_0^t V_{\text{sub}} ISF_{\text{v}} \, d\tau + \int_0^t C_{\text{j}} \frac{dV_{\text{sub}}}{d\tau} ISF_{\text{i}} \, d\tau$$

+

DC

-

Behavioral Model
– Block diagram of VCO



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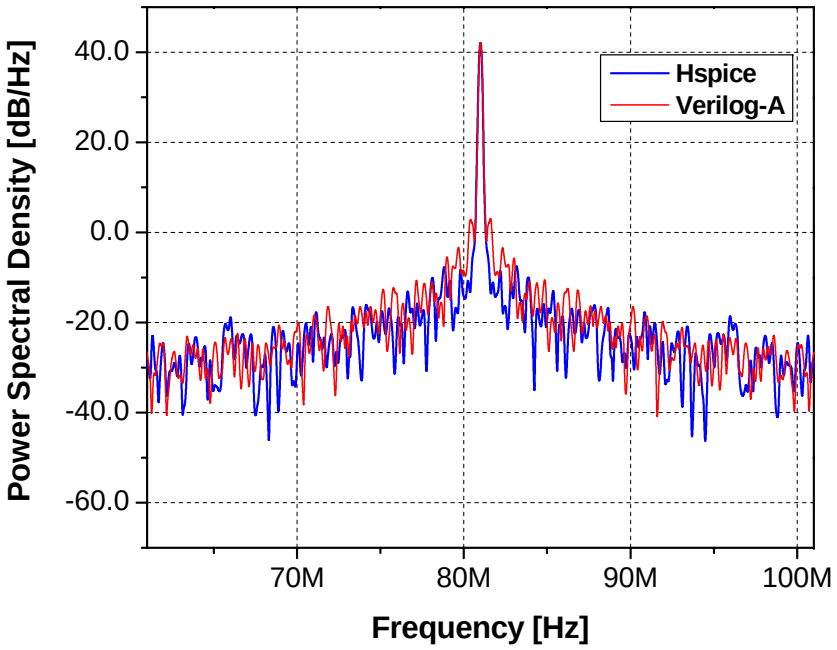
Comparison between Simulation Methodologies - I

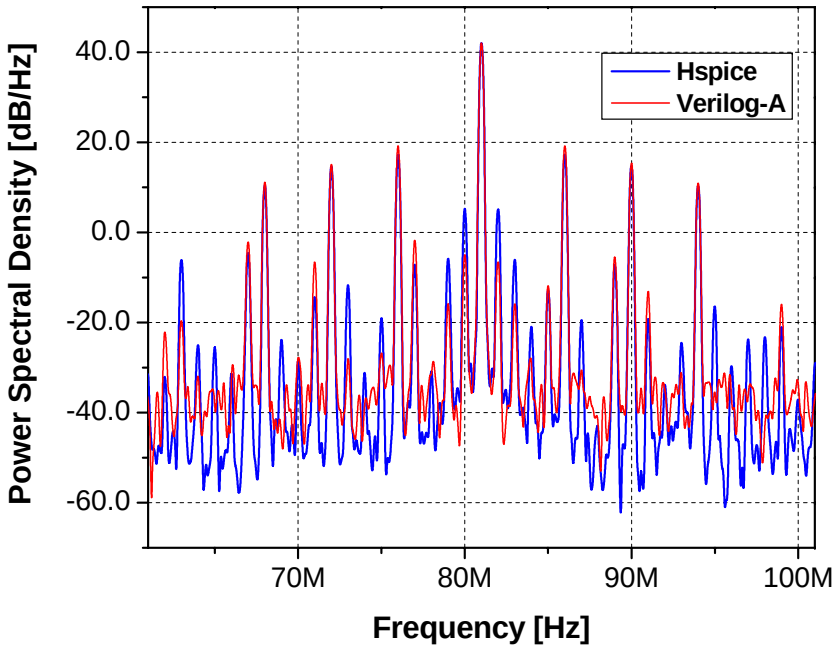
- Verilog-A and Hspice
- Two versions of Verilog-A
  - Interpreter based: Cadence
  - Compiler based: Tiburon Design Automation
- Transient simulation of PLL and sampling 1,250,000 temporal points

Language	Hspice	Cadence Verilog-A	Tiburon Verilog-A
Simulation time	14 hrs 53 mins	19 mins	18 mins

Comparison between Simulation Methodologies - II

- 81MHz PLL with white Gaussian random noise
- Summation of three sinusoidal waves (5MHz, 13MHz, and 90MHz)





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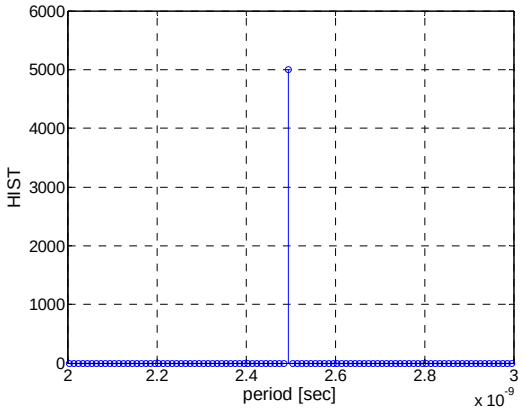
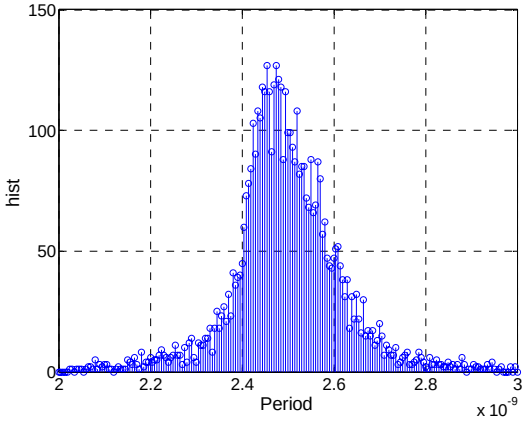
Period Histogram
- Concept

- A metric to estimate the phase shift
- Ideal case
  - One period, one peak
- With noise
  - Jitter causes the histogram changing shape.

- Ideal case

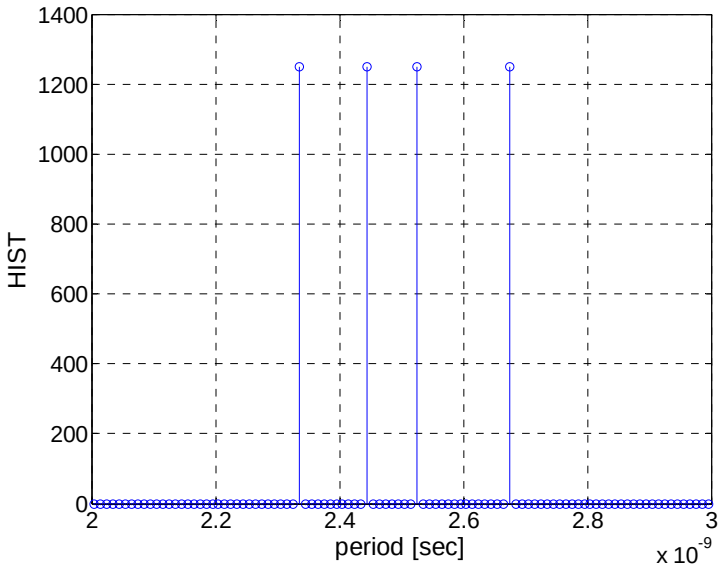


- With noise

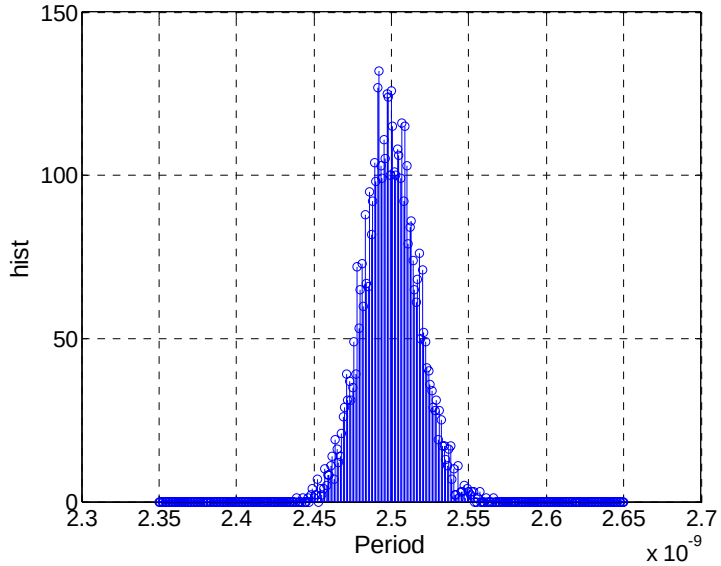


Period Histogram
- Noise dependency

- Periodic noise
  - 400MHz PLL with 100mV, 100MHz sinusoidal wave noise
  - Peak splitting

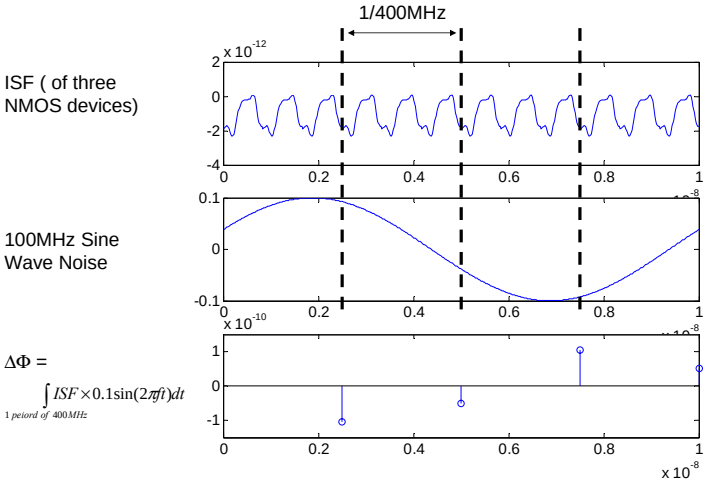


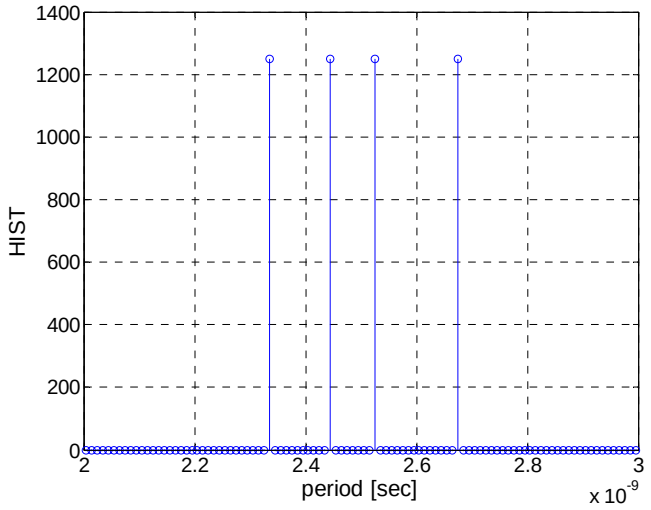
- Random noise
  - With 100mV(RMS) white Gaussian noise
  - Histogram spreading

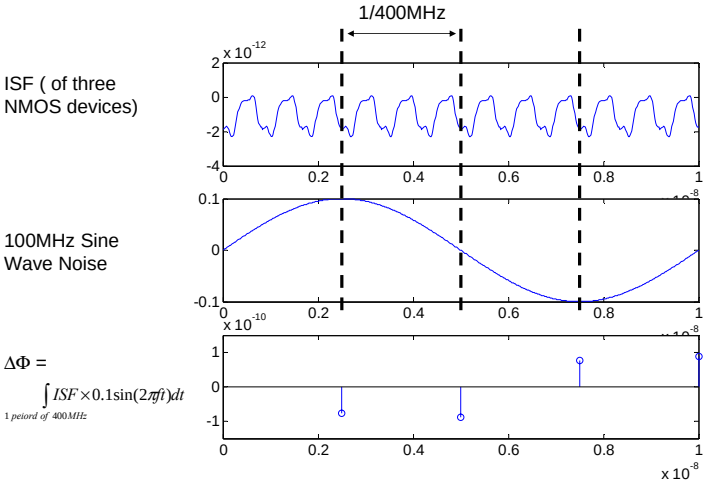


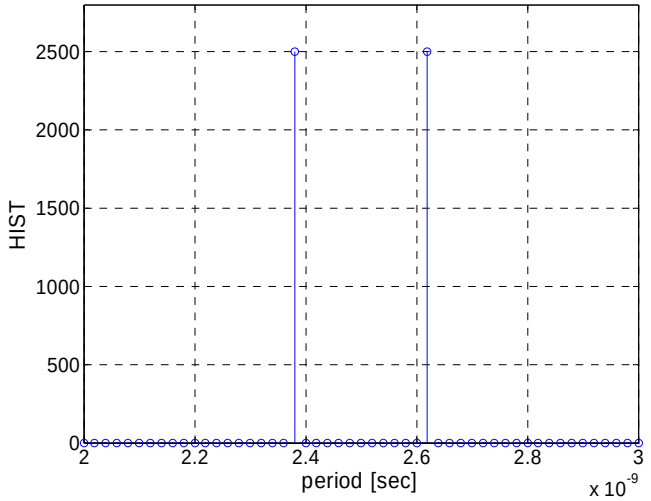
Period Histogram
- Variation with phase of noise

- 400MHz PLL with 100MHz sinusoidal noise



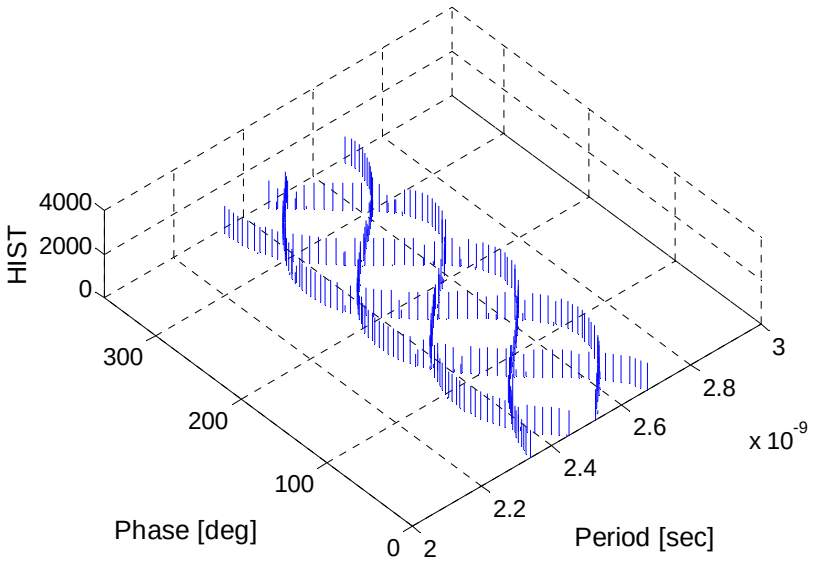




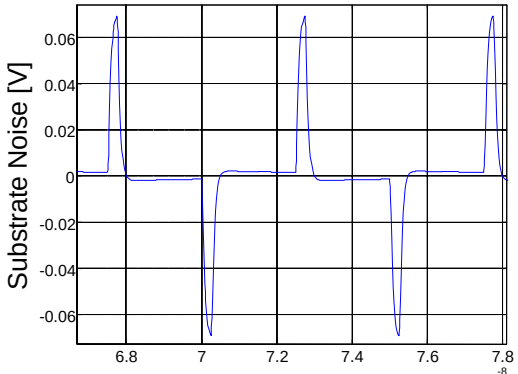


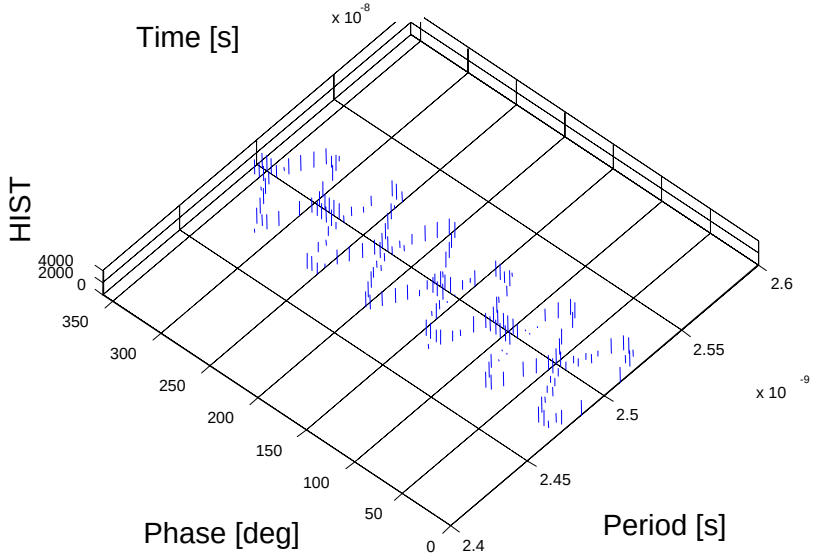
Period Histogram
- 3-D plot of period histogram

- 100MHz sinusoidal noise



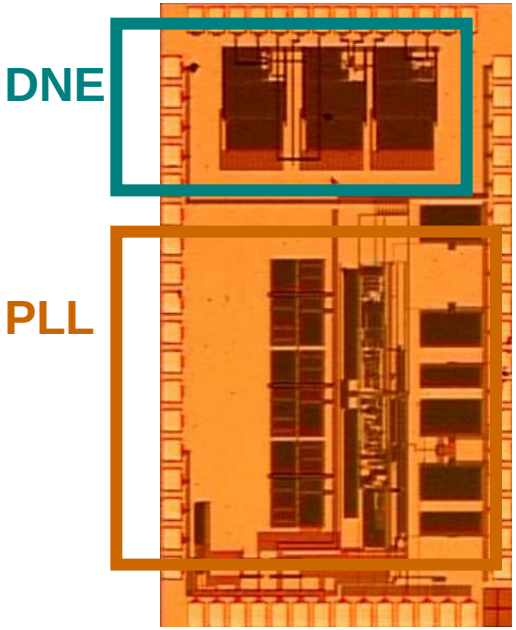
- Switching noise

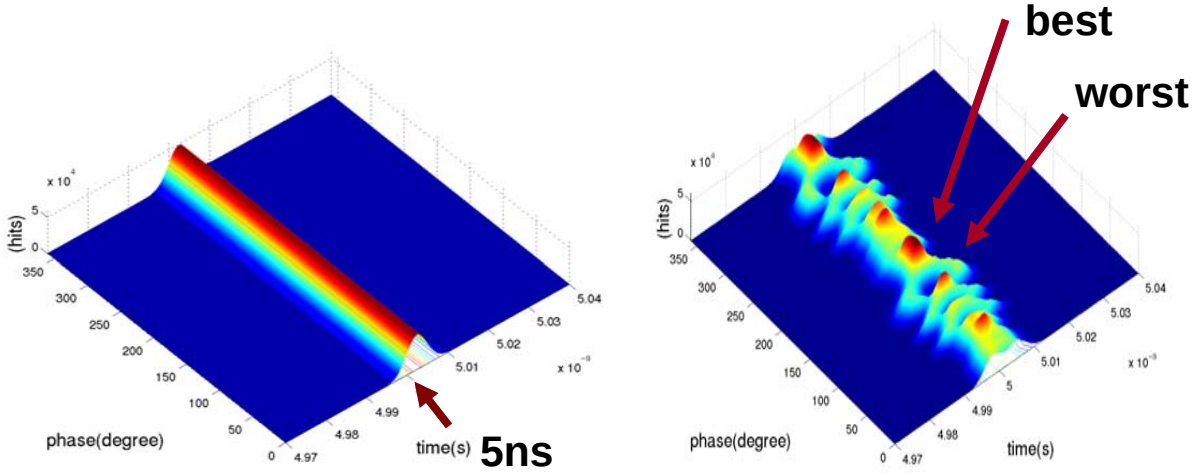




Test Vehicle

- 200MHz PLL* with Digital Noise Emulator (DNE)
  - TSMC .18µm generic logic process (TSMC CL018G)
- Period of the PLL output is measured and plotted as 3-D period histogram.

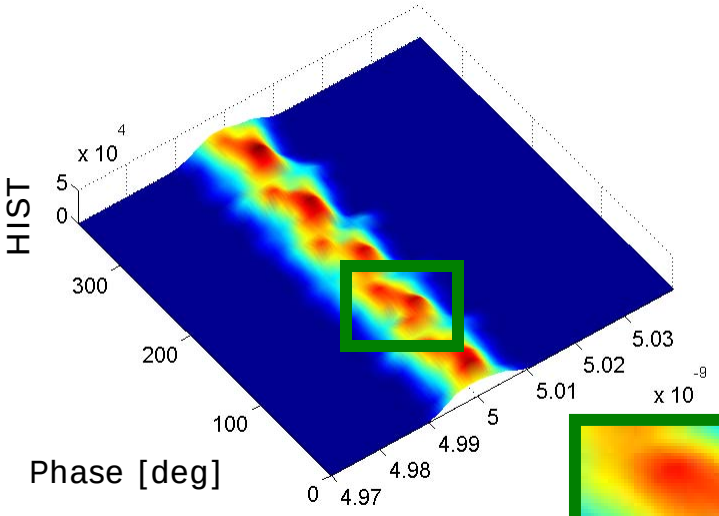




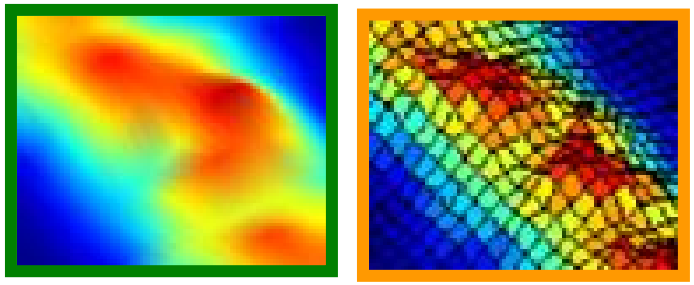
Measured 3-D plots of period histogram

*Designed by Barcelona Design

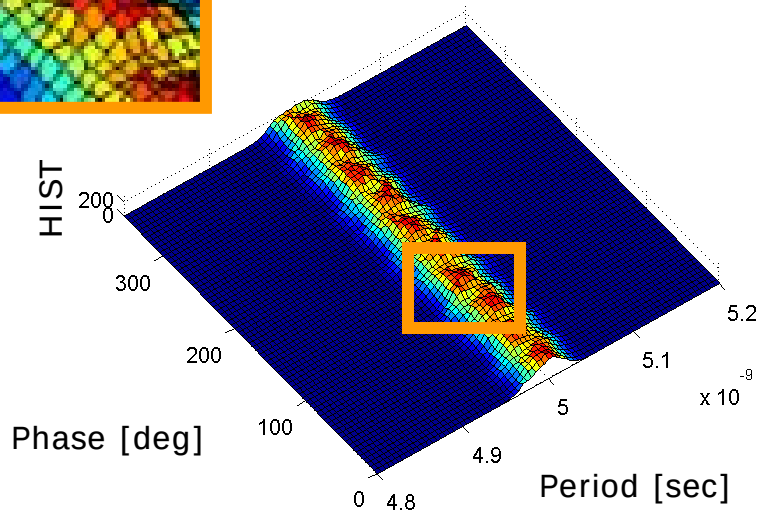
Comparison with Measurements
- 3-D Plot of period histogram



Measurement with 160MHz clock noise



Verilog-A Simulation with 160MHz clock noise plus random noise



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Conclusion

- **Impulse Sensitivity Function (ISF)** can be used as the behavioral model of the substrate noise coupling to VCO with a linear and time variant approach.
- **Two versions of Verilog-A** are utilized to implement the system level simulation and compared with the transistor level simulation (Hspice).
- Results from the system level simulation are compared with the measurement results in terms of the **period histogram**, showing good correlation.