Modeling of the diode with VHDL-AMS including reverse recovery

Lyse-Aline COYITANGIYE
LEMI
University of Rouen, IUT Rouen
76821 Mont-Saint-Aignan, France
lyse-aline.coyitangiye@univ-rouen.fr

Richard GRISEL
LEMI
University of Rouen, IUT Rouen
76821 Mont-Saint-Aignan, France
richard.grisel@univ-rouen.fr

ABSTRACT

A diode VHDL-AMS model is presented which can simulate the diode reverse recovery behavior. For VHDL-AMS to be useful to the analog design community, efficient semiconductor device model must be available. The model is based on the charge transport equations and they are simplified using the lumped-charge modeling technique. The model is demonstrated on the Advance-MS simulator.

1. INTRODUCTION

Circuit simulation is a technique employed to verify the intended operation of an electronic circuit prior to circuit construction. The process of simulation requires a language to describe the behavior of a circuit to be simulated and the description of the circuit itself. VHDL-AMS is one such language that supports the description of analog electronic circuits using Ordinary Differential Algebraic Equations (ODAEs) in addition to its support for describing and simulating discrete-event, analogue-mixed and multi disciplinary systems [5].

This paper presents the possibility to build a VHDL-AMS pn-junction diode model based on the physical lumped-charge technology[1].

2. PHYSICAL DEVICE MODELING

Physical device models are based on a description of carrier transport physics. They can be used to characterize the DC, transient and AC operation of devices, in addition to providing a detailed insight into the physical aspects of device operation. An important advantage of this type of model is that it can be used to predict the characteristics of new devices, based on a suitable description of the carrier transport mechanisms.

The study will be directed to the physics-based analytical modeling approach based on the lumped-charge technique developed by Lauritzen[1]. This methodology will be used to develop an extended model of simple p-n diodes. The goal is to establish a VHDL-AMS code for a p-n diode model that will be used to simulate physical behavior.

2.1. The lumped-charge modeling technique

We describe the lumped-charge (L-C) modeling technique used in the building of power semiconductor models for circuit simulators. The L-C approach represents an extension of the charge control and lumped model method introduced by Linvill in the early 1960's and was first used in the 1990's to develop compact models of power semiconductor devices. Here, we have referred to the Lauritzen-Ma lumped-charge diode model [1] that is suitable for power and non power diodes. The approach includes physics-based analytical modeling and has been developed to replace the standard SPICE models for accurate simulation.

In the L-C concept, distributions of charges that play a significant role in current flow are represented by one or more "lumps" or "packets" of charge at specific locations within the device. The lumps connect the input information using expressions from device physics. The L-C general assumptions are, typically, that in each lightly doped region, where injected charge carrier distribution and variation determine the device's static and dynamic characteristics, at least one charge-storage node and two connection nodes are needed. In the heavily doped regions, one charge node is necessary to serve as both the charge storage and connection node, since the special variation of carrier concentration is small [1]. The technique is based on the fundamental semiconductor equations which are applied to the lumped elements called nodes using the following guidelines. The charge nodes are linked using the following six physics equations:

- Current density equations;
- Current continuity equations;
- Charge neutrality equations;
- Boltzmann relations;
- Poisson equations;
- Kirchoff current and voltage laws.

The first five equations describe carrier distribution and transport between the charge nodes in the device. The last equation connects the internal variables of the model

equations to the terminal characteristics. The variables of the model stand for the charges and voltages

The lumped-charge diode model

In the model presented by C.Ma and P.Lauritzen [1] for a pin diode ($P^+N^-N^+$), a storage node and two connexion nodes are chosen in the lightly doped N^- region. The same technique can be applied to a pn-junction diode.

We consider two nodes 1 and 2 in the P and N regions respectively (Figure 1). Each node is both a charge storage node and a connexion node, assuming that the two regions are heavily doped regions. Physics equations can be written for the two lumped elements.

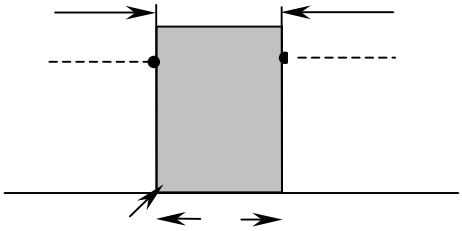


Figure 1. Location of the lumped-charge nodes.

Charge carrier transport at node 1 and node 2 is derived from the current density:

$$j_p = qp\mu_p E - qD_p \frac{dp}{dx} \tag{1}$$

The diffusion current equation in lumped-charge form is [4]:

$$i_{p12} = \frac{q_{p1} - q_{p2}}{T_n} \tag{2}$$

where $q_{p1} = qdAp_1$ and $q_{p2} = qdAp_2$

A is the device active area, d is the distance between nodes 1 and 2.

The carrier concentrations at the pn junction are related by the Boltzmann relations for electron and hole carriers :

$$p_{n0} = p_{p0}\exp\left(\frac{v_{12}}{\phi_t}\right) \quad , \quad n_{p0} = n_{n0}\exp\left(\frac{v_{12}}{\phi_t}\right) \tag{3}$$

where v_{12} represents the junction voltage

p_{p0} and n_{p0} is the thermal equilibrium hole and electron concentration in the N region.

The variation effects of the junction-depletion width under reverse bias voltage are described by the Poisson equation:

$$\frac{d^2v}{dx^2} = \frac{\rho(x)}{\varepsilon_s} \tag{4}$$

where v is the electrostatic potential, ρ is the space-charge density and ε_s is the semiconductor permittivity.

And the J1 junction-depletion width variation effects can be written as [1]:

$$l = \sqrt{\frac{2I_B(\phi_{12} - V_{12})}{\phi_B\left(1 + \frac{i_d}{I_B}\right)}} \tag{5}$$

where the constants : $\phi_B = qd^2n_{n0}/2\varepsilon_s$ and $I_B = qAn_{n0}v_{sat}$

ϕ_{12} is the built-in potential

Equation implementation

The pn diode model equations to be implemented are simple and are reduced to the following set [3]:

$$q_{p2} = Q_B\left(\exp\left(\frac{v_{12}}{\phi_t}\right) - 1\right) \tag{6}$$

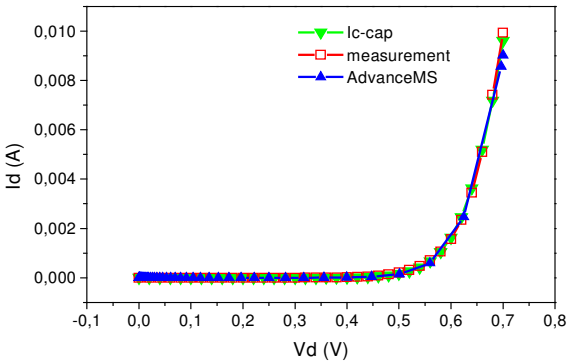
$$l = \sqrt{\frac{2I_B(\phi_{12} - V_{12})}{\phi_B\left(1 + \frac{i_d}{I_B}\right)}} \tag{7}$$

$$T_n = T_{n0}(1 - l)^2 \tag{8}$$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_{12}}{\phi_t}\right)^{1/2}} \tag{9}$$

Equation (6) is the pn junction equation, where parameter $Q_B = qlAn_{n0}$ represents the thermal equilibrium electron charge in the N region. Equations (7) and (8) are the Poisson equations and account for J1 junction-depletion width. Any variation of the charge within a p-n diode with an applied voltage variation yields a capacitance which must be added to the circuit model of a p-n diode. Equation (11) represents the depletion layer capacitance where parameter C_{j0} is the zero bias-capacitance.

Test verifications have been done on a rectifier diode 1N4004. Measurements of D-C and C-V characteristics are compared with AdvanceMS and Ic-cap(Spice simulator) simulations on Figure 2. The model parameters are extracted from simple DC measurements as have been proposed by C. Ma and P.Lauritzen in [1]. D-C and C-V SPICE parameters are extracted using Ic-cap simulator. Note the excellent match between simulation and measurement results.



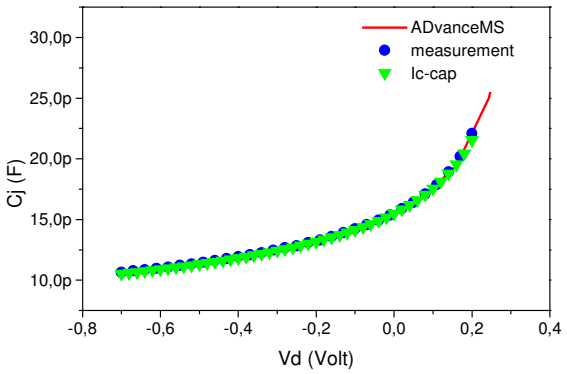


Figure 2 . D-C (upper) and C-V (lower) simulated and measured characteristics of a diode

VHDL-AMS REVERSE RECOVERY DIODE MODEL

3.1. Turn off transient: reverse recovery

In the case of bipolar devices, the recombination lifetime of minority carriers injected across pn junctions plays a key role in determining device performance.

When a diode carrying a steady forward current is suddenly reverse biased, it will not response to the reverse voltage until the excess electrons and holes stored in the neutral n and p region have been withdrawn.

Consequently, on application of reverse bias, the diode will pass a reverse current higher than the saturation current for some times [4]. The current then starts to falling as the stored charge of excess carriers is withdrawn, eventually reaching its reverse saturation value. The way in which the stored charge is removed depends on the source impedance of reverse drive.

3.2. Parameter extraction

Lauritzen and Ma introduced reverse recovery parameters and the extraction methodology. These parameters are T_1 the length of the turn-off period, I_{RM} the maximum reverse current, and T_{rr} the time constant of the decay tail. Equation (11) relates T_{rr} to the two dynamic parameters, lifetime τ and electron transit time T_n.

The reverse recovery current I_{RM} is the peak current overshoot. The reverse recovery time, T_{rr} is the time taken from I_{RM} to decay away to 25% of its peak value. The parameters τ and T_n are calculated from equations (10) and (11) [7]:

$$I_{RM}=a(\tau-T_{rr})\left[1-\exp\left(\frac{T_1}{\tau}\right)\right] \quad (10)$$

$$\frac{1}{T_{rr}}=\frac{1}{\tau}+\frac{1}{T_n} \quad (11)$$

$$Q_{rr}=\int_{i(t)<0} i(t) \quad (12)$$

where $a=-\frac{di}{dt}=\frac{V_{IN}}{L}$ represents the turn-off slope.

For simulating the reverse recovery, an inductor is connected in series with the pn diode (Figure 3) and the input voltage is stepped from a forward bias to a reverse bias.

Experimental reverse recovery data for the inductive turn off of a pn diode (1N4004) is shown in **Erreur ! Source du renvoi introuvable.**. The diode was chosen because its nominal reverse recovery time of 10µs can be easily observed during test. The data demonstrates the presence of oscillations during the turn-off process in addition to the larger oscillations at the end of the turn-off process. The oscillations are due to the charge and discharge of the depletion-region capacitance [2] and are modeled by a capacitor in series with conductance and resistor.

Figure **5** shows measured and simulated with Advance-MS reverse recovery current waveforms. The results shows the good functionality of the proposed model and suits the measurement data.

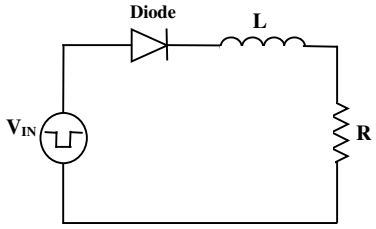


Figure 3 : A test circuit used for verification

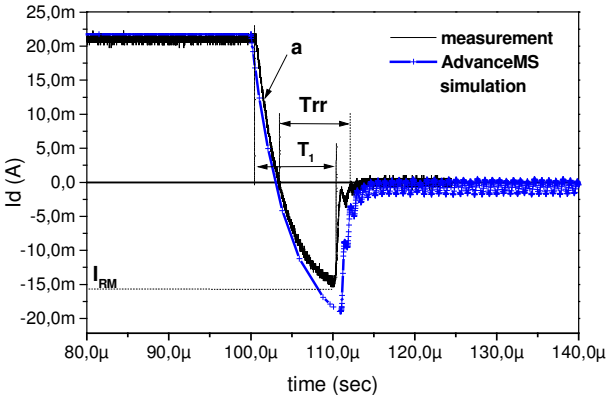


Figure 4: measured and simulated reverse-recovery current waveforms of 1N4004

3.3. Removal of excess charge

The total charge Qrr can be calculated from equation (12) by integration of the reverse current.

Figure **5** represents the reverse recovery charge, the charge decrease during the reverse recovery and become zero at the turn off step.

The charge-control expression (13) of the diode current is derived from the continuity equation and leads to the excess charge relation (14):

$$i(t)=\frac{dQ(t)}{dt}+\frac{Q(t)}{\tau} \quad (13)$$

$$Q(t)=2\tau\frac{V_{IN}}{R_L}e^{-\frac{t}{\tau}}+\tau\frac{V_{IN}}{R_L} \quad (14)$$

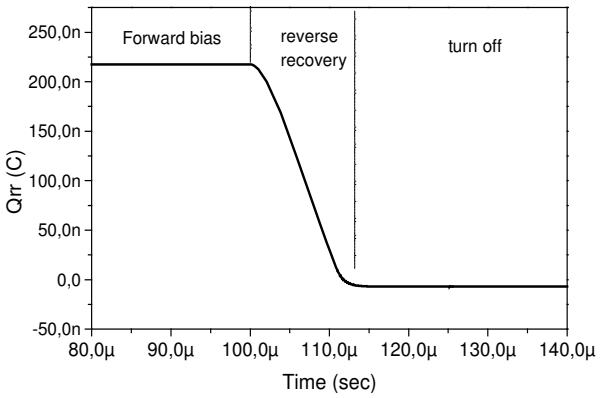


Figure 5 : Simulation of the excess charge removal (reverse recovery charge)

4. CONCLUSION

A simple diode lumped-charge model described in VHDL-AMS has been implemented in the ADvanceMS simulator for analogue and mixed signals. This work has presented a VHDL-AMS diode model where the reverse recovery phenomena have been taken account using the lumped charge approach. The general lumped-charge model for pin diodes can be extended to simple pn junction diodes**.** Understanding of the pn junction is essential to semiconductor device modeling. Physical parameters can be simulated and no statements are needed to define regions over which specific equations are valid.

VHDL-AMS can accurately simulate reverse recovery current. This work has attempt to exploit the features of the language.

5. ACKNOWLEDGMENTS

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