

An Extended SVD-based Terminal and Model Order Reduction Algorithm

Pu Liu, Sheldon X.-D. Tan, Boyuan Yan, Bruce McGaughy [†]

Department of Electrical Engineering, University of California, Riverside, CA 92521

[†] Cadence Design Systems Inc., San Jose, CA 95134

ABSTRACT

The paper proposes a new combined terminal and model order reduction method for compact modeling of interconnect circuits. The new method extends the existing SVDMOR method [3] by using higher order moment information for terminal responses during the terminal reduction and by applying separate SVD low-rank approximations on input and output terminals respectively. This is in contrast to SVDMOR method where input and output terminal responses are SVD approximated at the same time, which can lead to large error when the numbers of inputs and outputs are quite different. We analyze the passivity requirement for combined terminal and model order reduction and show the passivity enforcement may significantly hamper the terminal reduction effects. We also improve the computation efficiency of SVDMOR. Our experimental results show that ESVDMOR outperforms the SVDMOR in terms of accuracy for the similar reduced model sizes in a number of interconnect circuits when the input and output terminals are different.

1. INTRODUCTION

Compact modeling of passive RLC interconnect circuits by model order reduction (MOR) techniques has been intensively studied in the past due to the urgent need to reduce the increasing circuit complexity. The most efficient and successful algorithms are based on Krylov subspace projection [8, 2, 9, 6, 4].

But existing MOR methods mainly focus on the reduction of the internal nodes. When there are many terminal nodes, the efficiency of the existing Krylov subspace methods will degrade significantly. There are several reasons for the low efficiency. First, the time complexity of PRIMA [6] is proportional to the number of terminals of the circuits as moments excited by every terminal need to be computed and matrix-valued transfer functions are generated. Second, the poles of the reduced models are linearly increasing with the number of terminals, which make the reduced models much larger than necessary.

One way to mitigate this problem is by means of combined terminal reduction and model order reduction. Terminal or port reduction is to reduce the number of terminals/ports of given circuits under the assumption that some terminals are similar in terms of their timing information. Such similar terminals are justified by the facts that many terminals are indeed close to each other structurally. So their timing responses are similar also. Several terminal reduction algorithms has been proposed recently [1, 3, 5]. Method proposed in [1, 3], called SVDMOR, are based on the low-rank approximation of input and output position matrices before the model order reduction process. The low-rank approximation can be carried out on the DC [1] or a specific order of moments of responses [3]. However, our experimental re-

sults show that SVDMOR does not perform well when the input and output terminals are quite different. The SVD approximation is performed on the block moment matrix, which represent the response for both input and output terminals at the same time. So the approximation will not work well when the numbers of inputs and outputs are different dramatically. Basically the low-rank approximation or the number of independent terminals may not be same for both input and output terminals. This typically happens when the numbers of input and output terminals are quite different. This maybe the case for clock networks/meshes where you have a few driver (inputs) and many sinks (outputs).

Terminal reduction by SVD-based rank computation and terminal clustering via K-means method on terminal timing was proposed in [5]. The clustering is based on the higher order timing information. The method uses representative terminals to represent the reduced terminals. This method is very suitable for circuits with separate input and output terminals. But this method loses the timing difference between the representative terminals and their suppressed terminals.

In this paper, we propose a new SVD-based terminal reduction algorithm, called Extended SVDMOR or ESVDMOR method. Our approach is based on the SVDMOR method [3]. But the new method uses higher order moment information during the SVD approximation process to ensure that we can find the true numbers of independent input and output terminals. Also the ESVDMOR performs the SVD on input and output moment responses separately so that they can approximate the input and output responses better when they are different. Experimental results show that ESVDMOR outperforms SVDMOR in terms of accuracy under same or similar reduced model sizes when the input and output terminals are quite different.

The paper is organized as follows. In section 2, we review the SVDMOR method for model reduction with large number of terminals and show its weakness with experimental results. Section 3 presents our new ESVDMOR method. We first present main idea of the new terminal reduction method. Then we show how higher order moment information is represented for input and output terminal responses. After that we discuss some practical issues associated with the implementation, and present the whole terminal reduction and model order reduction flow of ESVDMOR. We also present a short discussions on the passivity issue in terminal reductions 4. The experimental results and conclusions are presented in section 5 and section 6, respectively.

2. REVIEW OF THE SVDMOR METHOD

In this section, we briefly review the SVDMOR method for terminal reduction, which was proposed recently for reducing the terminals of interconnect circuits [1, 3].

For a linear RLC interconnect network with p input and

q output terminals, we can apply Modified Nodal Analysis to formulate it into the state space equation form

$$\begin{aligned} G\dot{\mathbf{x}}(t) + C\ddot{\mathbf{x}}(t) &= B\mathbf{u}(t) \\ \mathbf{y}(t) &= L\mathbf{x}(t), \end{aligned} \quad (1)$$

where $G \in R^{n \times n}$ and $C \in R^{n \times n}$ are the conductive and storage element matrices. $L \in R^{q \times n}$ and $B \in R^{n \times p}$ are the output and input position matrices. $\mathbf{y}(t) \in R^q$, $\mathbf{u}(t) \in R^p$. State variables $\mathbf{x}(t) \in R^n$ can be nodal voltages or branch currents of the linear circuit.

The circuit transfer function is

$$H(s) = L(G + Cs)^{-1}B. \quad (2)$$

Then the i th block moment of the system is defined as

$$\mathbf{m}_i = L(-G^{-1}C)^i G^{-1}B, \quad (3)$$

which is a $q \times p$ matrix function.

The block moment \mathbf{m}_i can be directly computed in a recursive way

$$\begin{aligned} \mathbf{x}_0 &= G^{-1}B; \mathbf{m}_0 = L\mathbf{x}_0 \\ \mathbf{x}_1 &= -G^{-1}C\mathbf{x}_0; \mathbf{m}_1 = L\mathbf{x}_1 \\ \dots & \\ \mathbf{x}_i &= -G^{-1}C\mathbf{x}_{i-1}; \mathbf{m}_i = L\mathbf{x}_i \text{ for } i > 0, \end{aligned} \quad (4)$$

SVDMOR basically exploits the fact that many terminals are not independent in terms of their timing information, which can be reflected in their frequency domain moments. As a result, we can perform the singular value decomposition (SVD) on a block moment of specific order. For instance, if we perform the SVD on the 0th order block moment (DC response) \mathbf{m}_0 , we have

$$\mathbf{m}_0 = LG^{-1}B = U\Sigma V^T, \quad (5)$$

where U and V are orthogonal matrices and Σ is a diagonal matrix with singular values in the diagonal in a decreasing order. If there are k dominant singular values and we can use a k -rank matrix (a $k \times k$ full rank matrix) to approximate the original \mathbf{m}_0 based on the SVD theory as

$$\mathbf{m}_0 \approx U\Sigma_k V_k^T \approx U_k \Sigma_k V_k^T. \quad (6)$$

Notice that U_k is $q \times k$ matrix and V_k^T is a $k \times p$ matrix and Σ_k is a $k \times k$ matrix. After this, we can have the following expressions

$$B = B_b V_k^T, \quad (7)$$

$$L^T = L_c U_k^T, \quad (8)$$

where $B_b \in R^{n \times k}$ and $L_c \in R^{n \times k}$ are obtained using the Moore-Penrose pseudoinverse of V_k .

$$B_b = B V_k (V_k^T V_k)^{-1}, \quad (9)$$

$$L_c = L^T U_k (U_k^T U_k)^{-1}. \quad (10)$$

The circuit transfer function now becomes

$$H(s) = U_k L_c^T (G + Cs)^{-1} B_b V_k^T. \quad (11)$$

Notice that the transfer function $H_r(s)$, which is inside (11)

$$H_r(s) = L_c^T (G + Cs)^{-1} B_b, \quad (12)$$

is a $k \times k$ matrix transfer function, which actually is the terminal-reduced transfer function of (2) and can be reduced by the traditional Krylov subspace based model order reduction methods. If the reduced transfer function of (12) is $\hat{H}_r(s)$, then the final order reduced transfer function is

$$\hat{H}(s) = U_k \hat{H}_r(s) V_k^T. \quad (13)$$

SVDMOR performs the terminal reduction on the both input and output responses at the same time. This reflects

on the $q \times p$ block moment \mathbf{m}_i , where the column vectors of \mathbf{m}_i represent the i th moments from the p inputs and row vectors of \mathbf{m}_i represent the i th moments at the q outputs. The k -rank approximation in (6) can approximate well only one smaller-rank space spanned by either the column vectors or row vectors of \mathbf{m}_i . If two spaces have quite different ranks due to significant different numbers of input and output terminals, the approximation will not work well. This reflects the accuracy loss at the high frequency.

Fig. 1 shows the SVDMOR reduction results for a interconnect circuit, *net1026*, in frequency domain. This circuit has 6 inputs and 256 outputs. We perform both terminal reduction and following Krylov subspace based MOR. SVDMOR based on \mathbf{m}_0 reduces the terminals to only one input and one output terminals based on the singular values as shown in Table 2. From Fig. 1 we can see that results from SVDMOR are quite different from the original circuit at high frequencies (this is not due to model order reduction as will be shown in the experimental section).

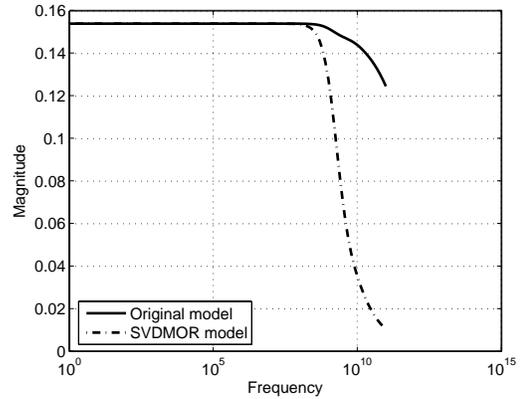


Figure 1: Frequency responses from SVDMOR method for *net1026* circuit.

Accuracy loss at high frequency after terminal reduction reflects the fact that the input and output terminals have different numbers of independent terminals. But SVDMOR can only approximate well one type of terminals as the SVD process is performed on the specific order of block moment matrix, which consists of both input and output terminal response information.

In the next section, we show how this problem can be mitigated by the new proposed ESVDMOR method using the higher order moment information.

3. THE NEW EXTENDED-SVDMOR METHOD

In this section, we present our new terminal and model order reduction algorithm, ESVDMOR. The basic idea of the new method is to perform the SVD low-rank approximation for the input and output terminals *separately* and use higher order moment information during the SVD approximation to find true terminal independency to ensure the accuracy of reduced model.

3.1 The New Terminal Reduction Algorithm

The main idea of the new terminal reduction method is to perform the SVD approximation on the input and output moment response *separately* with the use of high order moment information. We basically follow the terminal reduction framework of SVDMOR method [3] but with different moment matrices. But we improve the efficiency of SVDMOR by saving one computation steps as shown later.

The major problem for the SVD MOR method is that both input and output responses are considered at the same time during SVD due to the use of the specific order of block moments \mathbf{m}_i . So we can't accommodate higher order moment information. To mitigate this problem, we create new moment matrices for input and output terminals separately. In this way, we can use higher order moments during the SVD process for input and output responses.

Specifically, let's look at one specific moment block first. For a general linear system with p inputs and q outputs, each moment \mathbf{m}_i is a $q \times p$ matrix,

$$\mathbf{m}_i = \begin{bmatrix} m_{1,1}^i & m_{1,2}^i & \dots & m_{1,p}^i \\ m_{2,1}^i & m_{2,2}^i & \dots & m_{2,p}^i \\ \vdots & \vdots & \ddots & \vdots \\ m_{q,1}^i & m_{q,2}^i & \dots & m_{q,p}^i \end{bmatrix} \quad (14)$$

where each column j in \mathbf{m}_i represents the moment vector of all output terminals due to the input terminal j and each row k in \mathbf{m}_i represents the moment vector at the output terminal k due to all input terminals. Then a moment matrix, which consists of 0th to $(r-1)$ th order of block moments, can be written as

$$M = [\mathbf{m}_0 \quad \mathbf{m}_1 \quad \dots \quad \mathbf{m}_{r-1}]. \quad (15)$$

In order to perform terminal reduction for inputs and outputs separately, different moment matrices are constructed. Specifically for the output terminal reduction, we define the *output moment response matrix* M_O as:

$$M_O = \begin{bmatrix} \mathbf{m}_0^T \\ \mathbf{m}_1^T \\ \vdots \\ \mathbf{m}_{r-1}^T \end{bmatrix}, \quad (16)$$

where M_O is a $rp \times q$ matrix and each column j represents a moment series of output node j due to all input's impulse stimuli. Typically we expect the number of rows in M_O will be larger than the number of its columns so that the rank of the M_O is determined by the column vectors of M_O , which represents the q output terminals.

Similarly, for input terminal reduction, the *input moment response matrix* M_I is defined as:

$$M_I = \begin{bmatrix} \mathbf{m}_0 \\ \mathbf{m}_1 \\ \vdots \\ \mathbf{m}_{r-1} \end{bmatrix}, \quad (17)$$

where M_I is a $rq \times p$ and each column k represents a moment series at all output's nodes due to an input node k .

For both M_O and M_I , we require that the column vectors represents the responses for outputs and due to inputs respectively and the rows in both M_O and M_I will lose the terminal-related information as they represent the different orders of moments.

Next, we perform singular value decomposition to both input moment response matrix M_I and output moment response matrix M_O .

$$M_I = U_I \Sigma_I V_I^T \approx U_{I_{k_i}} \Sigma_{k_i} V_{I_{k_i}}^T, \quad (18)$$

$$M_O = U_O \Sigma_O V_O^T \approx U_{O_{k_o}} \Sigma_{k_o} V_{O_{k_o}}^T, \quad (19)$$

where Σ_{k_i} is a $k_i \times k_i$ diagonal matrix and k_i is the number of significant singular values for matrix M_I . $V_{I_{k_i}}^T$ is a $k_i \times p$ matrix. Similarly, Σ_{k_o} is a $k_o \times k_o$ diagonal matrix and k_o is the number of significant singular values for matrix M_O . $V_{O_{k_o}}^T$ is a $k_o \times q$ matrix.

Then we can perform the low-rank approximation for the input and output position matrix B and C respectively.

$$B = B_r V_{I_{k_i}}^T, \quad (20)$$

$$L = V_{O_{k_o}} L_r, \quad (21)$$

where $B_r \in R^{n \times k_i}$ and $L_r \in R^{k_o \times n}$ are obtained by computing the Moore-Penrose pseudoinverses of $V_{I_{k_i}}$ and $V_{O_{k_o}}$ respectively.

$$B_r = B V_{I_{k_i}} (V_{I_{k_i}}^T V_{I_{k_i}})^{-1}, \quad (22)$$

$$L_r = (V_{O_{k_o}}^T V_{O_{k_o}})^{-1} V_{O_{k_o}}^T L. \quad (23)$$

Notice that both $V_{I_{k_i}}$ and $U_{O_{k_o}}$ are orthonormal matrices, i.e. $V_{I_{k_i}}^T V_{I_{k_i}} = I$ and $U_{O_{k_o}}^T U_{O_{k_o}} = I$. Therefore, (22) and (23) can be further simplified as

$$B_r = B V_{I_{k_i}}, \quad (24)$$

$$L_r = V_{O_{k_o}}^T L. \quad (25)$$

So we save one computation step compared to the SVD MOR method [3].

As a result, the circuit transfer function now becomes

$$H(s) = V_{O_{k_o}} L_r (G + Cs)^{-1} B_r V_{I_{k_i}}^T. \quad (26)$$

Consequently we get a terminal reduced subsystem with transfer function $H_r(s)$.

$$H_r(s) = L_r (G + Cs)^{-1} B_r. \quad (27)$$

For this subsystem, the standard model order reduction techniques [8, 2, 9, 6, 4] can now be applied.

Consider both terminal and model order reductions, we can obtain the order reduced transfer function $\hat{H}_r(s)$,

$$\hat{H}_r(s) = \hat{L}_r (\hat{G} + \hat{C}s)^{-1} \hat{B}_r, \quad (28)$$

where

$$\begin{aligned} \hat{G} &= V^T G V; \quad \hat{C} = V^T C V \\ \hat{B}_r &= V^T B V_{I_{k_i}}; \quad \hat{L}_r = V_{O_{k_o}}^T L V \end{aligned} \quad (29)$$

where V is the projection matrix for reducing system of (27).

The final reduced transfer function becomes

$$\hat{H}(s) = V_{O_{k_o}} \hat{L} (\hat{G} + \hat{C}s)^{-1} \hat{B} V_{I_{k_i}}^T. \quad (30)$$

3.2 Practical Observation and Considerations

One important issue for the proposed method is to select the proper order of moments for the terminal reduction and for the model order reductions.

For the terminal reduction, our experimental results show that when the ranks of input and output moment response matrices are similar, SVD MOR typically performs well also. For the RC circuits tested in the experimental result section, we observe that the DC or first moments are typically sufficient for determining the ranks of input and output moment response matrices when they are similar. However, when the ranks of the input and output moment response matrices are different, higher order moment information can be useful for determining the true ranks of input and output moment response matrices, which typically happens when the input and output terminal numbers are quite different and SVD MOR does not perform well. In this case we need the high order moment information to compute the true ranks of the input and output moment response matrices separately.

Specifically, we use the following rule:

$$rp \geq q \text{ for } M_O \text{ when } q > p, \quad (31)$$

$$p \leq rq \text{ for } M_I \text{ when } p > q, \quad (32)$$

where r is the order of moments used. For M_O , if output terminal number q is larger than the input terminal number p , we need to add all moments up to $(r - 1)$ th order such that we have an equal or larger number of rows than the number of columns in M_O . This is true for M_I when the input terminal number p is larger than the output terminal number q . This determination process considers the worst case that all terminals are independent to others.

When $p = q$, r is set to 1 to satisfy (31) and (32). Under this condition, the higher order moment information is not necessary.

3.3 ESVD MOR Algorithm Flow

In this subsection, we give the whole combined terminal and model order reduction flow of the ESVD MOR method.

EXTENDED-SVD MOR ALGORITHM

1. Compute the block moments \mathbf{m}_i up to the $(r - 1)$ th order using (4).
2. Construct the input and the output moment response matrices defined in (17) and (16) respectively.
3. Perform the SVD-based low-rank approximation on the position matrices B and L in (1) using (24) and (25).
4. Perform the normal Krylov subspace based MOR on the terminal reduced system (27) and perform the transformations using (29).
5. Compute the final reduced system $\hat{H}(s)$ using (30).

4. PASSIVITY DISCUSSIONS

For model order reduction, the input and output position matrices B and L^T are required to be the same for ensuring passivity with projection based reduction. When B and L^T are not the same, passivity may not be ensured with existing projection methods. We notice that reduction by Truncation Balanced Realization (TBR) can make passive reduction of RLCK circuits with different B and L^T [7]. But passive TBR is a very expensive process and does not scale to solve large problems.

One may think that one can make all the terminals as bidirectional ones by making B and L^T equal. But we show in the experimental section, such a simple strategy for enforcing passivity may significantly reduce the terminal reduction qualities. One obvious reason is that many output terminals now become input terminals. So the responses excited by those terminals have to be considered for all the other terminals, which make the reduction more difficult and sometime impossible, which is evidently demonstrated by the full rank of the moment matrices in one example circuit.

Considering the terminal reduction, passivity further requires that B_r are L_r^T are the same and $V_{O_{k_o}}$ and $V_{I_{k_i}}$ are identical as well due to the requirements of the congruence transformation. As a result, the moments \mathbf{m}_i must be symmetric. This is required for both SVD MOR and ESVD MOR methods. It can be proved that when the inputs to the original models consist of only current sources or voltage sources for RLCK circuits, \mathbf{m}_i is symmetric. If both current and voltage sources are present, \mathbf{m}_i will not be symmetric and terminal reduction by both SVD MOR and ESVD MOR will not ensure the passivity.

In general, we observe that for efficient terminal reductions, the input and output terminals can not be bidirectional, which means B and L^T will be different.

5. EXPERIMENTAL RESULTS

The proposed method has been implemented in MATLAB. We tested our algorithm on a number of real industry interconnect circuits from our industry partner. For these

examples, We apply both SVD MOR and ESVD MOR terminal reduction methods along with Krylov subspace based model order reduction for internal node reduction. And we only consider the DC moment for the SVD MOR method.

The first example, *net27*, has 14 inputs and 118 outputs with model order of 182. Because there are more outputs than inputs, the number of the independent input terminals can be determined by using only DC moment as M_I . However, higher order moment information is needed to find the number of the independent output terminals. Here we use first 9 order block moments to construct the output moment matrix M_O , which considers the worst case that all the output terminals are independent to each other.

The singular values for \mathbf{m}_0 , which is used by SVD MOR, M_I , M_O are shown in Table 1. From the table we can see that we only need one input and one output terminal after terminal reduction by using SVD MOR method. By using M_I and M_O in the ESVD MOR method, we find that there are more than one dominant singular values of M_O . We choose one input and five outputs to make the reduced model more accurate.

Table 1: The singular values of DC moment, Input moment matrix and Output moment matrix of the circuit *net27*.

#	\mathbf{m}_0	M_I	M_O
1	5.1587	5.1587	19.828
2	3.9883×10^{-14}	3.9883×10^{-14}	4.4677
3	1.6681×10^{-14}	1.6681×10^{-14}	1.6517
4	-	-	0.3045
5	-	-	0.0348
6	-	-	2.4611×10^{-3}
7	-	-	1.6134×10^{-4}

To compare accuracy between the SVD MOR and ESVD MOR methods in a fair way, we make sure the reduced models for both algorithms have the same number of poles. If we use the same order of block moments, then more terminals will lead to more poles using the Krylov subspace MOR methods.

For circuit *net27*, 6 poles are used to approximate the original model for both SVD MOR and ESVD MOR methods. The results are shown in Fig. 2, which is the frequency responses corresponding to the second input and the 10th output.

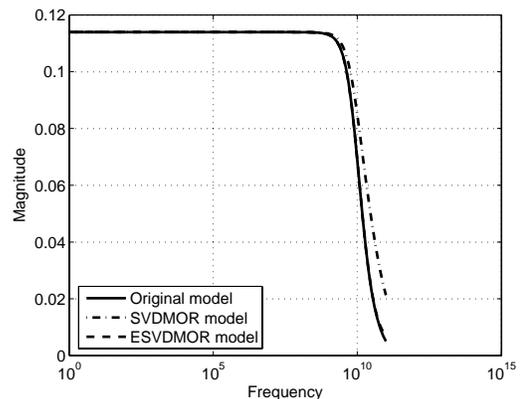


Figure 2: Frequency responses from SVD MOR and ESVD MOR for *net27* circuit.

From these frequency response results, we can see that our ESVD MOR model could match the original model up to 5GHz. In contrast, SVD MOR reduced model can only match frequency up to 500MHz. This clearly shows the advantage of the ESVD MOR over SVD MOR method when the input and output terminals have different dependency (different ranks in their moment responses matrices).

One may argue that we are more accurate since we use more terminals. Actually if we use five inputs and five outputs in SVD MOR method, the results are still not good comparing to our ESVD MOR method under the 6 poles. The results are shown in Fig. 3, where SVD MOR model #2 refers to the SVD MOR results with 5 input and 5 output terminals. So simply increasing the number of terminals in SVD MOR does not help to improve the model accuracy.

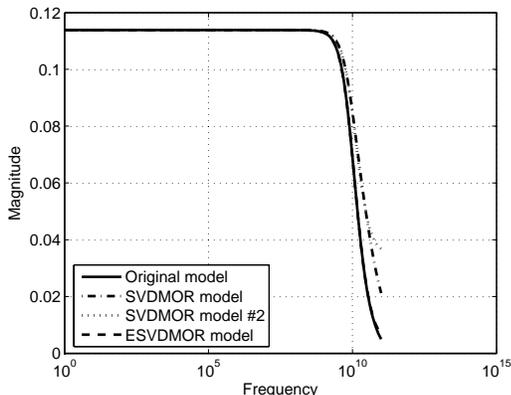


Figure 3: Frequency Response from SVD MOR and ESVD MOR with different terminals for *net27* circuit

The second example is circuit *net1026*, which has 6 inputs and 256 outputs with model order of 522. Since the number of output terminals is also larger than the number of input terminals, we use $r = 43$ order moments to construct the output moment matrix M_O . After we obtain the singular values as shown in Table 2, the terminal reduced subsystem for SVD MOR becomes a single-input and single-output (SISO) system, and the terminal reduced subsystem for ESVD MOR is a one-input and five-output (SIMO) system. We still use projection subspace based MOR with the same reduction order (5 poles) for both methods.

Table 2: The singular values of DC moment, Input moment matrix and Output moment matrix of the circuit *net1026*.

#	\mathbf{m}_0	M_I	M_O
1	7.5175	7.5175	2097.6
2	2.7376×10^{-15}	2.7376×10^{-15}	10.501
3	7.5742×10^{-16}	7.5742×10^{-16}	1.6625
4	-	-	0.12577
5	-	-	0.00134
6	-	-	8.278×10^{-6}
7	-	-	3.9216×10^{-8}

We choose the response between the first input and the first output and show the frequency domain response results in Fig. 4. This example have the similar situations with the first example: it has larger number of output terminals than the input terminals. As a result, input and output terminals have different numbers of independent terminals.

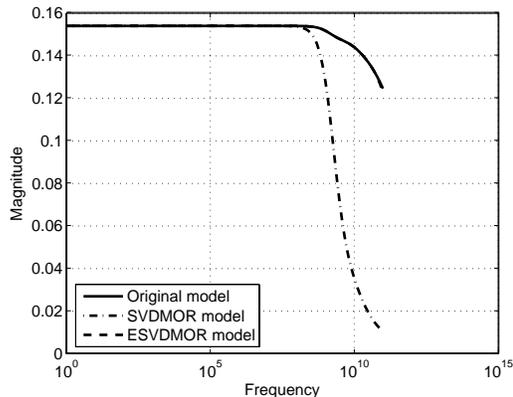


Figure 4: Frequency responses from SVD MOR and ESVD MOR for *net1026* circuit.

By just using one terminal for both input and output does not approximate well for the model order reduced system.

Again, if we use five inputs and five outputs for the SVD MOR model, the accuracy does not improve much as shown in Fig. 5(SVD MOR model #2).

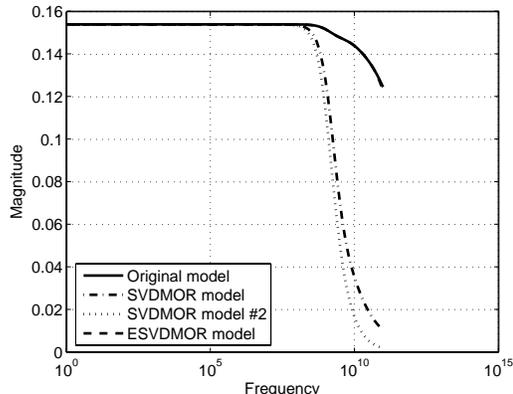


Figure 5: Frequency responses from SVD MOR and ESVD MOR with different terminals for *net1026* circuit.

To compare the terminal reduction effects when all the terminals are treated as bidirectional for *net1026* circuits, we list the singular value results with decreasing order after the SVD on the 0th and 1th moment matrices in Table 3:

From the Table 3, we can see that the singular values decay very slowly and the terminals can't be reduced very much. Actually the rank of the moment matrix \mathbf{m}_0 (given by Matlab rank command) is 261, which is close to the full rank of the moment matrix. And the rank of the moment matrix \mathbf{m}_1 is the full rank.

One obvious reason for this problem is that many output terminals now become input terminals. As a result, the responses due to those output terminals have to be considered during the terminal reduction process, which make the reduction process more difficult.

The third example is also a RC interconnect circuit, *net55*, which has 59 input terminals and 31 output terminals with model order of 187. Both the DC moment and the first moment are used to determine the number of independent inputs for the ESVD MOR method.

Table 4 gives the singular values for \mathbf{m}_0 , M_I , M_O . We notice that both M_I and M_O have the same ranks as \mathbf{m}_0 .