Average Behavioral Modeling Technique for Switched-Capacitor Voltage Converters

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ABSTRACT

This paper applies an average modeling technique to different types of switched-capacitor DC-DC converters, taking into account the circuit non-ideal parameters. An extensive set of experiments were carried out to test the validity of each model. The results show acceptable accuracy and simulation speed gain of several thousand times. This speed gain is achieved due to relaxation of the simulation timestep as opposed to traditional modeling and simulation techniques, where the simulator timestep is bound by the switching frequency. This modeling approach is most suitable for system level simulations where accuracy can be traded-off for speed.

1. INTRODUCTION

Complex systems today are becoming more and more mixed-signal, with the analog part being the design and verification bottleneck. While circuit-level simulation provides accurate results, it requires extensive computation over long time periods. Very often, however, speed is more critical than accuracy when simulations need to be repeated in order to identify key parameters in the design, or when the system needs to be simulated for a long time to gain enough insight of the operation and inter-functionality of the complete system. In such cases, a fast modeling technique is necessary where the optimal balance between simulation speed and accuracy may be achieved.

However, traditional behavioral models of some complex systems may still consume too much time during simulation. This may be due to high switching rates that slow down the simulation considerably, since the simulation time-step is bound by the switching period. In some cases, the actual information of interest is of a much lower frequency than the switching frequency.

An example of such circuits is the family of switched-capacitor DC-DC converters, also known as charge pumps. These circuits accomplish energy transfer and voltage conversion using capacitors and semiconductor switches [4]. Charge pump circuits provide a voltage that is a multiple or reverse polarity of the power supply voltage [13]. The two most common voltage converters are the voltage inverter and the voltage doubler circuits shown in Figure 1.

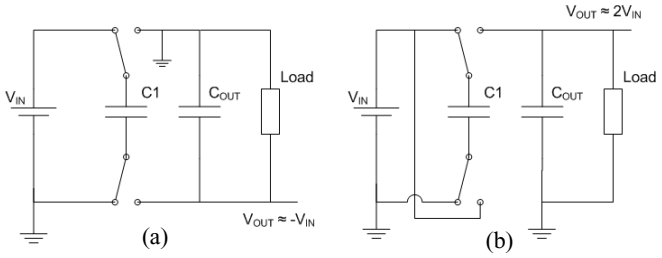

Figure. 1. Basic switched-capacitor circuits, (a) Voltage inverter, (b) Voltage doubler

In recent years, with the trend on low-power-low-voltage circuit design, switched capacitor voltage converters have become mandatory in power management ICs for battery powered portable applications [5] due to the many advantages they have over inductor-based switching regulators [3,10,14].

Our aim is to develop average models for these circuits that concentrate on the information bearing signal of lower frequency, thereby greatly relaxing the simulation time-step, and gaining the same information in a shorter time. These models may be useful for circuit design analysis and design parameter exploration, for circuit-based simulation, for obtaining engineering intuition into the operation of these switched circuits and for efficient execution of system level simulations [11].

Previous efforts to model switched-capacitor circuits include state-space averaging [10] and modified state-space averaging [3] techniques. However, the approach used in this paper to derive the average models is a much simpler one, and is based on the principle of conservation of charge and charge sharing between capacitors [2]. The resulting average models capture the effects of the circuit non-ideal parameters such as switch on resistance (R_{ON})and capacitor equivalent series resistance (R_{ESR}).

The paper is organized as follows. Section 2 describes the basic principle of operation of a charge pump voltage doubler. Then its equivalent average model is presented as proposed in [2]. Several experiments are carried out to test the validity of the average model proposed, by evaluating its speed and accuracy as opposed to a traditional circuit-level simulation. Our contributions appear in sections 3 and 4 where the charge pump inverter and push-pull doubler circuits are analyzed and their corresponding average models are derived. Each aver-

age model is tested under diverse simulation conditions to verify its validity and quantify the speed gain achieved. A conclusion is given in section 5 along with a proposal for possible future work.

2. CHARGE PUMP VOLTAGE DOUBLER

2.1. Basic Principle of Operation

Typically, there are two phases or states of operation [6] as illustrated in Figure 2.

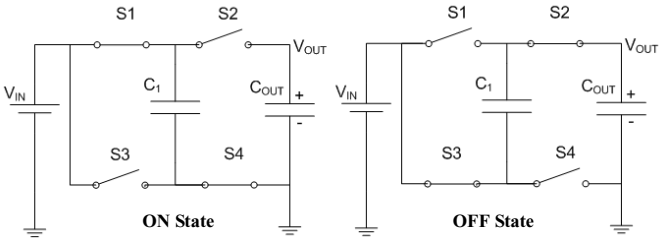

Figure. 2. Ideal voltage doubler circuit states of operation

In phase one, or the ON state, switches S1 and S4 are closed and S2 and S3 are open. In this phase, the capacitor C_1, also known as the flying or pump capacitor, is charged by V_{IN}. At the same time, C_{OUT} is discharged through the output load. In phase two, or the OFF state, S1 and S4 are open and S2 and S3 are closed. In this phase, the voltage on C_1 is discharged through C_{OUT} and the load, compensating the energy lost in C_{OUT} during the first phase. In other words, the two capacitors C_1 and C_{OUT} share charges during the second phase, where the amount of charge lost from C_1 is transferred to C_{OUT}. The final voltage V_{OUT} across C_{OUT} in the OFF state can be calculated using the following relation, where $V_{OUT\text{-}PREV}$ is the voltage across C_{OUT} from the previous state.

$$V_{OUT} = V_{OUT\text{-}PREV} + \left(\frac{C_1}{C_1 + C_{OUT}}\right)(V_{IN} + V_{C1} - V_{OUT\text{-}PREV}) \quad (1)$$

Figure 3 shows the converter operation for different output loads†.

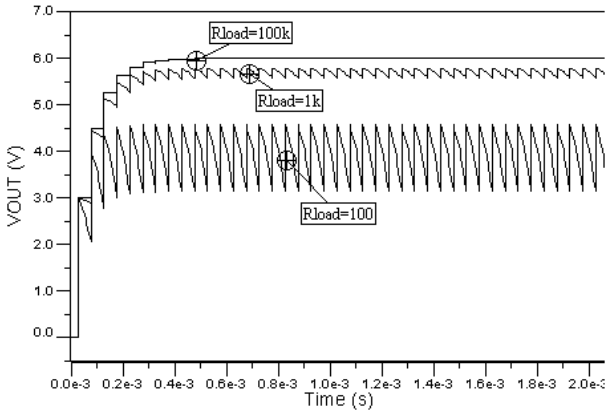

Figure. 3. Typical example of an ideal charge pump voltage doubler operation with varying output loads (V_{IN}=3V)

After initial start-up transient conditions are over and steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends on the load current and the switching frequency.

During the time the pump capacitor is charged by the input voltage, the output capacitor C_{OUT} must supply the load current. The load current flowing out of C_{OUT} causes a droop in the output voltage which leads to the appearance of output voltage ripple [9]. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching frequencies, which are generally limited to a few hundred kHz [15].

For a practical voltage doubler the switches will have finite on resistances (R_{ON}) and the pump capacitor will have an equivalent series resistance (R_{ESR}) as shown in Figure 4.

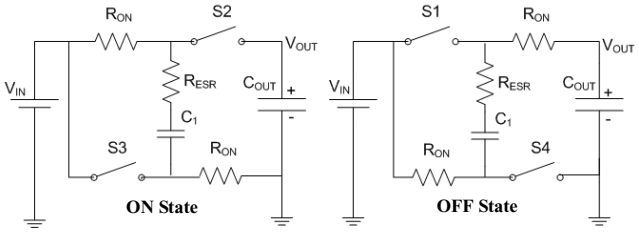

Figure. 4. Practical voltage doubler circuit states of operation

These resistances will prevent instantaneous voltage changes, corresponding to impulse currents, to occur on the capacitors at the switching edges [12]. Instead, these parasitics serve to limit the peak current and also increase the charge transfer time. Typical switch resistances can range from 1Ω to 50Ω, and R_{ESR} between 50mΩ and 200mΩ [15]. The relatively large switch resistance generally makes the final output voltage response overdamped, as illustrated in Figure 5.

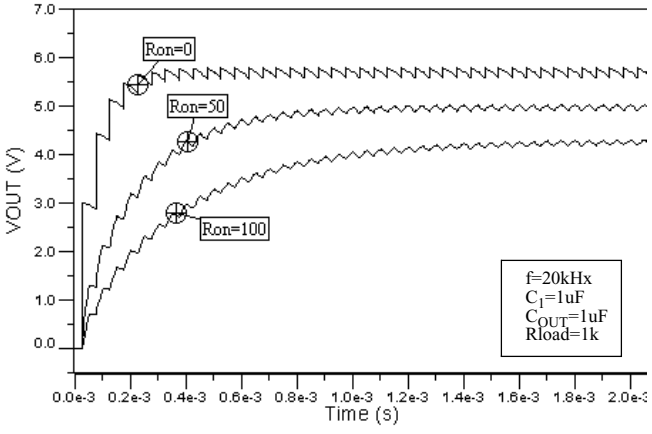

Figure. 5. Typical example of a non-ideal charge pump voltage doubler with different switch ON resistances (V_{IN}=3V)

† All simulations were carried out using Mentor Graphics mixed-signal simulation tool, ADVance MS™ [7]

2.2. Average Model

In order to save simulation time, the equivalent circuit in Figure 6, as proposed in [2], may be substituted for the real circuit. The equivalent circuit parameters are a function of the switching frequency (f), switching duty cycle (D), input supply voltage (V_{IN}), in addition to R_{ON}, R_{ESR} and C_{OUT}. The full detailed analysis and derivation of the equivalent circuit can be found in [2].

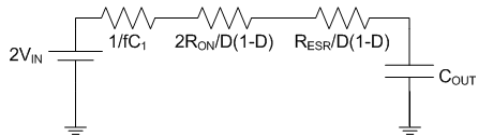

Figure. 6. Equivalent circuit of charge pump voltage doubler

This equivalent circuit will relax the simulation timestep greatly, and only the average information will be captured instead of the detailed transients and ripples of the actual circuit. This type of abstraction is useful in system-level simulations, enabling more efficient and, sometimes otherwise impossible, completion of simulation of the complete system.

2.3. Experiments and Results

To verify the validity of this average modeling approach, many simulations were carried out comparing a simple circuit-level description‡ (similar to Figure 4), with the average model††. The following simulation will be described as an example. In this simulation, the switching frequency was set to 20kHz, C_1=1µF, C_{OUT}=1µF and R_{ON}=R_{ESR}=0Ω. The output resistive load is varied during the simulation (100kΩ, 1kΩ and 500Ω). Figure 7 displays the simulation results. You can see how the behavioral model responds to the varying output load which is an important feature of DC-DC converters in general.

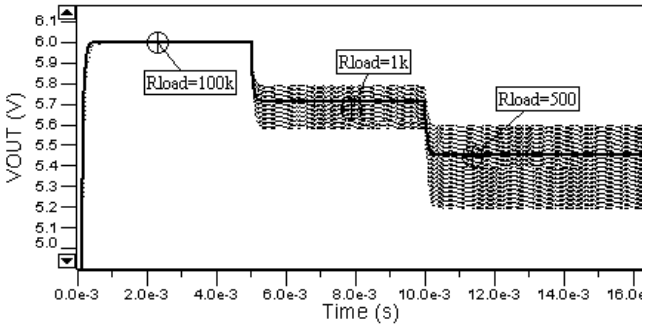

Figure. 7. Simulation of average voltage doubler model (solid line) versus actual circuit (dotted line), while varying the output load (V_{IN}=3V)

‡ The circuit-level description was implemented using switch macromodels and primitive elements from Mentor Graphics circuit simulator, Eldo™ [8].

††All behavioral models were developed using VHDL-AMS™. Any other analog or mixed-signal HDL would have been applicable.

The accuracy was determined by measuring the average value of the steady-state circuit simulation output voltage for each load (V_{OUT}) and comparing it with the average model output ($V_{OUT\text{-}AVE}$) at the same region. The error was measured using the following relation.

$$Error(\%) = (V_{OUT} - V_{OUT\text{-}AVE})/V_{OUT} \times 100\% \quad (2)$$

The accuracy of the behavioral model was almost 0% error for Rload=100kΩ, 0.3% for Rload=1kΩ and 0.5% for Rload=500Ω. The model was almost 4000 times faster when simulated for 10,000 switching cycles, where a single cycle corresponds to a single pair of ON and OFF states. Notice that this comparison was made for a very simple circuit representation. For a practical real-life circuit implementation, the circuit simulation would take much longer whereas the model simulation time will remain the same resulting in a much greater speed gain.

3. CHARGE PUMP VOLTAGE INVERTER

3.1. Basic Principle of Operation

Similar to the voltage doubler, there are two states of operation that are repeated periodically, as shown in Figure 8.

During the ON state, which is equivalent to the first half of the switching cycle, the charge pump capacitor, C_1, is charged to the input voltage. During the second half of the switching cycle, or the OFF state, its voltage is inverted and applied to the output capacitor and the load, leading to an output voltage that is negative the input voltage [15].

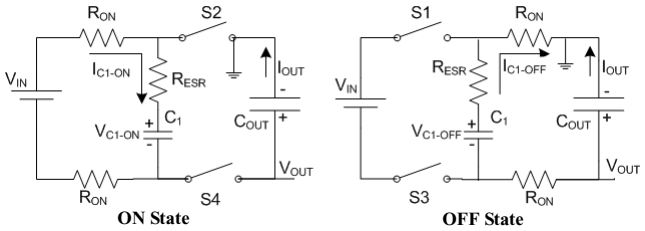

Figure. 8. Voltage inverter circuit analysis

In the following section we derive an average model for charge pump inverters.

3.2. Average Model

A very similar analysis as the one used for the voltage doubler circuit can be carried out to reach an average representation for the voltage inverter circuit. At steady state, the amount of charge flowing into C_1 during ON state is equal to the amount of charge flowing out of C_1 in the OFF state,

$$\Delta Q_{C1\text{-}ON} = \Delta Q_{C1\text{-}OFF} \quad (3)$$

$$I_{C1\text{-}ON\text{-}AVE} DT = I_{C1\text{-}OFF\text{-}AVE}(1-D)T \quad (4)$$

where D is the switching duty cycle and T is the switching period.

Also, the average output current can be represented by the weighted sum of the average ON and OFF output currents:

$$I_{\text{OUT-AVE}} = \frac{I_{\text{OUT-ON-AVE}}DT + I_{\text{OUT-OFF-AVE}}(1-D)T}{T} \quad (5)$$

The output is disconnected during the ON state therefore $I_{\text{OUT-ON-AVE}}$ is equal to zero. During the OFF state, the output current, $I_{\text{OUT-OFF-AVE}}$, is equivalent to $-I_{\text{C1-OFF-AVE}}$. Therefore, using (4) and (5) we get,

$$I_{\text{C1-OFF-AVE}} = -I_{\text{OUT-AVE}}/(1-D), \text{ and} \quad (6)$$

$$I_{\text{C1-ON-AVE}} = -I_{\text{OUT-AVE}}/D \quad (7)$$

By applying KVL to the circuit in Figure 8 during the ON state,

$$V_{\text{C1-ON}}(t) = V_{\text{IN}} - 2R_{\text{ON}}I_{\text{C1-ON}}(t) - R_{\text{ESR}}I_{\text{C1-ON}}(t) \quad (8)$$

And re-writing this equation in terms of average voltages and currents during the ON state,

$$V_{\text{C1-ON-AVE}} = V_{\text{IN}} - 2R_{\text{ON}}I_{\text{C1-ON-AVE}} - R_{\text{ESR}}I_{\text{C1-ON-AVE}} \quad (9)$$

Similarly for the OFF state,

$$V_{\text{C1-OFF-AVE}} = -V_{\text{OUT}} + 2R_{\text{ON}}I_{\text{C1-OFF-AVE}} + R_{\text{ESR}}I_{\text{C1-OFF-AVE}} \quad (10)$$

The difference in charge stored in C_1 between ON state and OFF state is equal to the net charge transferred to the output in one cycle

$$\Delta Q_{\text{C1-AVE}} = Q_{\text{C1-ON-AVE}} - Q_{\text{C1-OFF-AVE}} = C_1(V_{\text{C1-ON-AVE}} - V_{\text{C1-OFF-AVE}}) \quad (11)$$

Substituting Equations (9) and (10) in (11), we get:

$$\Delta Q_{\text{C1-AVE}} = C_1(V_{IN} + V_{\text{OUT}} - 2R_{\text{ON}}I_{\text{C1-ON-AVE}} - 2R_{\text{ON}}I_{\text{C1-OFF-AVE}} - R_{\text{ESR}}I_{\text{C1-ON-AVE}} - R_{\text{ESR}}I_{\text{C1-OFF-AVE}}) \quad (12)$$

Now, substituting Equations (6)and (7) in (12), we get,

$$\Delta Q_{\text{C1-AVE}} = C_1\left(V_{IN} + V_{\text{OUT}} + (2R_{ON} + R_{\text{ESR}})I_{\text{OUT-AVE}}\frac{1}{D(1-D)}\right) \quad (13)$$

Therefore the average output current,

$$I_{\text{OUT-AVE}} = -f\Delta Q_{\text{C1-AVE}} = -fC_1\left(V_{IN} + V_{\text{OUT}} + (2R_{ON} + R_{\text{ESR}})I_{\text{OUT-AVE}}\frac{1}{D(1-D)}\right) \quad (14)$$

Notice that the direction of the output current is opposite to that of the net charge flow in C_1.

By re-arranging (14) we get,

$$-V_{IN} - V_{OUT} = \left(\frac{1}{fC_1} + \frac{2R_{\text{ON}} + ESR}{D(1-D)}\right)I_{\text{OUT-AVE}} \quad (15)$$

This relation can be represented by the following average equivalent circuit:

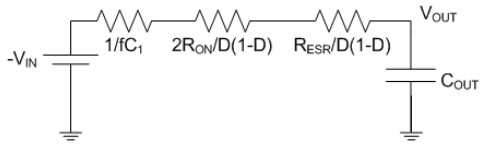

Figure. 9. Equivalent Circuit of Charge Pump Voltage Inverter

3.3. Experiments and Results

In order to verify the accuracy and validity of the derived average representation, we carried out the same set of simulations that were carried out for the voltage doubler. Figure 10 displays a sample of the simulations carried out.

In this simulation, the switching frequency was set to 20kHz, C_1=1µF, C_{OUT}=1µF and R_{ON}=R_{ESR}=0Ω. Again, you can see how the behavioral model responds to the varying output load during the simulation (100kΩ, 1kΩm and 500Ω). The accuracy of the behavioral model ranged between 0%-0.5%error using (2). The model was more than 4000 times faster when simulated for 10,000 switching cycles.

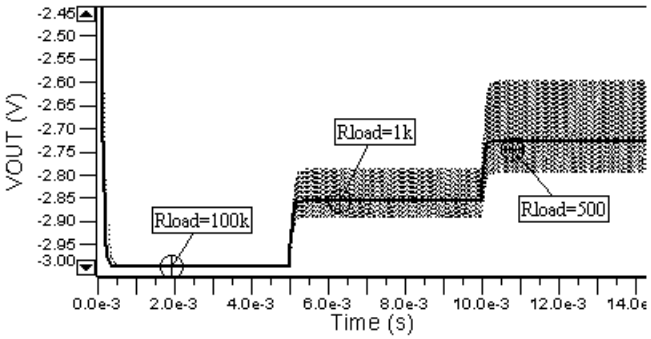

Figure. 10. Simulation of average voltage inverter model (solid line) versus actual circuit (dotted line), while varying the output load (V_{IN}=3V)

4. PUSH-PULL VOLTAGE DOUBLER

The term ”push-pull” refers to two charge pumps working in parallel and in opposite phase to deliver charge to support the output voltage. When one capacitor is pumping charge to the output, the other is recharging. This technique minimizes voltage loss and output voltage ripple.

4.1. Basic Principle of Operation

Two sets of switched-capacitor voltage doublers are connected in parallel delivering charge to the output as shown in Figure 11. The two voltage doublers run in opposite phases,

i.e., when one pump capacitor is being charged, the other is charging the output [1].

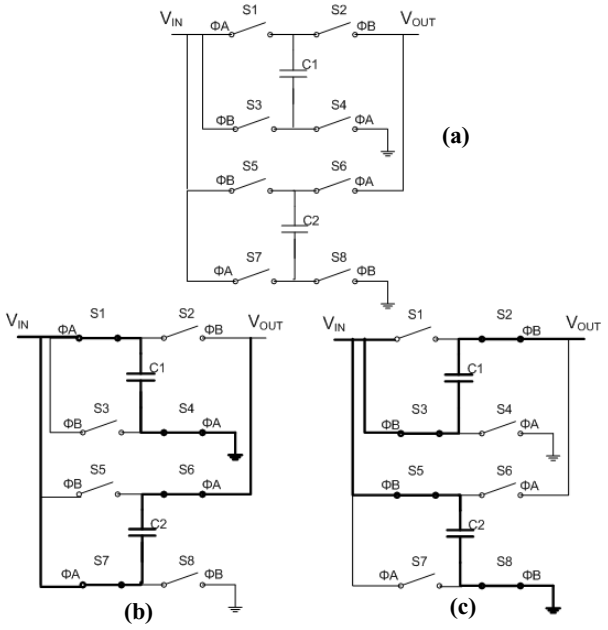

Figure. 11. (a) Ideal push-pull voltage doubler circuit, (b) Phase I, (c) Phase II

In this architecture one of the pump capacitors is always delivering charge to the output. As a result, output ripple is at a frequency that is double the switching frequency. This allows the use of a smaller output capacitor compared to a conventional voltage doubler. Figure 12 illustrates the difference in charge time, efficiency and output voltage ripple between the push-pull architecture and the conventional voltage doubler.

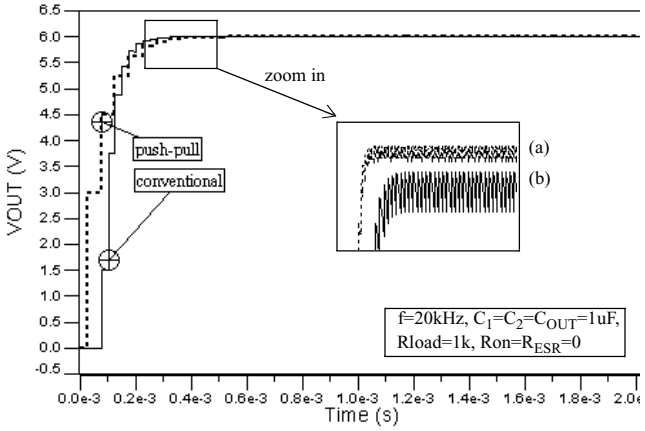

Figure. 12. Circuit Simulation of (a) ideal push-pull voltage doubler, versus (b) conventional voltage doubler

4.2. Average Model

As described in the previous section, the push pull architecture can be considered as two conventional charge-pump voltage doublers working in parallel. This inspired us to modify the average equivalent circuit that was shown in section 2.2 by adding an additional parallel branch to the model.

$$2V_{\text{IN}} - V_{\text{OUT-AVE}} = \left(\frac{1}{f(C_1 + C_2)} + \frac{2R_{\text{ON}} + R_{\text{ESR}}}{2D(1-D)}\right) I_{\text{OUT-AVE}} \quad (16)$$

This will have an effect of lowering the equivalent total resistance between input and output which will lead to a faster charging time of the output capacitor and improved efficiency of the voltage doubler, which is the major advantage of this architecture over the conventional voltage doubler.

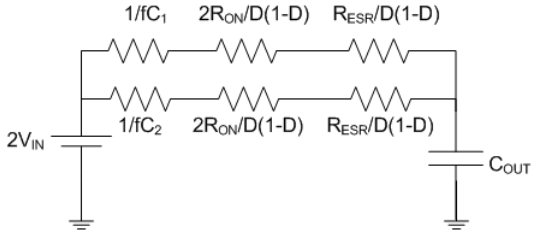

Figure. 13. Equivalent circuit of push-pull charge pump voltage doubler

The same systematic analysis that was carried out for the derivation of the average models of the voltage doubler and inverter circuits could be applied here to obtain the same resulting average equivalent circuit.

4.3. Experiments and Results

The following experiments were carried out to verify the accuracy and region of validity of the derived average representation. A simple circuit-level push-pull voltage doubler circuit (similar to Figure 11), and its corresponding average model were simulated and compared. The output resistive load was varied over three different values (100kΩ, 1kΩ and 500Ω), and the value of the switch ON resistance was swept over four values (0Ω, 10Ω, 50Ω and 100Ω). All different combinations of Rload and R_{ON} were simulated at 2 different switching frequencies (20kHz and 250kHz). Figure 14 displays a sample of the simulations carried out.

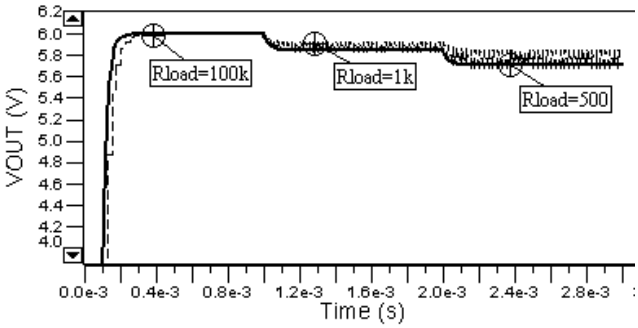

Figure. 14. Simulation of average push-pull voltage doubler model (solid line) versus actual circuit (dotted line), while varying the output load (V_{IN}=3V, f_{CLK}=20kHz, C_1=C_2=1μF, R_{ON}=0)

Tables 1 and 2 illustrate the simulation results in terms of output voltage error (using equation (2)), between the average model and the circuit-level simulation for different parameter combinations, for both switching frequencies.

Table 1. Results in terms of error (%) for f_{CLK}=20kHz

Rload	R_{ON}=0	R_{ON}=10	R_{ON}=50	R_{ON}=100
100k	0.007	0.0167	0.023	0.025
1k	0.6	1.6	1.9	1.9
500	1.2	2.3	3.7	3.3

Table 2. Results in terms of error (%) for f_{CLK}=250kHz

Rload	R_{ON}=0	R_{ON}=10	R_{ON}=50	R_{ON}=100
100k	0	0.0017	0.0017	0.0017
1k	0.05	0.19	0.18	0.17
500	0.1	0.37	0.31	0.28

The simulations were very accurate with errors less than 4% over a wide range of parameters. The error reaches the maximum for the extreme case of very low output resistance and large values of R_{ON}. The model accuracy increases as the switching frequency increases, where the converter output voltage exhibits smaller voltage droop during the OFF state. The model is around 4500 times faster when simulated for 10,000 cycles. Again, a comparison with a real-life push-pull transistor level circuit will exhibit a much larger speed gain.

5. CONCLUSION

We have presented an average modeling technique for switched capacitor voltage converters. Average modeling is beneficial when the nature of the circuit includes two frequencies, a high frequency corresponding to the switching frequency, and a lower frequency, which conveys the information of interest. The average modeling technique focuses on the lower frequency, and discards the detailed analysis of the high frequency component, leading to a much smaller number of simulation timepoints and therefore a much faster simulation. The developed models can be implemented using any analog HDL and are used to study the behavior of such circuits and perform faster system simulations. The models capture the circuit non-idealities such as capacitor R_{ESR} and switch ON resistance. We have verified that the developed models match the circuit-level simulations faithfully over a wide range of switching frequencies and circuit parameters. The models provide a speed gain of several thousand times when compared to a simple circuit.

Future work may include comparing the average models derived in this paper to other average models using different averaging techniques as described in [3, 10]. Also, a real-life circuit may be used to give a better idea of the speed gain and accuracy of the proposed modeling methodology.

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