A New Approach for Modeling the Nonlinearity of Analog to Digital Converters Based on Spectral Components

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ABSTRACT

This paper presents a novel modeling approach for analog to digital converters (ADCs). The non linearity of the converter is modeled using a linear combination of Chebyshev polynomials. The model relies on a Fast Fourier Transform (FFT) test applied to the output of the ADC. The harmonics extracted from the FFT test are the coefficients of the Chebyshev polynomials. The model appears to be much faster, compared to real circuits and models developed with other techniques, without losing much accuracy. The proposed model is convenient for all architectures of ADCs with high resolution bits.

1. INTRODUCTION

Analog and mixed-signal systems are now becoming increasingly complex and require longer simulation times. Using behavioral models, whether in top-down design or bottom-up verification, is becoming more popular because it reduces the simulation time of such systems while maintaining a reasonable level of accuracy.

Analog to Digital Converters (ADCs) are considered as an important component of mixed-signal systems since they interface the analog part of the design to the digital portion. Understanding the functionality of ADCs with the associated integral nonlinearity (INL) is of major interest to designers. The INL is defined as the deviation of the transfer function of the ADC from the ideal straight line [4]. In other words, the INL describes the nonlinear characteristics of the converter.

The aim of this paper is to present a new efficient modeling approach for analog to digital converters taking into account the INL. The INL is modeled using Chebyshev polynomials. The resulting behavioral model is independent of the ADC architecture, and is suitable for all ADC types. The model is useful for bottom-up verification of ADC circuits and can be used in larger system simulations.

We first present in Section 2 some of the different approaches used for ADC modeling. In Section 3 we present the proposed modeling approach based on the theory of the "Chebyshev test" that will be used to evaluate the *average* dynamic characteristics of the ADC. Section 4 presents some simulation results including comparisons between real circuits and different modeling approaches for ADCs with the new proposed modeling solution. A conclusion follows in Section 5.

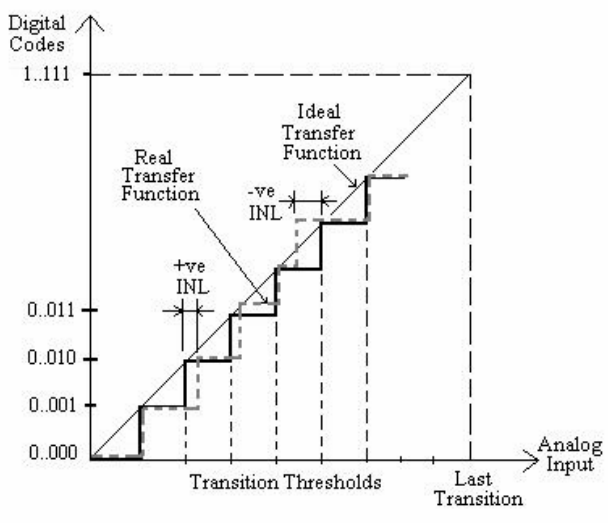

Figure. 1. Transfer function of ADCs showing the INL

2. ADC MODELING

The behavior of any device refers to the input-output characteristics and the response of the device in different domains (time domain, frequency domain, ...etc). A behavioral *model* of a component can be specific for certain domains, or it can suit all types of simulations. The main issue for ADC modeling is determining the *nonlinear* input-output transfer function. An accurate model should imitate the real circuit showing the deviation of the real device from an ideal response.

For a converter with "N" resolution bits, the input is divided into (2^N-1) transitional thresholds. These thresholds show the different input ranges that give different digital codes. The smallest analog increment the converter can resolve is evaluated as $(Inputfullscale/2^N)$ and expressed in terms of "LSB" (Least Significant Bit). In other words, it is the minimum change in the input that causes a change in the output [3]. The full scale input of an ADC is the maximum voltage that can be applied at the input.

Figure 1 shows the transfer function of an ADC illustrating the INL. The horizontal axis represents the analog input volt-

age with the different thresholds the converter can resolve. The vertical axis shows the corresponding output digital code. In the same figure, the solid staircased line shows the ideal transfer function of the converter and the solid straight line is a representation of the transfer function. The dashed staircased line is an example of a transfer function of a non ideal ADC. At every transitional threshold the horizontal difference between the dashed staircased line and the representation of the ideal transfer characteristics is the INL.

The difference between the thresholds is the value of the quantization. Due to the finite length of the digital output, there is always a quantization error. The quantization noise power is evaluated as [3]:

$$\text{Quantization Noise Power} = \frac{Q^2}{12} \quad (1)$$

where,

$$Q = \frac{Inputfullscale}{2^N} \quad (2)$$

It can be seen that for high resolution converters i.e. high values of "N", the quantization noise value is much less than that of low resolution ADCs.

One approach for ADC modeling found in the literature depends on the structure of the converter itself. The main modeling effort consists in building behavioral models for the building blocks of the ADC. This approach is illustrated in [1][9]. In this approach, the models typically show the imperfections of every individual block constructing the ADC. All modeled imperfections contribute to the overall nonlinearity of the converter.

An alternate approach is to model the analog to digital converter as a whole [1]. Some models based on this approach require the user to provide the INL value at every input threshold i.e. (2^N-1) different numbers. For a high number of resolution bits, this is a monumental task (65,535 parameters in case of a 16 bit ADC). Other models generate a random INL error based on a maximum number given by the user, this error is then added to the input thresholds. These models are computationally extensive and since they generate the INL randomly, they do not reflect a proper level of accuracy. In the following section, we present a new modeling approach based on formulating the INL as a polynomial.

3. A NOVEL MODELING APPROACH

Considering the nonlinearity of any converter, the value of the INL in terms of LSB versus the input voltage is illustrated as the highly fluctuating line in Figure 2. The proposed model evaluates the average value of the INL using a polynomial. This average value is shown as the smooth thick line in Figure 2.

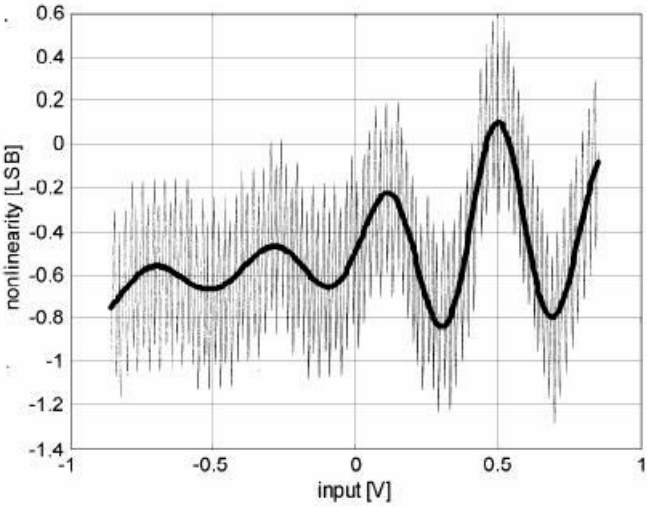

Figure. 2. A general figure for the INL of an ADC chip [5]

Describing the well-known staircase transfer function of the ADC as a polynomial requires a large number of terms. So, it is useful to decompose the nonlinear staircase function to the cascade of a smooth nonlinear block and an ideal quantization block [5]. This is shown in Figure 3.

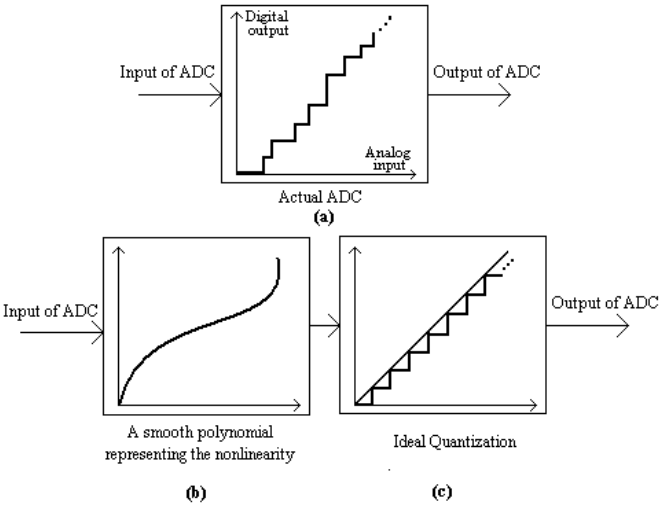

Figure. 3. The decomposition of the transfer function of the ADC. (a) The nonlinear actual transfer function of the ADC. (b) The smooth polynomial block. (c) The ideal quantization block.

Consider the actual transfer of the ADC as *g(x)* and the quantization block *as quant()* and the smooth polynomial as $g_s(x)$. The cascade of the decomposed blocks is formulated as [5]:

$$quant(g_s(x)) = g(x) \quad (3)$$

The proposed modeling approach presented in this paper relies on the theory of the "Chebyshev test" for generating the unique polynomial describing the non linearity of a given ADC.

3.1. The "Chebyshev Test" Theory

The Chebyshev test is to stimulate the ADC with a sinusoidal signal $x(t)=Vcoswt + C$ to obtain the best polynomial approximation for the input-output characteristics.

Consider the nonlinear ***static*** transfer function of a converter,

$$y = f(x) \tag{4}$$

where the function *f()* is operating on the input *x* to give the output *y*. When stimulated by a sinusoidal input in the form:

$$x(t) = V\cos\omega t + C \tag{5}$$

will result in a periodic output in the form of:

$$y(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(nwt) + e(t) \tag{6}$$

where the term *e(t)* takes into account all random errors like noise [5][6].

If the transfer function is a *polynomial* then *f(x)* can be expanded in the sum of Chebyshev polynomials as follows [5]:

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n C_n\left(\frac{x-C}{V}\right) \tag{7}$$

where $C_n()$ is the Chebyshev polynomial of the first type and,

$$C_n(\cos\theta) = \cos(n\theta) \tag{8}$$

Similarly, from the approximation of dividing the characteristics of the ADC into a polynomial and an ideal quantizer, we can describe the smooth polynomial *g(x)* as:

$$g(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n C_n\left(\frac{x-C}{V}\right) \tag{9}$$

provided that the effect of the quantization is neglected. This is true for high resolution bits as shown in (1) and (2).

To describe the ***dynamic*** response of the converter, additional terms are introduced in the output equation,

$$y(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(nwt) + \sum_{n=1}^{\infty} b_n \sin(nwt) + e(t) \tag{10}$$

where the out of phase terms accounted for by the coefficients b_n are caused by the dynamic nonlinearity [6]. It can be seen in Figure 4 [6] that the dynamic response of a converter is not a single valued function, meaning that the converter responds to rising inputs and falling inputs differently. The converter transfer function can be divided into two functions: $g_1(x)$ and $g_2(x)$ describing the ADC response to falling and rising values of the sinusoidal input respectively.

$$g_1(x) = g(x) + h(x) \tag{11}$$

$$g_2(x) = g(x) - h(x) \tag{12}$$

where *g(x)* representing the average characteristic and *h(x)* representing the deviation from the average [6]. The average function *g(x)* is that of (9), and h(x) is a function of the second kind of Chebyshev polynomials.

Above, we described the difference between the static and dynamic response of ADCs. The work presented in this paper considers only the static characteristic of a given ADC, where the function *g(x)* describing the static response is also the average of the dynamic response. The Chebyshev test will give an accurate measurement to the smooth part of the nonlinearity.

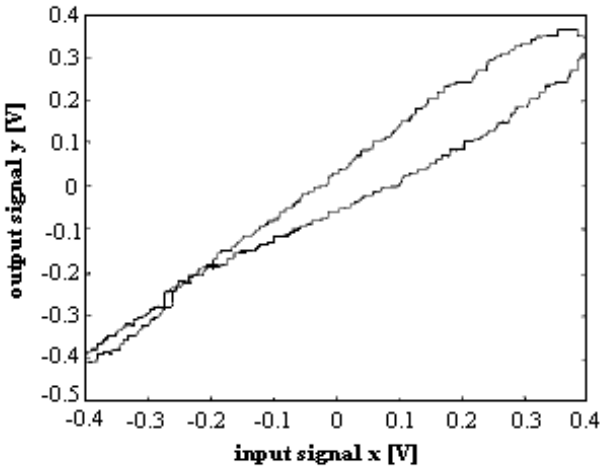

Figure. 4. Dynamic Response of an ADC using a sinusoidal input [6].

3.2. Modeling the INL

Equation (9) allows one to measure exactly a polynomial nonlinearity. The coefficients a_n of (9) can be evaluated using a Fast Fourier Transform (FFT) test applied to the output of the ADC, which is carried out as follows:

- Apply a sinusoidal input to the converter. This input test signal has to span the full scale to be able to evaluate the INL for the whole input range. A sufficiently low test frequency must be used to validate the usage of (6) [6].
- Apply an FFT to the output of the converter (staircased sinusoidal wave) using a suitable sampling frequency and number of FFT points.

The FFT determines the frequency components of a signal. The output of the test includes a noise floor and significant harmonics. The quantization noise forms the noise floor, which is a small value for high resolution bits. This noise is not a defect but it is due to the finite length of the digital output. For ADCs with 8 resolution bits and more, the quantization effect can be neglected [7][8]. The INL and other converter impairments cause the *harmonics* and add extra

noise to the noise floor [8]. Also *offset* effects on the harmonic distortion are negligible with respect to the nonlinearity effects [2].

The first few harmonics (amplitude and phase) extracted from the FFT test are inserted in the model. The harmonics taken into consideration are those above the noise floor. The error of the ADC is then calculated as the difference between the input signal and a signal constructed from the *limited number of harmonics*. The input is scaled to the output, i.e. inputs spanning the full input range will also span the output full range (from code 000...0 to 111...1).

The INL is modeled using the following equation:

$$inl = \left(a_0 - \frac{1}{2}(2^N - 1)\right) + \left(a_1 - \frac{1}{2}(2^N - 1)\right)\cos(\omega t + f_1) \quad (13)$$
$$+ a_2\cos(wt + f_2) + a_3\cos(wt + f_3) + a_4\cos(wt + f_4)$$
$$+ a_5\cos(wt + f_5) + a_6\cos(wt + f_6) + a_7\cos(wt + f_7)$$
$$+ a_8\cos(wt + f_8) + \ldots$$

where the coefficients a_n are the harmonics values extracted from the FFT test and f_n are the phases of the harmonics in radians.

3.3. Model Implementation

The model is implemented using Verilog-AMS hardware description language. It assumes an ADC with high resolution bits to neglect the effect of the quantization noise. The model parameters are:

- Number of resolution bits (N).
- Conversion time (td) which is the time the ADC takes to convert the analog input to the digital code.
- Offset error, representing a shift in the transfer function to the right or to the left.
- Gain error, representing a change in the slope of the ideal straight line representing the transfer function of the ADC.
- The reference voltages, where the difference determines the input full scale range.
- The harmonics extracted form the FFT test (amplitude and phase).

A partial listing of the model is given in Listing 1.

From (9), an infinite number of harmonics is required, but this is to get the actual response. Harmonics above the noise floor are sufficient to represent the INL. The model presented here uses a limited number of harmonics. The more harmonics used, the better the accuracy and the closer the modeled INL is to the actual value. As the INL is plotted, if the INL versus the code words is a bow shaped plot, this indicates the predominance of the even harmonics wheras, an S-shaped plot indicates the predominance of odd harmonics [4].

Listing 1. ADC Model Implementation using Verilog-AMS

```
module adc(out,in,clk)
    parameter integer N=16 from [12:24]; //resolution in bits}
    parameter real ref_plus = 5;
    parameter real ref_minus= -5;\
    parameter real td= 1e-9; // conversion time
    parameter real offset_error= 0; //in terms of LSB
    parameter real gain_error= 0; // in terms of LSB
    parameter real test_frequency= 15.25879;//test frequency
    // hx: harmonic components in dB
    // phx: the phase of each harmonic
    parameter real dc_component = 90.30866;\
    parameter real h1= 90.309;\
    parameter real ph1 = 0.008306843;
    parameter real h2= -29.70907;\
    parameter real ph2 = 179.302248269;
    parameter real h3= -23.73895;
    parameter real ph3 = 77.269534889;
    parameter real h4= -21.79287;
    parameter real ph4 = -32.298964788;
    parameter real h5= -18.40337;
    parameter real ph5 = 105.741288156;
    parameter real h6= -29.09376;
    parameter real ph6 = -177.111585591;
    parameter real h7= -17.02576;
    parameter real ph7 = 91.889480473;

initial
begin
    fullscale=ref_plus-ref_minus;
    LSB=fullscale/pow(2,N);
    a0 = pow(10,(dc_cmoponent/20));
    a1 = pow(10,(h1/20));
    ...
end

always @(posedge clk)
begin
    inl=(a0-(0.5*(pow(2,N)-1)))+(a1-(0.5*(pow(2,N)-1)))*cos(w*t+f1)
    + a2*cos(2*w*t + f2);
    ...
end

endmodule
```

4. SIMULATION RESULTS

This section shows some simulation results comparing the behavior of the model to a real circuit†.

An ADC model with a different modeling approach is also compared to the proposed solution.

The first example consists of, a 12-bit SAR (Successive Approximation Register) analog to digital converter simu-

† All simulations were done using Mentor Graphics-ADVance MS version 4.2-2.1.

lated at the transistor level. A sinusoidal input spanning the full input range was used to stimulate the ADC. The ADC clock used was 5MHz. The staircased output was passed through an FFT test and the harmonics were extracted. These harmonics were plugged into the model. Both, the model and the circuit , were stimulated using a ramp signal, slow enough to cover all codes of the ADC. The input-output characteristics of both simulations is compared in Figure 5. This figure is only a zoomed part to show clearly part of the simulation. The rest of the transfer function is also very close. The model runs in *1sec 120ms* achieving a gain of more than 300x.

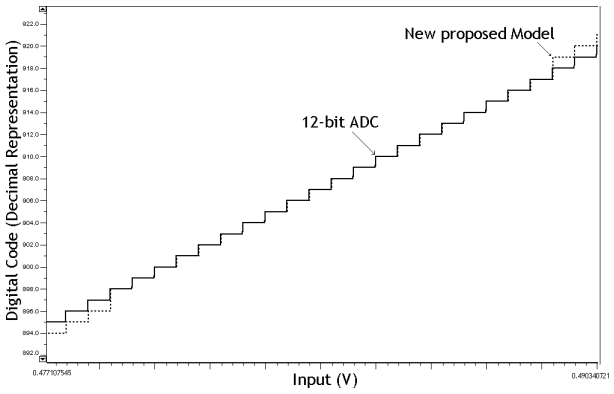

Figure. 5. A comparison between a 12-bit ADC Spice circuit and the output from the proposed behavioral model.

The second example compares the output obtained from the suggested model and a general ADC model having the INL as an input vector. Both models used a resolution of 16 bits.The input fullscale used is 10 volts varying from -5.0 volts to +5.0 volts. The old approach simulated in *45min 29sec 820ms* while the new model simulated in *15sec 450ms*. A speed gain of 176x acquired. Results shown below in Figure 6 show a zoomed figure comparing the two transfer characteristics. .

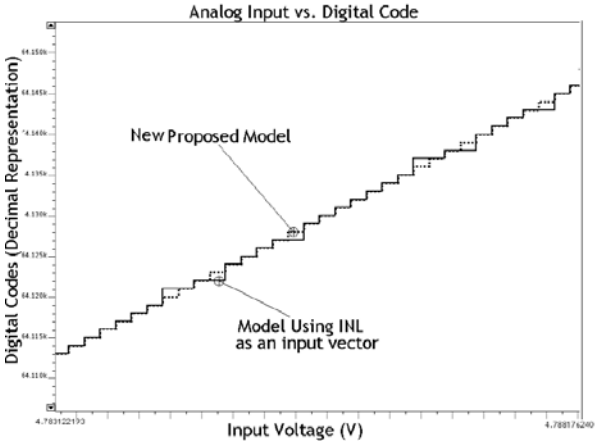

Figure. 6. A comparison between the transfer functions of a 16-bit behavioral model using the INL as an input vector and the new model.

Figure 7 shows the INL value calculated for the full scale input from the model.

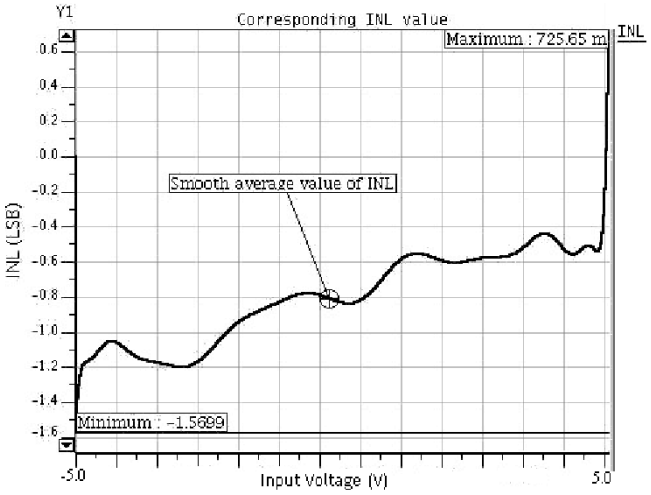

Figure. 7. The INL value calculated from the new model.

The two models were further simulated with a sinusoidal input. The old model completed the transient simulation in *1hr 31min 39sec 730ms* while the new model simulated in *38sec 270ms* achieving a speed gain of 143x. A zoomed portion of the sinusoidal outputs is shown in Figure 8.

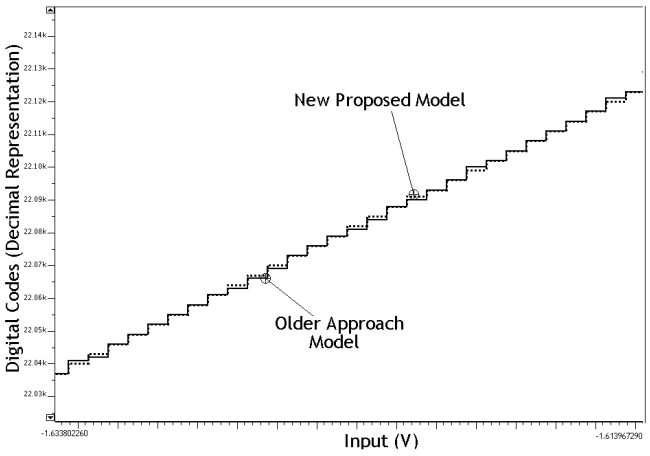

Figure. 8. A comparison between the two models stimulated by a sinusoidal input.

Applying an FFT to both outputs results in a very close spectral distribution as shown in Figure 9.

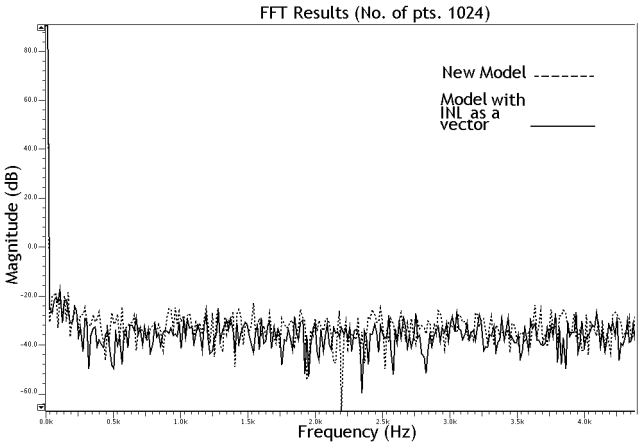

Figure. 9. Spectral comparison between the two model.

5. CONCLUSION

The work presented in this paper targets a new approach for ADC modeling. Chebyshev polynomials were used to describe the average nonlinearity of the converter. The proposed approach was found to suit all types of ADCs because it is not a structural model. It models the average overall performance of the converter which is required at different levels of the design process. From the experimental results, the model showed a noticeable speed gain with minimal loss of accuracy. The transfer function generated by the model is very close to that of the real circuit. Future work will be devoted to further experimental tests, validating the model for low resolution bits and calculating the deviation from the average. In addition, other effects such as supply noise and temperature effects will be added to the model.

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