Expected Performance Centering for Analog/RF Designs

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Abstract

We unite the conventional analog/RF design objectives such as design centering and performance targeting and propose a generalized analog/RF design objective. We propose expected performance centering, i.e., to maximize the expected performance margin of a circuit under process and environmental variations for topology selection with performance specification in a hierarchical design. We develop three methods to compute expected performance margin. Our experimental results show improved expected performance margin achieved by the proposed expected performance centering technique.

1 Introduction

Analog/RF design complexity arises due to (1) complex design specification including up to tens of performance metrics, such as gain, linearity, noise signal ratio, power consumption, etc., and (2) the significant sensitivities of the design metrics to variations of environmental and design parameters, such as temperature, supply voltage, transistor channel length, threshold voltage, gate oxide thickness, and resistive and capacitive parasitics. Such sensitivities have been growing increasingly significant due to the latest technology scaling, and introduce significant variations of analog/RF design performance metrics. As a result, analog/RF design must target parametric yield optimization.

Several techniques have been proposed for analog/RF design parametric yield maximization. Implicit parametric yield optimization techniques include robust programming, which includes process parameter variability bounds as inequality constraints, and optimize design metrics under such constraints [12]. Stochastic programming includes explicit probability density functions in constraints and targets parametric yield optimization [6]. Exact parametric yield can be computed by surface integrals [3, 4]. Maximum parametric yield can be found by design centering, e.g., to find a point in the variable space with the maximum distance to the boundaries of an acceptability region [1, 8, 9]. Alternatively, performance centering finds the maximum performance margin, e.g., the maximum distance to the performance boundaries in a performance space [5].

We observe that design centering does not take into consideration of performance targeting, while performance centering does not take into consideration of parametric yield, e.g., a circuit with a large performance margin and a small parametric yield may not dominate another circuit with a small performance margin and a large parametric yield. We propose expected performance centering, i.e., to maximize the expected performance margin of a circuit under process and environmental variations for topology selection with performance specification in a hierarchical design, which unifies design centering and performance centering. We develop three methods to compute expected performance margin. Our experimental results compare design centering, performance centering, and expected performance centering.

The rest of this paper is organized as follows. We first present the notations that we use in this paper before we briefly present the existing analog/RF design optimization methods and objectives in Section 2, and propose expected performance centering in Section 3. We present our experimental results in Section 4, and conclude in Section 5.

2 Background

2.1 Notations

We use the following notations in this paper.

- x = design parameters[1]
- ε = design parameter variabilities
- $P(x+\varepsilon)$ = probability density function for design parameter variabilities
- $y = f(x)$ = performance metrics given by macromodeling in terms of design parameters
- U = performance constraints
- R = acceptability region in the solution space such that $y_i \leq U_i$, $\forall x \in R$, $\forall i$
- $Y = P(y \leq U)$ = parametric yield, i.e., the probability for the performance constraints are satisfied
- ρ = performance margin
- ϕ = expected performance margin

[1] We refer to design parameters which include parameters given by designers (e.g., transistor channel length and width), process parameters (e.g., transistor threshold voltage), and environmental parameters (e.g., temperature and supply voltage), etc.

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2.2 Methods

2.2.1 Robust Geometric Programming

Robust programming takes design parameter variabilities into account by including their bounds in terms of polyhedrons (i.e., intersection of a finite number of halfspaces) or ellipsoids as constraints, e.g., as follows [12].

$$\begin{array}{ll} \textit{minimize} & sup_{x\in\mathcal{U}} f_0(x) \\ \textit{subject to} & sup_{x\in\mathcal{U}} f_i(x) \le 1,\ i=1,...,m \\ & g_i(x) = 1,\ i=1,...,p \\ & x_i > 0,\ i=1,...,n \end{array} \quad (1)$$

where $x \in \mathcal{U}$ define uncertainties/variabilities.

In case that the objective f_0 and the constraints f_i are posynomial functions, g_i are monomial functions, (1) becomes a geometric program [2], and can be efficiently solved for analog/RF design automation.

2.2.2 Stochastic Programming

Explicit analog/RF design parametric yield maximization needs to (i) take into account variabilities for the design parameters and (ii) include the probabilistic parametric yield function in the objective [3, 4]. This gives a stochastic program as follows [6].

$$\begin{array}{ll} \text{Maximize} & P(y < U) \\ \text{Subject to} & P(x) \end{array} \quad (2)$$

Stochastic programming is a framework for modeling optimization problems which involve uncertainties and probability distributions. It maximizes the expectation of certain function of random variables, e.g., analytically or numerically, to provide useful information to a decision-maker [6].

2.2.3 Parametric Yield Computation

Parametric yield is the probability for the design parameter variations not to result in an unacceptable circuit performance. In a *disturbance space*, e.g., a Cartesian space spanned by the parameter variations, the *acceptability region* is defined as the set of parameter variations which do not result in unacceptable circuit performance for given design parameters. *Parametric yield* is given by the volume integral of the joint probabilistic density function of the variations in the acceptability region, or, the surface integral on the boundary of the acceptability region by applying Stokes' theorem [3, 4].

$$Y = \int_R P(x)dx = \int_{\partial R} D(x)dx \quad (3)$$

where R is the acceptability region, $y_i(x) \le U_i,\ \forall x \in R,\ \forall i$, ∂R gives the boundaries of the acceptability region R, $P(x)$ is the joint probability density function of the design parameters, $D(x)$ is the vectorial field which divergence is the joint probability density function $P(x)$, i.e.,

$$\nabla \cdot D(x) = P(x)$$

2.3 Objectives

2.3.1 Design Centering

Based on parametric yield and yield gradient computation, a greedy algorithm finds the maximum parametric yield [3, 4]. A double-sided ellipsoidal technique recursively divides a hyperellipsoid into three parts using two parallel hyperplanes [1]. A convexity-based technique approximates an acceptability region by a polytope and recursively partition the polytope into two parts using a hyperplane [8].

A more efficient approach is to find the *parameter distances* [9] as a guide to find maximum parametric yield. A parameter distance is given by a performance margin and the gradient of the performance metric respect to the design parameter. An exponential function is applied to provide a differentiable approximation of the minimum function of the parameter distances [9]. The maximum parameter distance may not imply the maximum parametric yield, e.g., in the presence of non-convex acceptability regions, or multiple acceptability regions in a close range, but serve as a guide to find a good starting point for the maximum parametric yield.

2.3.2 Performance Centering

Performance centering finds the maximum performance margin, i.e., the maximum slack to all performance constraints. In a performance space, this corresponds to finding the center of a performance acceptability region with the maximum distance to all boundaries [5].

$$\begin{array}{ll} \text{Maximize} & \rho = \Pi_i S_i \\ \text{Subject to} & S = U - y \\ & S > 0 \\ & x > 0 \end{array} \quad (4)$$

Performance centering is proposed to evaluate the "capability" for each candidate circuit topology to meet given performance specifications, e.g., in a hierarchical design, for topology selection. The objective of performance centering differs with the objective of design centering, in that the latter is for yield maximization, while the first is for performance targeting.

2.3.3 Quality Loss Function

Taguchi proposed to reduce performance variability as a means to increase parametric yield and product quality [4]. Observing that design centering optimizes only parametric yield, which is insensitive to the tightness of performance distributions, Taguchi proposed to optimize quality loss function, which is defined to increase gradually as the circuit performance deviates away from the target performance, as a means to measure the closeness of their performances to the targets. However, Taguchi only considered quality loss function for a single performance metric, which is chosen arbitrary, e.g., any symmetric function could serve as a Taguchi quality loss function.

3 Robust Optimization by Expected Performance Centering

3.1 Comparing Analog/RF Design Objectives

We now compare design centering and performance centering for a given performance macromodel and the acceptability region boundaries, e.g., as shown in Fig. 1.

Performance centering finds the maximum *performance margin*, i.e., a point in the *performance space* with the maximum distance to all performance boundaries. In Fig. 1, this corresponds to finding x_1 in the deepest valley. However, there is no parametric yield consideration. For example, performance centering could find a solution with large margins to all performance bounds but also a large gradient of performance regarding to disturbances, therefore of a small parametric yield. In Fig. 1, this corresponds to a deep but narrow valley.

Alternatively, design centering finds maximum parametric yield, which, e.g., in some cases, implies the maximum *variable margin*, i.e., a point in the *variable space* with the maximum distance to the performance boundaries $y = f(x) = U$. In Fig. 1, this corresponds to finding the widest valley. However, design centering regards circuits with accepted performance with equal quality, without preference of performance margins. E.g., it may find a shallow valley in Fig. 1.

Quality loss function introduces increased penalty in analog/RF design optimization as the expected circuit performance deviates from the specified target performance. However, in many design scenarios, designers do not have a specific performance target. Rather, a minimum allowable performance requirement is specified. Achieving further performance improvement is preferred, because it would boost the overall system specification, or, in a hierarchical design, an improved performance in a module leads to increased design margins for the other modules. We propose expected performance centering which fits better with these design scenarios compared with quality loss function optimization.

3.2 Expected Performance Centering

We propose a more sophisticated design objective, i.e., expected performance centering, which is to maximize the expected performance margins under process and environmental variations. Expected performance centering combines parametric yield maximization and performance centering into a more generalized design objective. It is an extension of design centering / yield maximization, in that it introduces preference of large performance margins among accepted solutions. It is also an extension of performance centering, in that it introduces yield consideration. E.g., in topology selection in a hierarchical design for given performance specifications, a circuit with a large performance margin and a small yield may not be preferable to that of a small performance margin and a large yield. In Fig. 1, expected performance centering finds a deep and wide valley.

Mathematically, we define *expected performance margin* as follows.

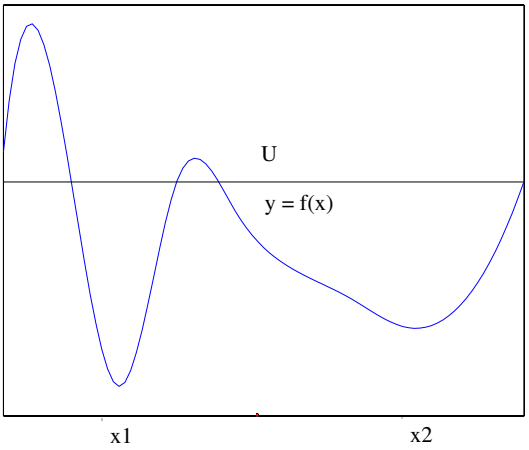

Figure 1: Performance $y = f(x)$ and its bound U. Performance centering finds x_1 for maximum performance margin (i.e., the deepest valley). Design centering / parametric yield maximization finds x_2 for maximum variable margin (i.e., the widest valley). Expected performance centering finds a deep and wide valley.

Definition 1 *For design performance requirements $y \le U$ under design parameter distribution $P(x)$,* expected performance margin *is given by:*

$$\begin{aligned} \phi(x) &= \int_R \rho(x+\varepsilon)P(x+\varepsilon)d\varepsilon \\ &= \int_R \Pi_i(U_i - y_i(x+\varepsilon))P(x+\varepsilon)d\varepsilon \end{aligned} \tag{5}$$

where $y_i(x+\varepsilon) \le U_i$, $\forall x+\varepsilon \in R$, $\forall i$.

For design parameters of extremely small variabilities, e.g., $P(x+\varepsilon) = \delta(\varepsilon)$, (5) becomes

$$\phi(x) = \int_R \rho(x+\varepsilon)\delta(\varepsilon)d\varepsilon = \rho(x) \tag{6}$$

i.e., expected performance margin becomes conventional performance margin.

For a extremely small performance margin which can be approximated by a constant $\rho(x) = \Pi_i U_i - y_i(x) = \alpha$, (5) becomes

$$\phi = \int_R \alpha P(x)dx = \alpha \int_R P(x)dx = \alpha Y \tag{7}$$

i.e., expected performance centering becomes parametric yield maximization or design centering.

In general cases, expected performance centering provides a better estimate of product quality in the presence of design parameter variations. In a hierarchical design, a large performance margin of a module circuit ease design complexity of the rest of the system. Performance margin as a product of the performance metrics also gives an estimate of the volume of the performance space bounded by the Pareto front [10, 11]. A

larger volume of performance space implies a larger capability to tradeoff among the performance metrics, and possibly a larger parametric yield [5].

We formulate the problem of expected performance centering as follows.

$$\begin{array}{ll} \text{Maximize} & \phi(x) = \int_R \rho(x+\varepsilon)P(x+\varepsilon)d\varepsilon \\ \text{Subject to} & \rho(x+\varepsilon) = \Pi_i(U_i - y_i(x+\varepsilon)) \\ & y_i(x+\varepsilon) \le U_i,\ \forall x+\varepsilon \in R,\ \forall i \\ & x \ge 0 \end{array} \quad (8)$$

3.3 Computing Expected Performance Margin

3.3.1 Sampling

(5) is in the form of an expectation of a distribution, which indicates that an expected performance margin can be computed by a Monte Carlo simulation based on the design variable distributions.

$$\phi_{sampling} = \frac{1}{N}\sum_{i=1}^{N}\Pi_i(U_i - y_i(x+\varepsilon = a_i)) \quad (9)$$

where a_i are sampling points in an acceptability region $y(x+\varepsilon) \le U$, which are generated by following the variable distributions $P(x+\varepsilon)$.

Therefore, expected performance margin ϕ can be taken as a weighted sum of performance margins of the variational variables. A performance margin is in the form of posynomial function and can be optimized by geometric programming. As a result, an expected performance margin is also in the form of a posynomial function, and can be optimized by geometric programming.

3.3.2 Integral of Gaussian Distributions

For efficiency improvement, we can compute integrals based on closed form $y(x) = f(x)$ and $P(x+\varepsilon)$ formulas. For example, for (piecewise) linear polynomial macormodels $y(x) = f(x)$ and Gaussian design parameter distributions $P(\varepsilon)$,

$$\begin{aligned} f(x) &= a_0 + a_1 x \\ P(\varepsilon) &= \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(\varepsilon-\mu)^2}{2\sigma^2}} \end{aligned} \quad (10)$$

we can use Gaussian integrals, e.g., as follow.

$$\begin{aligned} \int_0^z \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(\varepsilon-\mu)^2}{2\sigma^2}} d\varepsilon &= \frac{1}{2} erf(\frac{z-\mu}{\sqrt{2}\sigma}) \\ \int_0^z \frac{1}{\sqrt{2\pi}\sigma} \varepsilon e^{-\frac{(\varepsilon-\mu)^2}{2\sigma^2}} d\varepsilon &= \frac{\sigma^2}{\sqrt{2\pi}}(1 - e^{-\frac{(z-\mu)^2}{2}}) \\ &\quad + \frac{\mu}{2} erf(\frac{z-\mu}{\sqrt{2}\sigma}) \end{aligned} \quad (11)$$

3.3.3 Surface Integral

Similar to (3), by applying Stokes' theorem, we can achieve volume integral by computing surface integral of a vectorial field which divergence is the joint probability density function.

$$\begin{aligned} \phi(x) &= \int_R \Pi_i(U_i - y_i(x+\varepsilon)P(x+\varepsilon)d\varepsilon \\ &= \int_{\partial R} \Pi_i(U_i - y_i(x+\varepsilon)D(x+\varepsilon)d\varepsilon \end{aligned} \quad (12)$$

where R is the acceptability region, $y(x) < U \forall x \in R$, $P(x)$ is the joint probability density function of the design parameters, $D(x)$ is the vectorial field which divergence is the joint probability density function $P(x)$, i.e.,

$$\nabla \cdot D(x) = P(x)$$

3.4 Overall Flow

We formulate robust/RF analog design optimization problem as follows.

Problem 1 *Given*

1. *design parameter x,*
2. *design parameter variabilities $P(x+\varepsilon)$,*
3. *performance constraints $y < U$,*

find design parameters x^* such that the expected performance margin $\phi(x^*)$ is maximized.

Algorithm 1 presents our proposed analog/RF design optimization method by expected performance centering.

Algorithm 1: Expected Performance Centering for Analog/RF Designs

Input: x, $P(x+\varepsilon)$, $y \le U$
Output: x^* s.t. $\phi(x^*)$ is maximized

1. Construct a performance macromodel $y = f(x)$
2. Find acceptability region boundaries $y = f(x) = U$
3. Compute performance margin $\rho(x)$
4. Compute expected performance margin $\phi(x)$
5. Find maximum expected performance margin $\phi(x^*)$

We construct a macromodel for an analog/RF design by circuit simulation and data regression. and find performance boundaries $y = f(x) = U$ based on the analytical performance macromodel, which is more efficient than the line search algorithm as in [3, 4].

After finding the boundaries of the acceptability regions, we compute expected performance margin within the acceptability regions by sampling, direct volume integral, or surface integral. Finally, a steepest descent search algorithm can be applied to find the largest expected performance margin.

4 Experiments

We present a simple analog/RF circuit design as an illustrative example which shows the differences between the existing analog/RF design objectives and compares our proposed expected performance centering with the existing design centering and performance centering techniques.

We design a three-inverter ring oscillator (which schematic is shown in Fig. 2) based on Synopsys HSpiceRF simulation on Berkeley Predictive Technology Model (BPTM) of $70nm$ technology. We adjust two design parameters, namely, channel width W and channel length L for each transistor in the ring oscillator, to achieve three performance metrics: oscillation frequency $f_0 \geq 1GHz$, phase noise $N \leq -40dB$, and power consumption $P \leq 1mW$.

Fig. 3, Fig. 4 and Fig. 5 show respectively the contours of oscillation frequency f_0, phase noise N, and power consumption P of the ring oscillator for different transistor channel width W and transistor channel length L, which are multiple times of the minimum transistor channel length $0.07\mu m$. Fig. 6 shows the three performance constraints and the acceptability region bounded by the oscillation frequency boundary $f_0 \geq 4GHz$ and the phase noise boundary $N \leq -40dB$. Table 1 gives the design parameters and the performance metrics of the four corners of the acceptability region. We approximate the three performance metrics in the acceptability region via bi-linear interpolation as follow.

$$\begin{aligned}
\Delta f_0 &= (\frac{W}{64}-1)(-0.61L+2.10)+(2-\frac{W}{64})(-0.49L+1.26) \\
\Delta N &= (\frac{W}{64}-1)(2.44L-5.79)+(2-\frac{W}{64})(2.10L-4.69) \\
\Delta P &= (\frac{W}{64}-1)(0.17L-0.32)+(2-\frac{W}{64})(0.09L+0.32) \quad (13)
\end{aligned}$$

Design centering finds the largest distance to the boundaries of the acceptability region. Because process variation has little effect on the large transistor channel width W, in this case, design centering finds the median of the longest vertical strip of the acceptability region, which is at $(W,L) = (128, 2.91)$.

Performance centering finds the largest performance margin, by computing the derivative of the performance margin, e.g.,

$$\begin{aligned}
\Delta f_0 \cdot \Delta N \cdot \Delta P &= -0.25L^3 + 1.93L^2 + -4.82L + 3.90 \\
\frac{\partial}{\partial L}(\Delta f_0 \cdot \Delta N \cdot \Delta P) &= -0.75L^2 + 3.86L - 4.82 = 0 \quad (14)
\end{aligned}$$

for $W = 128$, and the performance center is given by one of the roots of the quadratic equation at $(W,L) = (128, 3.04)$,

Assuming Gaussian distribution for transistor channel length L with $3\sigma = 20\%\mu_L$,[2] we find the expected performance margin by taking samples for the design centering solution, performance centering solution, and the points in between. Table 2 gives the results. We observe that performance centering solution has a larger product of the performance margins ($80.33MHz \cdot dB \cdot mW$) than the design centering solution ($75.37MHz \cdot dB \cdot mW$), however, the largest expected performance margin ($67.53MHz \cdot dB \cdot mW$) is achieved at $(W,L) = (128, 3.00)$, other than the design centering solution and the performance centering solution. Expected performance centering finds such a solution.

[2] Our methodology can still be applied in cases that transistor channel length is not in a Gaussian distribution.

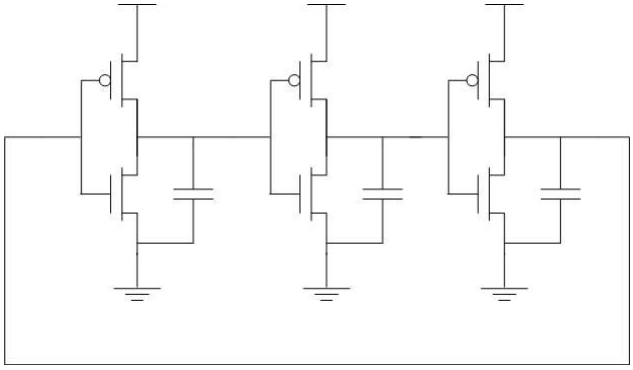

Figure 2: A three-inverter ring oscillator.

Table 1: Design parameters and performance metrics of the four corners of the acceptability region.

W	L	f_0	N	P
128	3.46	1.00	-42.67	0.78
128	2.37	1.66	-40.00	0.92
64	2.59	1.00	-40.75	0.44
64	2.23	1.17	-40.00	0.47

5 Conclusion

We propose expected performance centering, which unifies performance centering and design centering as analog/RF design objectives. For a large parametric yield, expected performance centering approaches conventional performance centering. For a small parametric yield, expected performance centering approaches design centering. We develop three methods which compute expected performance centers, and present a circuit example which illustrates the differences between the design objectives. Expected performance centering provides a new method for analog/RF design optimization.

Table 2: Performance margin (ρ) and expected performance margin (ϕ) in $MHz \cdot dB \cdot mW$ for (I) the design centering, (II) the performance centering, and (III) the expected performance centering solutions.

	W	L	ρ	ϕ
I	128	2.91	75.37	65.42
II	128	3.04	80.33	67.12
III	128	3.00	79.76	67.53

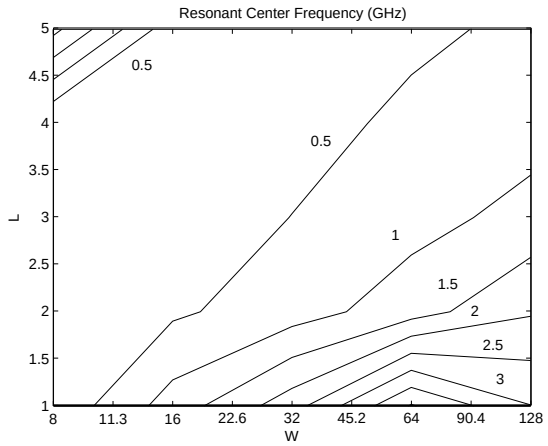

Figure 3: Resonant center frequency (Hz) as a function of transistor channel width W ($\times 0.07\mu m$) and transistor channel length $L(\times 0.07\mu m)$.

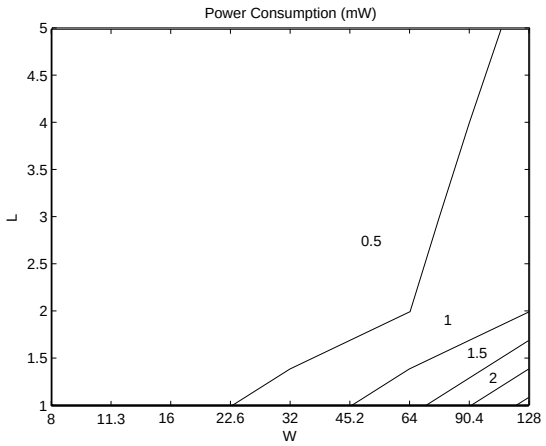

Figure 5: Power consumption (W) as a function of transistor channel width W ($\times 0.07\mu m$) and transistor channel length L ($\times 0.07\mu m$).

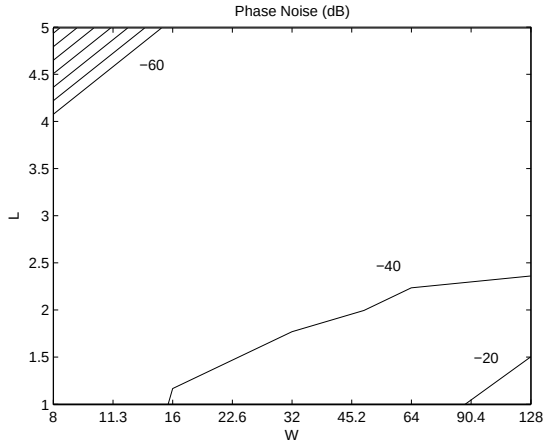

Figure 4: Phase noise (dB) as a function of transistor channel width W ($\times 0.07\mu m$) and transistor channel length $L(\times 0.07\mu m)$.

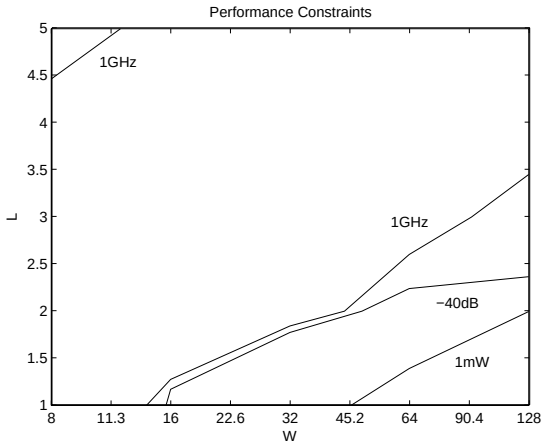

Figure 6: Acceptability region given by the performance constraints ($f_0 \geq 1GHz$, $N \leq -40dB$, and $P \leq 1mW$) in the design space of transistor channel width W ($\times 0.07\mu m$) and transistor channel length L ($\times 0.07\mu m$).

References

[1] H. L. Abdel-Malek, A.-K. S. O. Hassan, and M. H. Heaba, "A Boundary Gradient Search Technique and Its Applications in Design Centering," *IEEE Trans. on CAD*, 18(11), 1999, pp. 1654-1661.

[2] S. Boyd, S.-J. Kim, L. Vandenberghe, and A. Hassibi, "A Tutorial on Geometric Programming," Technical report, Electrical Engineering Department, Stanford Univeristy, 2005. Available at `www.stanford.edu/ ~boyd/gp _tutorial.html` .

[3] S. W. Director, P. Feldmann, K. Krishna, "Statistical Integrated Circuit Design," IEEE Journal of Solid-State Circuits, 28(3), 1993, pp. 193-202.

[4] P. Feldmann and S. W. Director, "Integrated Circuit Quality Optimization using Surface Integrals," IEEE Trans. CAD, 12(12), 1993, pp. 1868-1879.

[5] X. Li, J. Wang, L. T. Pillegi, T.-S. Chen, and W. Chiang, "Performance-Centering Optimization for System-Level Analog Design Exploration," in *Proc. DAC*, 2005, pp.

[6] P. Kall, and S. W. Wallace, *Stochastic Programming*, John Wiley & Sons, 2005.

[7] J. Kim, J. Lee, L. Vandenberghe, and C.-K. Yang, "Techniques for Improving the Accuracy of Geometric-Programming Based Analog Circuit Design Optimization," in *Proc. ICCAD*, 2004, pp.

[8] S. S. Sapatnekar, P. M. Vaidya, and S. Kang, "Convexity-based algorithms for design centering," *IEEE. Trans. Computer-Aided Design*, 13(12), 1994, pp. 1536-1549.

[9] R. Schwencker, F. Schenkel, H. Graeb, and K. Antreich, "The Generalized Boundary Curve - A Common Method for Automatic Nominal Design and Design Centering of Analog Circuits," in *Proc. DATE*, 2000, pp. 42-47.

[10] G. Stehr, H. Graeb, and K. Antreich, "Performance Trade-Off Analysis of Analog Circuits by Normal-Boundary Intersection," in *Proc. Design Automation Conference*, 2003.

[11] G. Stehr, H. Graeb, and K. Antreich, "Analogy Performance Space Exploration by Fourier-Motzkin Elimination with Application to Hierarchical Sizing," in *Proc. ICCAD*, 2004.

[12] Y. Xu, K.-L. Hsiung, X. Liu, I. Nausieda, S. Boyd, and L. Pileggi, "OPERA: Optimization with Ellipsoidal Uncertainty for Robust Analog IC Design," in Proc. *DAC*, 2005, pp. 632-637.