Automated Receiver Design and Optimization for 4G Wireless Communication Systems

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ABSTRACT

This paper presents the design methodology and underlying algorithms of a tool developed for automated receiver design and optimization for fourth generation (4G) Wireless Communication Systems. An algorithm to systematically design and optimize the receiver budget for the multi-standard case is introduced. The goal of this algorithm is to find a multi-standard receiver budget that meets or exceeds the specs of the addressed wireless standards while keeping the requirements of each of the receiver blocks as relaxed as possible. This tool offers RF engineers a deep insight into the receiver behavior at a very early stage of the design flow. It models the impact of some circuit non-idealities using a high level of abstraction. This reduces the number of design iterations and, thus, the time-to-market of the solution. The reuse of already available intellectual property (IP) blocks is also considered in the tool. This can result in a significant cost reduction of the receiver implementation.

1. INTRODUCTION

Highly integrated multi-standard receivers have many desirable characteristics that make them suitable for the fourth generation wireless. The demands on 4G wireless terminals reduce the viability of a stacked solution. On the contrary, the use of programmable hardware able to adapt to different standards and different environmental conditions can be key in reducing the overall power consumption, area and cost of a mobile terminal.

A good architectural design is not only vital in order to reduce the time-to-market of the solution. It may also produce a larger overall power save than power reduction circuit techniques implemented in each individual block.

The realization of an efficient receiver budget is one of the most compelling problems RF engineers face nowadays. Even in the single standard case, the level of complexity of a wireless communications receiver is enormous. When the multi-standard case comes into the picture, this problem is aggravated with the need to share as much hardware as possible while keeping the performance levels high and the power consumption low.

The advantage of programmable blocks and architectures comes in terms of re-usability, flexibility, and area and power consumption. Moreover, using digitally tunable blocks allows to compensate for process variations and other effects that greatly affect analog circuits increasing, thus, the reliability of the overall system.

Even though we are getting closer to the Software Defined Radio (SDR) paradigm, there are still a number of major practical problems associated with placing the ADC right after the antenna. Therefore, frequency translation is still a must in most modern receivers. This together with filtering and amplification stages eases the job of the analog-to-digital converter and keeps the power consumption low enough to make the system practical for mobile terminals. In these receivers the analog input signal goes through a series of amplification, filtering and frequency translation stages until it is converted into a digital signal for digital post-processing.

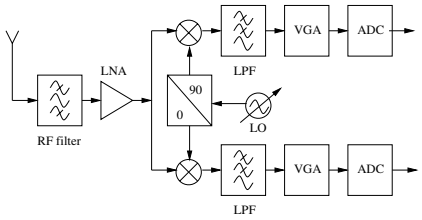

Figure 1: Zero IF receiver architecture.

Figure 1 shows the block diagram of a zero-IF receiver, one of the most promising architectures used in multi-standard wireless communications receivers.

We propose a tool that automates the process of design space exploration for multi-standard RF receivers. This tool is aimed to ease the RF engineer's job as it fills a gap left by the already available CAD tools that address the receiver design problem. This paper describes the underlying algorithms employed in the tool when designing and optimizing a multi-standard receiver budget. The paper is organized as follows: Section 2 gives an overview of the related work, Section 3 reviews some basic definitions, Section 4 describes the proposed methodology, Section 5 shows simulation results using a WCDMA/WLAN multi-standard receiver as an example. Finally, the conclusions are discussed in Section 6.

2. RELATED WORK

The system level design is still nowadays done in many instances using the help of spreadsheets. Besides being error prone, this method is very limited in the number of different design possibilities it can explore within a given time. There is a number of EDA tools [1–5] that automate parts of this process. Most of them focus on analysis [3–5]. They may provide accurate models for the blocks [3, 5] or analyze the frequency behavior of certain parts of the circuit [3,5], but in

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general these tools provide little or no help at all to the RF engineer in the system level design process. Other reported tools [1,2] and methodologies [6] help in the design process, but they only address the single-standard case. The main difference between our approach and the existing approaches is that we provide a design tool for multi-standard receivers.

3. BACKGROUND

3.1 Radio Electronics Definitions

Sensitivity:The sensitivity of a receiver is the minimum signal power that has to be detected in the presence of noise.

Selectivity: The selectivity measures the ability to select a weak desired signal channel in the presence of much stronger adjacent interferers (blockers).

Automatic Gain Control (AGC): AGC is introduced in receivers in order to be able to adjust the total gain of the chain. The maximum gain option will be used when receiving signals close to the sensitivity level. The minimum gain option will be used when receiving signals of large power. The control mechanism introduced by the AGC allows to address the far-near problem leading to an overall power save and avoidance of undesired effects such as desensitization [7].

The cost functions that are evaluated in this tool are the overall noise figure (NF), the second and third order intercept points (IIP2, IIP3), and the number of bits of the analog-to-digital converter (ADC). An extensive description of this parameters can be found at [7].

The overall **noise factor for the cascaded receiver blocks** is calculated using Friis equation:

$$nf = 1 + (nf_1 - 1) + \frac{nf_2 - 1}{A_1} + \cdots + \frac{nf_m - 1}{A_1 \cdots A_{(m-1)}} \quad (1)$$

where nf_i is the noise factor and A_i is the power gain of the i-th block. The noise figure is the equivalent in dB of the noise factor, $NF = 10log(nf)$.

At a given frequency, the **third order intercept point (IIP3)** is equal to:

$$\frac{1}{IP_3^2} = \frac{1}{IP_{3,1}^2} + \frac{A_1}{IP_{3,2}^2} + \cdots + \frac{A_1 \cdots A_{n-1}}{IP_{3,n}^2} \quad (2)$$

where $IP_{3,i}$ is the third order intercept point and A_i is the gain of the i-th block. The **second order intercept point (IIP2)** has an equivalent equation.

The number of bits of the ADC is related with the **dynamic range (DR_{ADC})** of its input:

$$DR_{ADC} = P_{max} - P_{noise} + M \quad (3)$$

where P_{max} is the maximum signal power present at the ADC input, P_{noise} is the input noise floor, and M a margin set by the user. It should be brought out that P_{max} does not necessarily correspond to the maximum power input signal coming from the standard. It might come from a distortion component or from an outside blocker, for instance. It should be, therefore, highlighted that both the gain distribution and the filtering characteristics of the receiver chain play an important role in determining the dynamic range of the ADC.

The **effective number of bits of the ADC** $ENOB_{ADC}$ can be calculated as:

$$ENOB_{ADC} = \frac{DR_{ADC} - 1.76}{6.02} \quad (4)$$

As it can be seen from equations 1 and 2, linearity and noise impose qualitatively opposed conditions to the gain distribution. In order to achieve a good overall noise figure, a high gain in the front-end is desirable. On the contrary, a low front-end gain is preferred when looking at the linearity of the system. This parameter interaction is taken into account in the search for a receiver that meets specs.

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3.2 Definitions

We define the Usable Region UR of a receiver block as the subset of $\mathbb{R}^N$ where the specs of the block are both feasible and useful in the context of radio receivers. N is the number of parameters that define the characteristics of each block. The usable region UR is a very small subset of $\mathbb{R}^N$, which helps reducing the convergence time. The usable regions are the mechanism that allows to include the experience of an analog/RF designer into the tool. For instance, a filter with $10dB$ in-band attenuation is not an useful block to have in a receiver. Hence, there is no need to consider a filter with such characteristics during the design process.

Let B be the number of blocks of the receiver chain, $x_i \in UR_i \forall i \in \{1, B\}$ the parameter vector that contains the specs of the i^{th} block, $S \subset UR$ the set of parameter distributions $x = (x_1, \ldots, x_B)$ that meet the receiver specs, $x_{r,i} \in UR_i$ contains the most relaxed (and therefore easiest to meet) block specs, that is, A_{min}, NF_{max}, $IIP3_{min}$, etc., $x_{t,i} \in UR_i$ contains the toughest) block specs, that is, A_{max}, NF_{min}, $IIP3_{max}$, etc.

4. METHODOLOGY

4.1 The receiver budget problem

The main goal of this tool is to find a parameter distribution $x = (x_1, \ldots, x_B)$ such that $x \in S$ and $d(x_i, x_{r,i})$ is minimized, where $d(x_i, x_{r,i})$ is the Euclidean distance between x_i and $x_{r,i}$.

In other words, find a multi-standard receiver budget that meets or exceeds the specs of the addressed wireless standards while keeping the requirements of each of the receiver blocks as relaxed as possible.

Many tradeoffs have to be done when fixing the characteristics of each of the blocks. The interdependency between the overall noise and non-linearity characteristics on the gain and selectivity of all the blocks shown in Section 3.1 makes this task difficult.

4.2 Design Methodology

The receiver budget is realized taking the radio specifications of the standards to consider as goal functions. They constitute the input to the tool together with the receiver architectures the user wants to explore and the usable regions of the receiver blocks. At the output, a receiver budget with its performance is shown to the user.

The architecture selection and the order in which the amplifying and filtering operations are performed [7] will lead

```
while specs_met == false
  if gain_redistrib_needed == true
    redistribute_gain;
  else % gain redistribution not needed
   if rand ¡ p % change it anyway sometimes
      redistribute_gain;
   else
     redistribute_params_not_meeting_specs;
   end;
  end;
  cost = check_specs;
  if cost ¡ specs
   specs_met = true;
  end;
  if cost ¡ best_cost
   best_budget = this_budget;
  end;
end;
```

Figure 2: Algorithm to find a budget meeting specs.

to different block combinations and therefore, different results.

The first step is to check for convergence, that is, whether or not the specs are achievable at all. In this test, the best possible value for each parameter within the usable region is employed when calculating the cost functions. If any of the cost functions is not achievable, execution is halted and the usable regions revised.

The next step is to generate a seed solution. Each parameter of each block is set to its most relaxed value, that is, $x_{initial} = x_{r,1} \dots x_{r,B}$. Then, the operations sketched in Figure 2 are performed.

4.3 Impact Oriented Parameter Distribution

We propose a reassignment scheme for the values of the block parameters based on their impact on the overall system. It also takes into account how much margin for changing the parameter has, that is, its distance to the toughest block specs $d(x_i, x_{t,i}$. This parameter reassignment only takes place when the overall value does not meet specs.

Let us describe first the way this algorithm works in the case of the noise figure. Table 1 shows a numerical example of the noise figure reassignment. Equation 1 shows the aggregated noise factor, which is a function of the noise factors and gains of each of the blocks. The difference Δ between the current noise factor value and a new noise factor value is, therefore:

$$\Delta = \Delta_1 + \frac{\Delta_2}{A_1} + \cdots + \frac{\Delta_m}{A_1 \cdots A_{(m-1)}} \tag{5}$$

Hence, a change in the front-end noise factor has a bigger impact in the overall noise factor. Let A_i be the power gain of the i-th block and δ_i the margin for change of its noise factor, that is, the difference between its current value and the best achievable value the noise factor range allows for. The impact of tweaking the noise factor of the i-th block is:

$$\chi_i = \begin{cases} \delta_1 & \text{if } i = 1 \\ \frac{\delta_i}{A_1 \cdots A_{i-1}} & \text{if } i \neq 1 \end{cases} \tag{6}$$

Table 1: Noise figure reassignment

Parameter	RF filter	LNA	Mixer	IF filter	VGA
nf max	10	10	100	10	1000
nf min	1.26	1.26	3.16	1.99	3.16
A_i	0.36	65.8	5.5	0.3	5e+5
current nf	1.55	1.5	6.38	2.26	36.3
overall nf	4.17				
Δ	0.23				
δ_i	0.29	0.29	3.21	0.26	33.12
χ_i	0.29	0.79	0.13	0.002	0.83
χ_i'	0.14	0.38	0.06	9.7e-4	0.4
Δ_i	0.032	0.032	0.35	0.03	3.69
new nf	1.517	1.517	6.02	2.23	32.6
new ov. nf	3.94				

which, in relative value, turns into:

$$\chi_i' = \frac{\chi_i}{\sum_i \chi_i} \tag{7}$$

If an improvement of value Δ is desired in the noise factor, the individual Δ_i values will be:

$$\Delta_i = \begin{cases} \Delta \cdot \chi_1' & \text{if } i = 1 \\ \Delta \cdot \chi_i' \cdot A_1 \cdots A_{i-1} & \text{if } i \neq 1 \end{cases} \tag{8}$$

When the current noise factor is within an ϵ of the desired one, $\Delta = nf_{current} - nf_{specs}$. Otherwise, Δ is a fraction of that difference. Since the gain distribution often changes along the process of optimizing all the parameters this measure leads to designs that meet specs while keeping the requirements of the individual blocks as relaxed as possible. A very small value of ϵ or of the factor that scales Δ may increase significantly the time for converging to a parameter distribution meeting specs. These values should be chosen carefully.

A similar procedure is followed when reassigning the linearity parameters. Since the equations are slightly different, using a multiplicative factor between the current and the new linearity values is more convenient. Taking:

$$IP_{3new} = \mu IP_3 \tag{9}$$

where IP_3 is the current IP3 value, makes the difference:

$$\frac{1}{IP_3^2} - \frac{1}{IP_{3new}^2} = \frac{1}{IP_3^2} - \frac{1}{\mu^2 IP_3^2} = \frac{\mu^2 - 1}{\mu^2 IP_3^2} = \frac{\mu_1^2 - 1}{\mu_1^2 IP_{3,1}^2} + A_1 \frac{\mu_2^2 - 1}{\mu_2^2 IP_{3,2}^2} + \cdots + A_1 \cdots A_{n-1} \frac{\mu_n^2 - 1}{\mu_n^2 IP_{3,n}^2} \tag{10}$$

This equation can be rewritten as:

$$\frac{1}{\eta} = \frac{1}{\eta_1} + \frac{A_1}{\eta_2} + \cdots + \frac{A_1 \cdots A_{n-1}}{\eta_n} \tag{11}$$

where $\frac{1}{\eta_i} = \frac{\mu_i^2 - 1}{\mu_i^2 IP_{3,i}^2}$.

Equation 11 is very similar to Equation 5. Therefore, an equivalent procedure to the one described by equations 5 to 8 is followed when computing the $\frac{1}{\eta_i}$ values. The obtained $\frac{1}{\eta_i}$

are ultimately converted to the μ_i scaling factors providing, thus, the new values for the IP_3 components.

The DR_{ADC} is calculated according to Equation 3. The noise and signal levels along the receiver blocks are calculated in order to be able to determine the signal of maximum power P_{max} and the noise power P_{noise} at the input of the ADC. The proper gain and filtering settings have to be applied for the different types of input signals. For instance, the maximum input signal will use the minimum gain option of the AGC loop and the in-band gain of the filters; the minimum input signal will use the maximum gain option of the AGC loop and the in-band gain of the filters; blockers and adjacent channels will use the maximum gain option and the attenuation provided by the filters at their offset frequencies from the desired channel (worst case scenario). If the ENOB specs are not met, the gain of the AGC is adjusted, the filtering specs are hardened or both. The probability of choosing each of these options depends on the origin of the signals that determine the ADC dynamic range.

The routine that changes the gain distribution has to determine both the direction of the change (increase or decrease the gain) and the amount of gain change to be introduced. When only the noise figure specs are not met, the routine will increase the front-end gain. The opposite will happen when only the linearity specs are not met. In this situation, the front-end gain will be decreased. In the event of both the noise figure and linearity specs not being met, changes of random direction are made in the gain distribution. When changing the gain, it is ensured that the new gain value is within the range limits. The absolute value of the gain variation is random within these limits.

In a receiver chain, there are blocks with variable gain and blocks with fix gain. When the multi-standard case is being evaluated, the gain changes for the blocks with programmable gain are introduced with probability one. If the block is not programmable in gain, the gain reassignment is taken into consideration with a very small probability. Depending on the gain values the various standards try to assign to a block and the direction they are trying to push the new value to, a different gain value will be resolved.

4.4 Power Considerations

The proposed multi-standard budget design tool is implementation independent. Hence, it is not possible to perform a fairly accurate power consumption estimation. Power is, nevertheless, one of the major concerns in circuit design. Therefore, the optimization algorithm takes some high-level general measures that help keeping the power consumption low:

- $x_{initial} = x_{r,1} \ldots x_{r,B}$. Small gain, higher NF, smaller IIP's mean less current.
- The order of the filters is increased only when it is absolutely needed. Smaller order means less filtering stages and, therefore, less area and power consumption coming from the filters.
- ADC with as small DR as possible.

4.5 Block Reuse and Reliability Issues

Having the whole design flow of an RF receiver from system to silicon into focus, the use of a high level tool such as the one described in this paper can save a significant amount of time and manpower. In comparison with their digital counterparts, the analog and RF blocks have an extremely large design cycle. The level of uncertainty between simulated and fabricated circuits and the limitations of the available automated design tools for analog circuits worsen this situation. Intellectual Property (IP) block reuse is, therefore, very important not only due to the time save it entails but also due to reliability issues. Including already tested blocks in a new design increases the chances of first pass success.

The proposed tool and methodology help RF designers in taking the right choices at system level increasing, thus, the

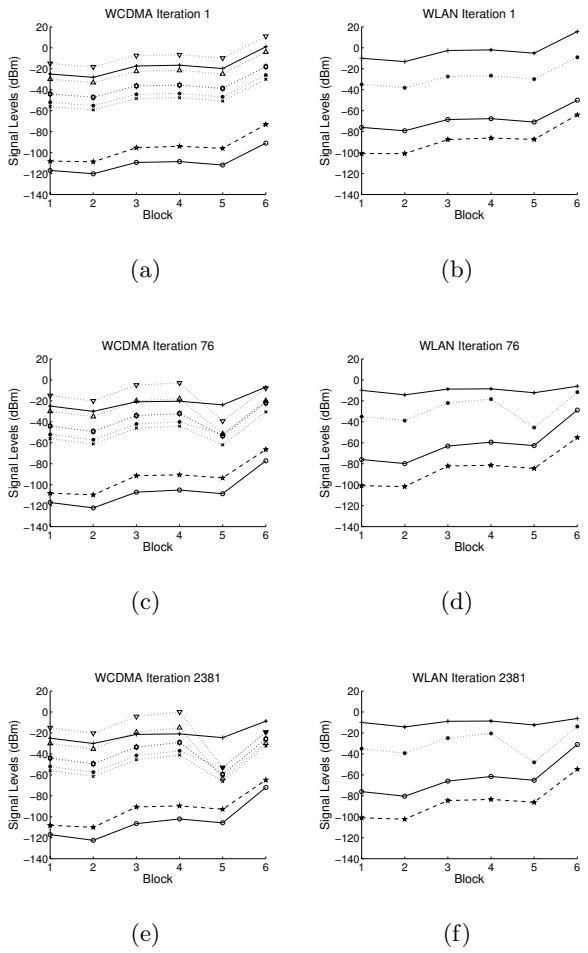


Figure 3: Evolution of the signal levels along the blocks for WCDMA and WLAN for different simulation steps. The WCDMA signals shown in 3(a), 3(c) and 3(e) correspond to: + P_{max}, o P_{min}, * Adjacent Channel at 5 MHz offset, x Adjacent Channel at 10 MHz offset, □ Adjacent Channel at 15 MHz offset, ◇ Out-of-band Blocker at 15 MHz offset, ▽ Out-of-band Blocker at 60 MHz offset, △ Out-of-band Blocker at 85 MHz offset, ★ Noise Floor. The WLAN signals shown in 3(b), 3(d) and 3(f) correspond to: + P_{max}, o P_{min}, * Adjacent Channel at 25 MHz offset, ★ Noise Floor

Table 2: Summary of the WCDMA (TDD) and WLAN(802.11b) RF specifications.

Parameter	WCDMA	WLAN
RF Frequency Band	2010-2025 MHz 1900-1910 MHz	2400-2485 MHz
RF Channel Bandwidth	3.84 MHz	20 MHz
Channel Separation	5 MHz	5/25 MHz
Sensitivity	-117 dBm	-76 dBm
Max Power Level	-25 dBm	-10 dBm
Adjacent Ch. Selectivity	33 dB	35 dB

chances of first pass success. Reducing the probability of silicon re-spins, common in analog and RF designs, months can be saved in a project [8].

5. SIMULATION RESULTS

The budget design methodology described in Section 4 was tested using the design of a WCDMA/WLAN multi-standard receiver as a benchmark. The radio characteristics of these two standards are summarized in Table 2 [9, 10].

We have chosen a zero-IF receiver architecture, widely used in multi-standard receivers, for the examples shown in the following sections.

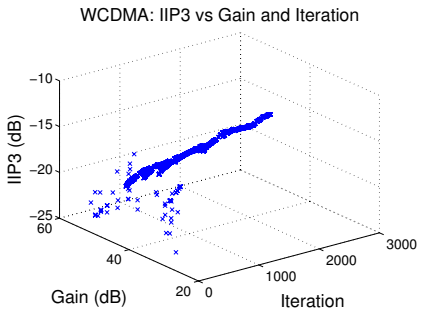
5.1 Evolution of the Budget Design

The RF standard specs (summarized in Table 2) are mapped into receiver specs [11]. The resulting receiver specs are shown in Table 3. In order to find a parameter distribution meeting these receiver specs using the zero-IF shown in Figure 1 the budget design tool is executed.

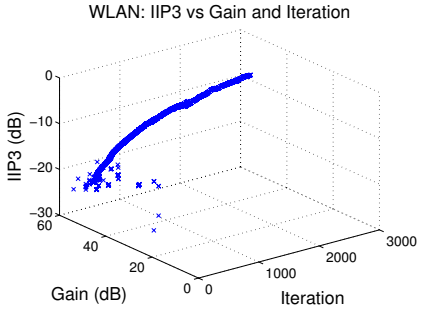
Figure 3 illustrates one aspect the evolution of the optimization process of the WCDMA/WLAN multi-standard budget. The resulting signal levels along the receiver blocks are shown at three simulation steps. The level of the desired input signals (maximum and minimum option), adjacent channels, blockers and noise floor is plotted against the different blocks. These signal levels are shown at the input of the RF filter (1), the LNA (2), the mixer(3), the baseband filter (4), the baseband VGA (5), and the ADC (6).

The redistribution of the block characteristics performed during the optimization of the budget makes these signals evolve with the simulation step as illustrated in this figure. The distribution of the gain, noise figure, linearity performance, and filtering characteristics changes along with the simulation step. These parameters are readjusted in order to meet the requirements shown in Table 3. Note how in time this adjustments attenuate adjacent channels and out of band blockers that may interfere with the desired signal. This figure shows how the power level of the signals along the blocks is adapted in time to meet the performance levels set by the wireless communication standards.

As an example, Figure 4 shows how the IIP3 evolves in a typical run for WCDMA and WLAN as a function of the gain and iteration number. IIP2, NF, and DR_{ADC} convergence to the goal values in a similar manner. Their plots are not shown here for the sake of brevity.



(a)



(b)

Figure 4: Evolution of the cascaded IIP3 for 4(a) WCDMA and 4(b) WLAN for a typical run

Table 3: Specifications and performance of a typical run for a WCDMA/WLAN multi-standard receiver.

Standard	WCDMA		WLAN	
Parameter	Specs	Result	Specs	Result
$DR_{ADC}(dBm)$	60	58.3	49	48.9
$ENOB_{ADC}$	10	9.3	8	7.8
$Gain(dB)$	-	45.5	-	47.4
$NF(dB)$	9	6.4	11	7.7
$IIP3(dBm)$	-17	-15.6	-5	-4.8
$IIP2(dBm)$	14	27.6	23	28.1

5.2 A Budget Design Example

Table 3 summarizes the performance achieved by a receiver with the parameter distribution shown in Table 4. This results come from a typical run of the tool. In this example, the resulting RF filters are centered around the bands shown in Table 2. They are Butterworth bandpass filters of 2^{nd} (WCDMA) and 3^{rd} order (WLAN). The baseband filters are lowpass Butterworth filters with a cutoff frequency equal to the baseband channel bandwidth (half of the RF channel bandwidth shown in Table 2). They are filters of 4^{th} (WCDMA) and 6^{th} order (WLAN).

Table 4: Parameter distribution for the proposed WCDMA/WLAN multi-standard receiver.

WCDMA					
Parameter	RF filter	LNA	Mixer	BB filter	VGA
Gain (dB)	-3.74	15.52	4.24	-3.56	33.00
NF (dB)	2.57	2.28	5.89	9.75	10.26
IIP3 (dBm)	3.23	-0.30	1.69	3.23	4.38
IIP2 (dBm)	40.00	35.00	55.00	45.00	50.00
WLAN					
Parameter	RF filter	LNA	Mixer	BB filter	VGA
Gain (dB)	-3.74	14.93	4.24	-3.52	35.55
NF (dB)	3.17	2.59	6.76	12.63	12.89
IIP3 (dBm)	13.42	11.05	12.44	13.42	13.73
IIP2 (dBm)	40.00	35.00	55.00	45.00	50.00

Table 5: Execution time results

Benchmark	$t_{min}(s)$	$t_{max}(s)$	$t_{mean}(s)$	σ
WCDMA/WLAN	3.07	25.47	9.69	3.73

5.3 Timing analysis

The budget optimization is based on simulated annealing. Its execution time is non-deterministic and very dependent on the cooling temperature and the goal functions. Table 5 shows the maximum, minimum, mean and standard deviation of the execution time for the specs shown in Table 3. The statistics are calculated over 200 runs of the tool.

5.4 Comparison with other Tools

The low execution time shown in Section 5.3 is due to the fact that this is an implementation independent high level tool. A similar design carried out using the already available tools mentioned in Section 2 would take much longer time. Our approach is, hence, very good as a first step when designing an RF receiver, especially if the multi-standard case has to be considered. It cannot be used alone though. For the frequency settings and an interference oriented frequency planning the results from [12] have been fed into the tool described herein.

Once the receiver specs have been set using our approach, tools providing more accurate models should be used so that further non-idealities can be accounted for (see Section 2). Final adjustments in the block specs may have to be done at this point. It is recommended to provide some margin in the cost functions when doing the budget design using our tool in order to minimize the number of design iterations.

6. CONCLUSIONS

A design and optimization methodology that can be used for system level specification of wireless communication multi-standard receivers has been proposed in this paper. This methodology has been implemented in a tool.

The focus of the proposed methodology is to meet or exceed specs without overdesigning the receiver blocks. The developed impact oriented parameter distribution allows for a fast convergence of the algorithm while serving the purpose of not setting too tough requirements in blocks where it is not needed.

The use of this tool/methodology helps RF engineers in the design of receiver budgets for different receiver architectures. This may help reducing the number of silicon spins and consequently the time-to-market. The usefulness of this tool has been shown through a design example of a WCDMA/WLAN multi-standard zero-IF receiver.

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