Reliability Simulation based on Verilog-A

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Behavioral Modelling And Simulation conference

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Outline

- Device Degradation and Circuit Reliability
- Reliability Physics
- Reliability Models
- Reliability Simulation
- NBTI Model in Verilog-A
- Experiments
- Conclusions

Device Degradation and Circuit Reliability

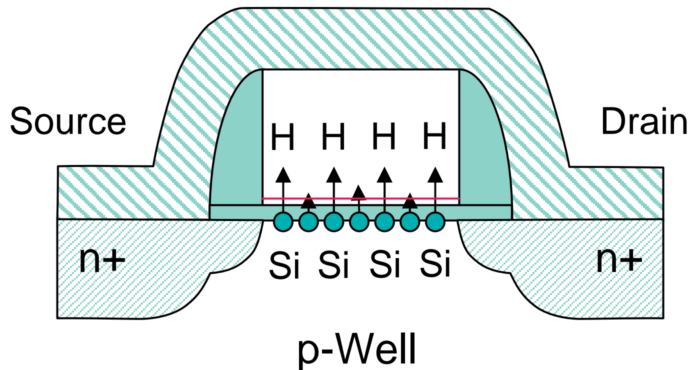
- Initial research kicked off by request for reliability effects inside standard MOSFET models
  - BSIM4, MOS Model 11
  - For 90nm CMOS processes and beyond
  - Initially aimed at NBTI* effect
  - CHC† to be added later
- Issue – there is no model for NBTI
  - Did not want to introduce volatile model code in existing models
  - Concerns on overhead of reliability models
- Solution required for simulating circuit-level reliability

Image courtesy of Freescale Semiconductors

* NBTI = Negative Bias Temperature Instability
† CHC = Channel Hot-Carrier

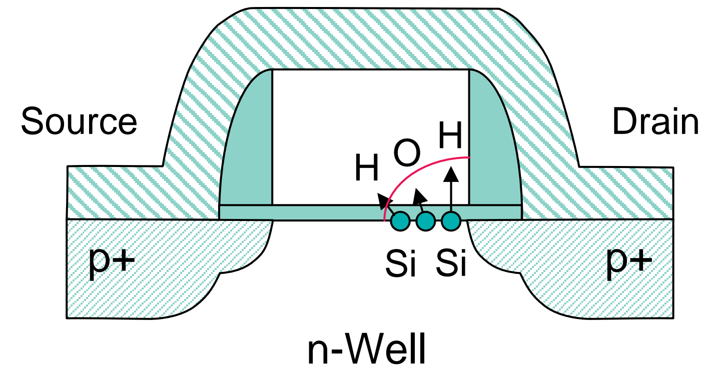
Reliability Physics

- Both HCI and NBTI can be attributed to charges at the Si – SiO_2 interface
  - NBTI related to breaking of Si – H bonds in PMOS devices
  - CHC related to both Si – H and Si – O bonds in NMOS devices



PMOS with NBTI effect

1D hydrogen diffusion

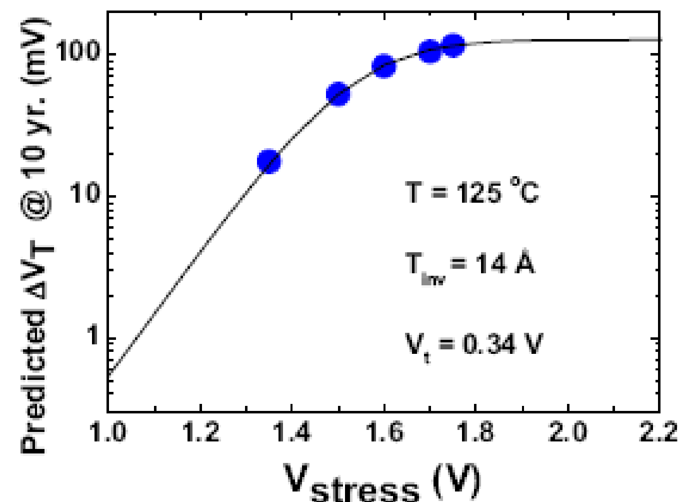


NMOS with CHC effect

2D charge trapping

Reliability Physics

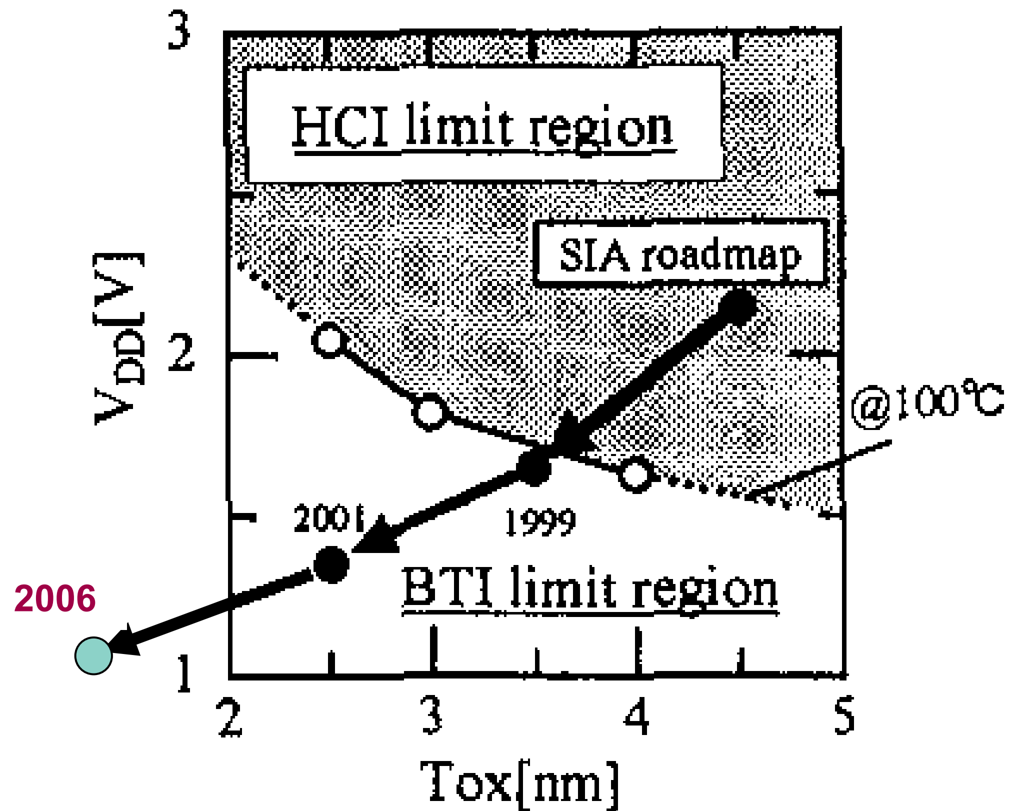
- NMOS devices with modern gate dielectric materials ($SiON_x$ or high-k materials) may exhibit PBTI
  - Similar degradation mechanism to NBTI
  - Occuring in NMOS devices under positive bias situations
- NMOS reliability model may need to support two mechanisms
  - CHC during switching transients (current related)
  - PBTI during constant voltage stress



A. Kumar et al, SISPAD 2006

NBTI and Circuit Reliability

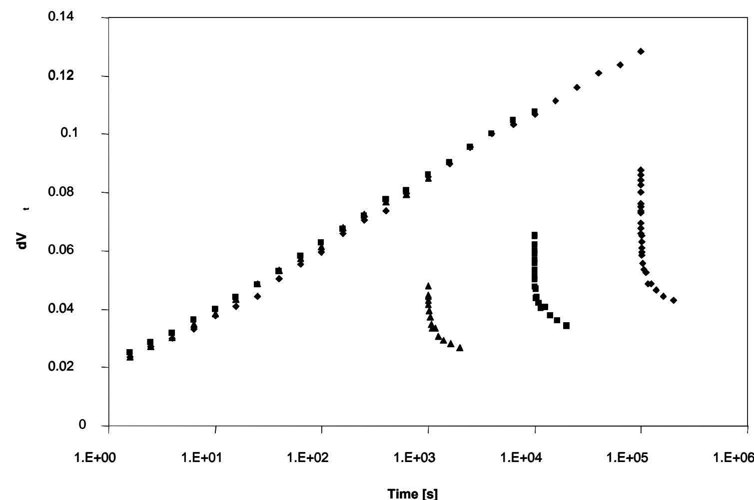
- NBTI has two main effects
  - V_{th} shift due to charge buildup in the gate dielectric
  - Mobility (μ) reduction due to interface traps at the channel surface
- Recovery effect makes models complicated
- Probably two degradation + two recovery effects active
  - Related to hydrogen diffusion through gate dielectric and gate polysilicon



N. Kimizuka et al, VLSI Tech 1999

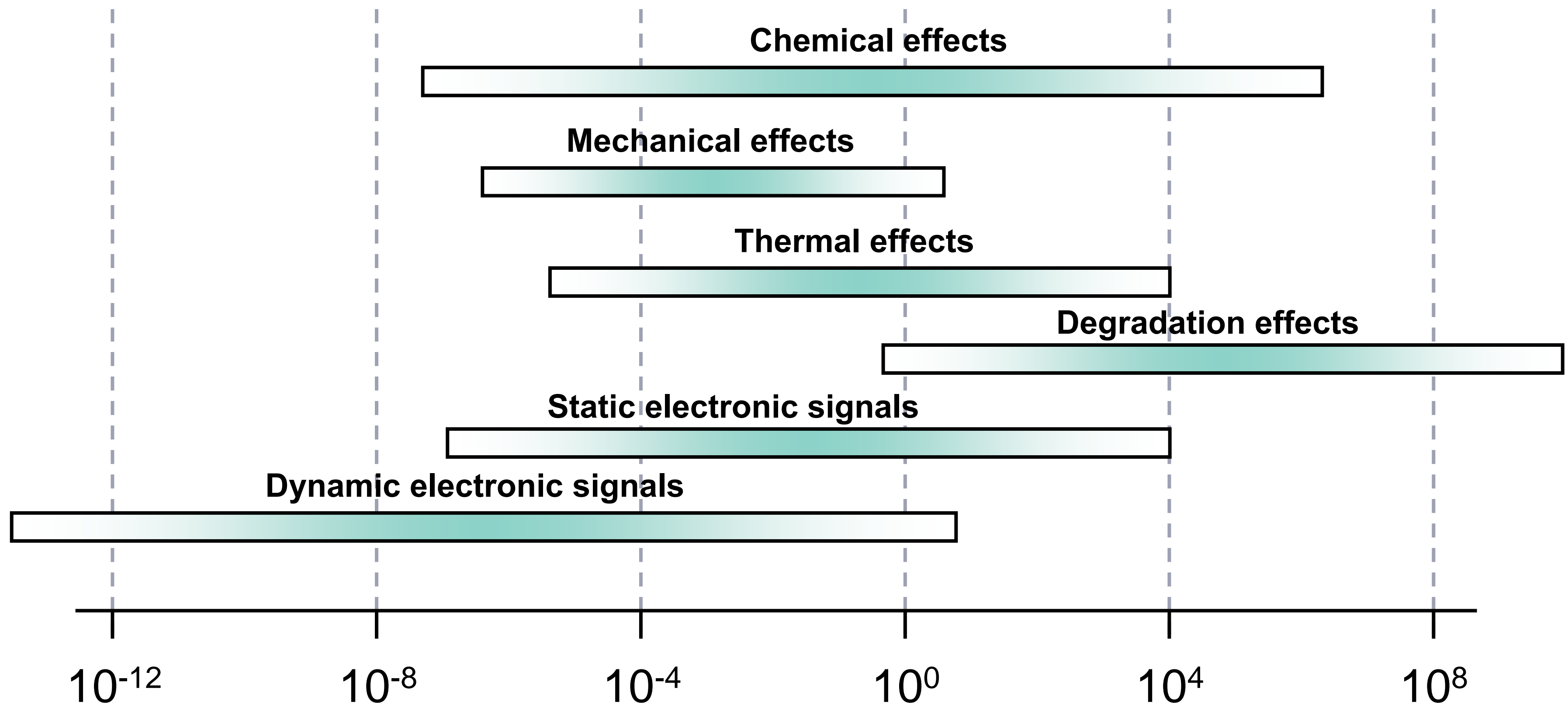
Reliability Models and Simulation

- NBTI Models are still in a state of flux
  - Very much dependent on material
  - Recovery effects are present that (partially) undo the damage of interface charge generation
- Most NBTI models still used for TCAD applications
  - Targeted at process optimization
  - Not for circuit simulation
- A dynamic environment is required because of development state.
  - Compact modelling capabilities
  - Not bound to a single circuit simulation flow.
- Solution: Verilog-A



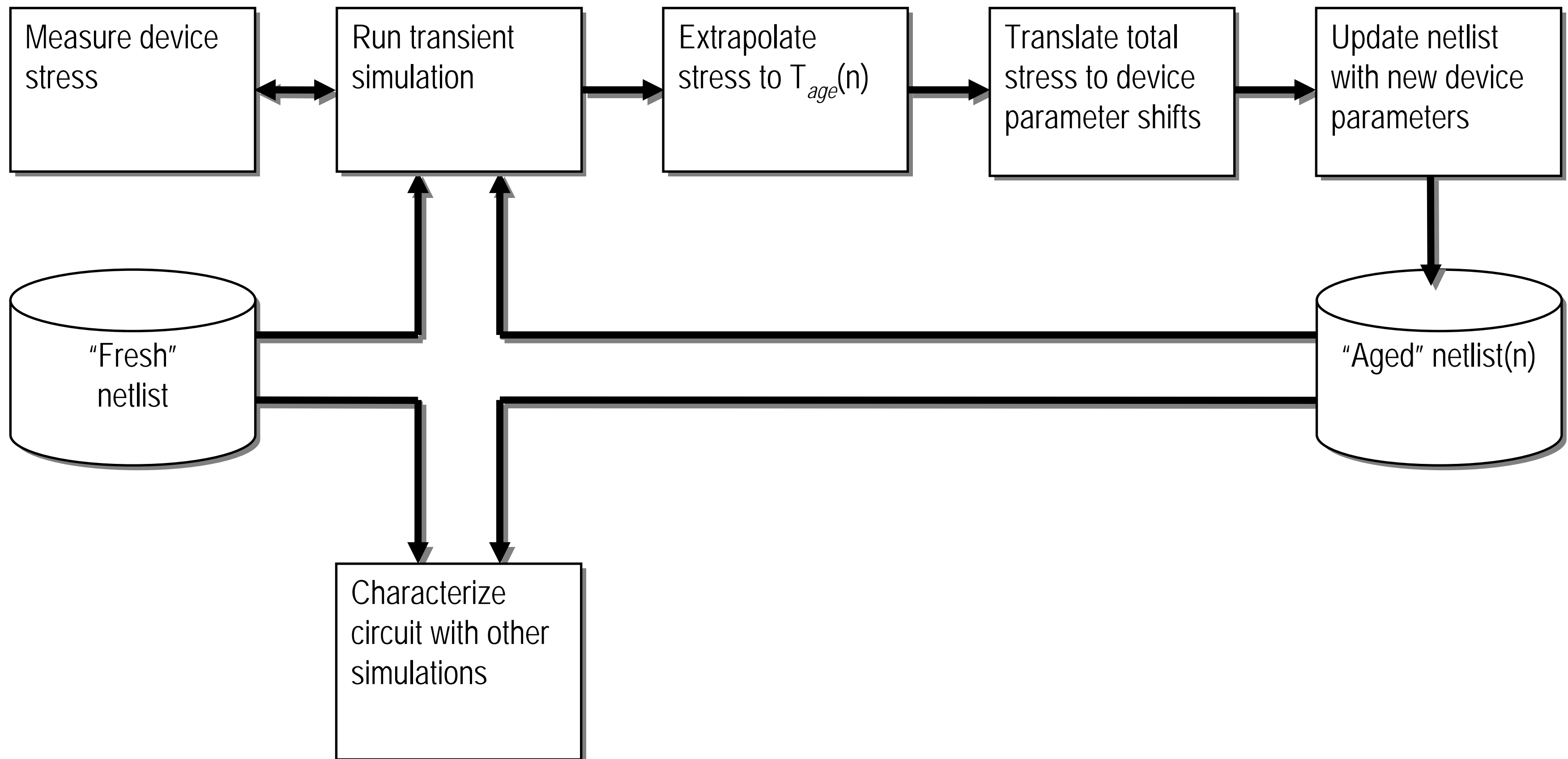
Reliability Simulation

- Based on separation of time scales
  - No “hyperacceleration” to prevent undesired mixing effects



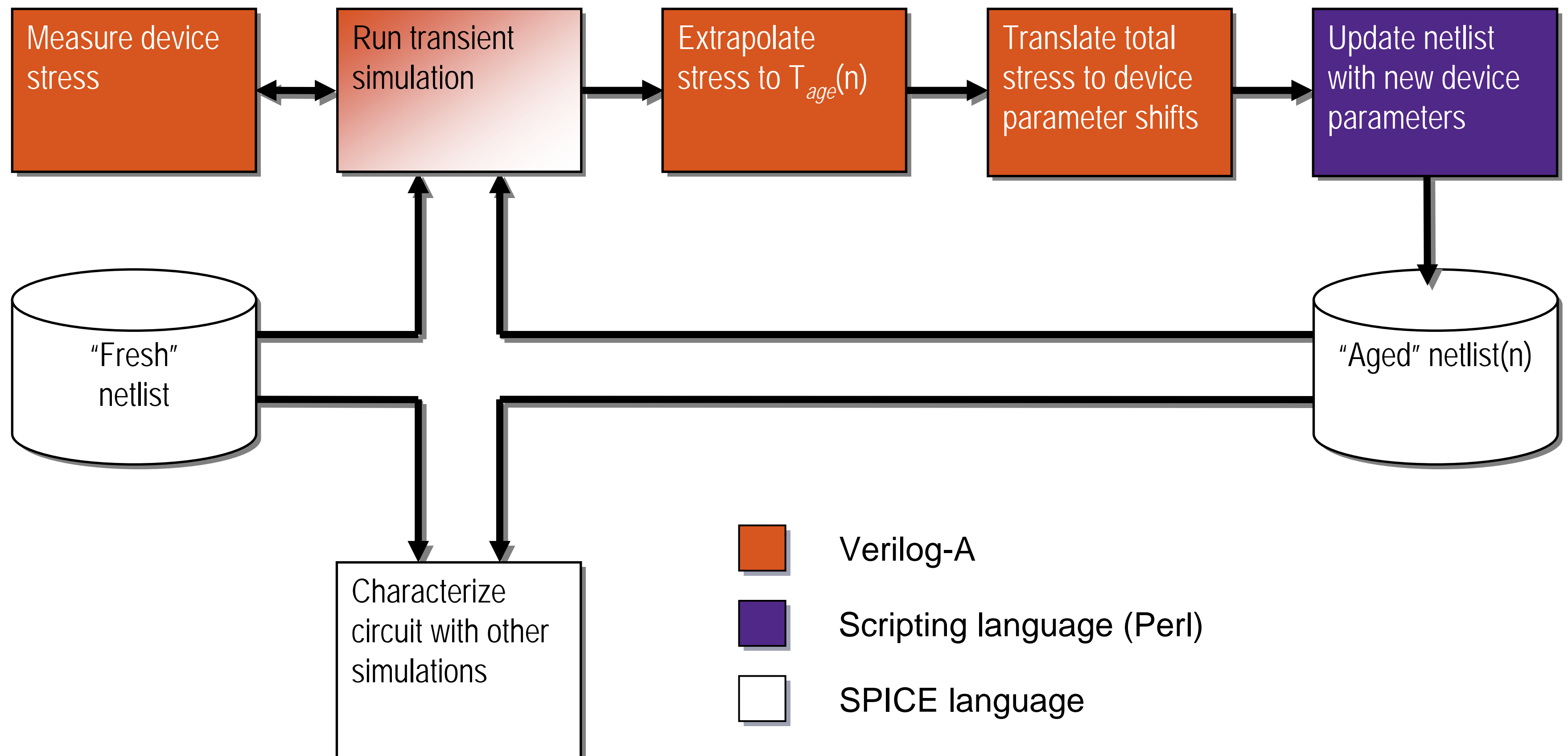
Iterative Reliability Simulation

- BERT (BErkeley Reliability Tool) methodology (C. Hu, Microelec.J. 1992)



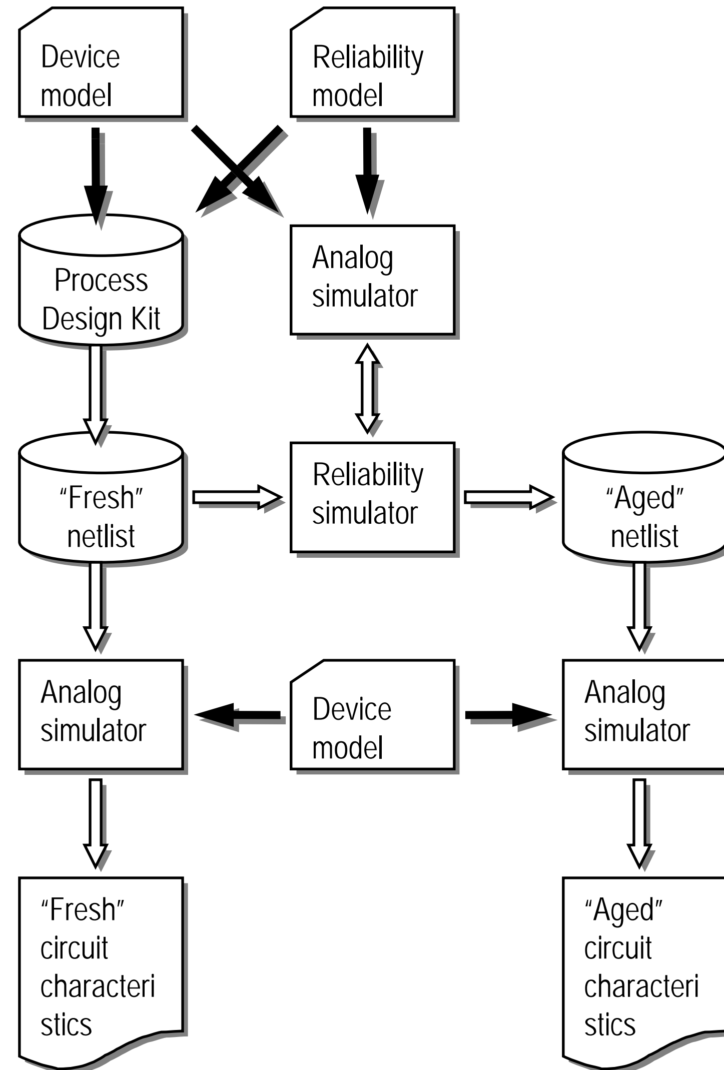
Reliability Simulation based on Verilog-A

- PRESTO (Presto REliability Simulation TOol)



Circuit-level Reliability Simulation

- Requirements
  - Circuit netlist
  - PDK*
- Simulator
  - Support for Verilog-A
  - Support for instance-based netlist update
    - **alter** statement in Spectre
    - **.STEP** statement in Eldo
- Reliability Simulator
  - Reliability Models piggybacked on MOSFET instances



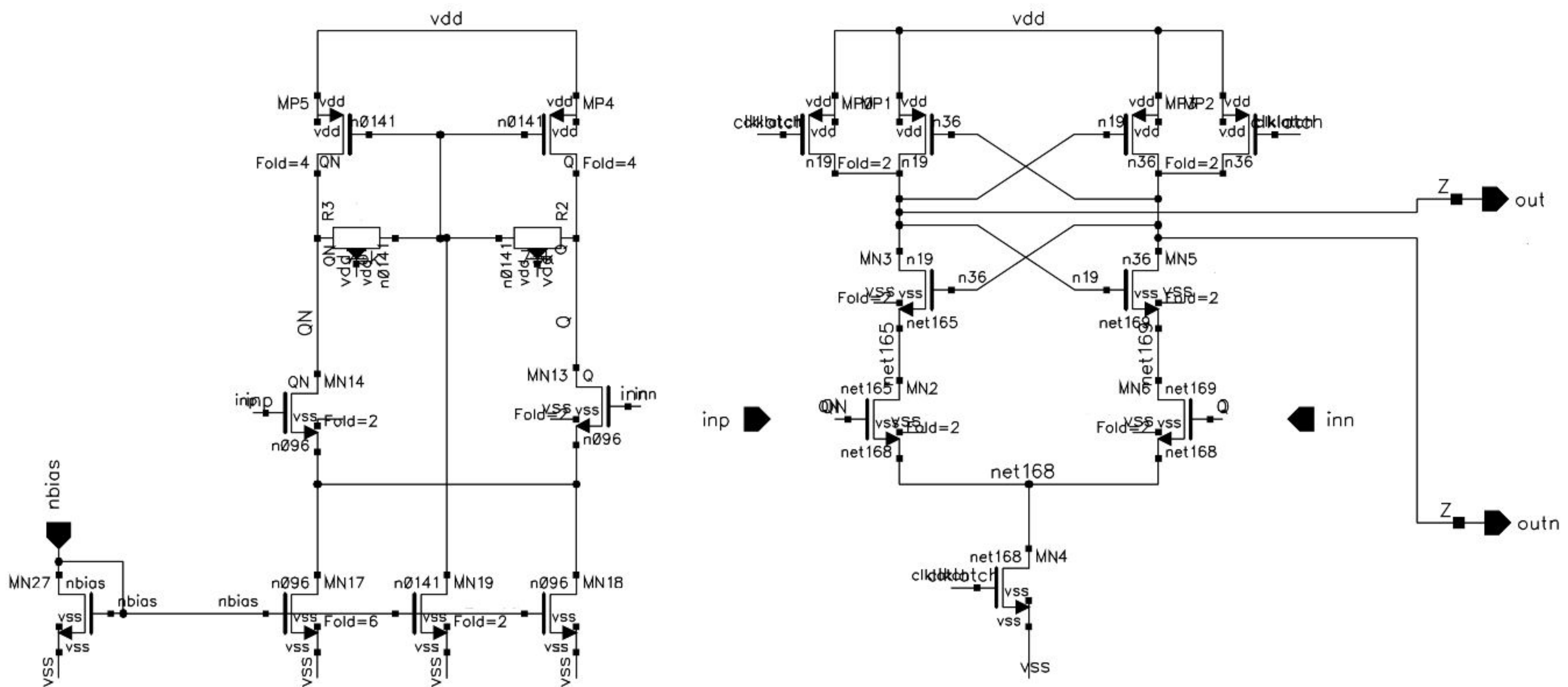
* PDK = Process Design Kit
† CHC = Channel Hot-Carrier

Verilog-A Code of NBTI Model

```
`include "disciplines.vams“

`define XML_FILE_NAME "nbti.xml"

module mnbti (d, g, s, b);
inout d, g, s, b;
electrical d, g, s, b;

parameter integer active = 1 from [0:1];
parameter real dta = 0.0;
parameter real tage = 0.0 from [0:inf);
parameter real tstart = 0.0 from [0:inf);
parameter real tstop = 1.0e+34 from (tstart:inf);
parameter real alpha_dp = 0.0;
parameter real VG_dp = 0.0;
parameter real Ea_dp = 0.0;
parameter real n_dp = 1.0;
parameter real tsat_dp = 1.0e+06 from [0:inf);
parameter real Vfb = 0.0;

localparam real eq_stress_time = tstop - tstart;

branch (g, d) gd;
branch (g, s) gs;
branch (d, b) db;
branch (s, b) sb;

integer stressed, calculate, update_file;

real vgs, exp_temp_dp, c_dp, exp_vg_dp, eq_vgs, dp, delta_vfb;
real eq_nbti_dp, eq_time, eq_stress_time_int;

analog begin
  // Initialization
  @(initial_step)
    if (active && analysis("tran") && (tage > 0)) begin
      update_file  = $fopen(`XML_FILE_NAME);
      calculate = ((alpha_dp == 0) || (Ea_dp == 0)) ? 0 : 1;
    end

// Stress measurement
  if (calculate) begin
    // activation flag to sync with user specified tstart and tstop
    stressed = ($abstime > tstart) ? (($abstime > tstop) ? 0 : 1) : 0;
    vgs = (abs(V(db)) >= abs(V(sb))) ? V(gs) : V(gd);
    if (vgs > 0) vgs = 0; // positive bias not taken into account
    exp_temp_dp = Ea_dp / $vt($temperature + dta);
    exp_vg_dp = VG_dp * abs(vgs);
    c_dp = alpha_dp * exp(-exp_temp_dp) * exp(exp_vg_dp);
    // Permanent damage calculation
    eq_nbti_dp = idt(((exp_vg_dp == 0) || !stressed)
      ? 0.0 : pow(c_dp, 1.0/n_dp), 0.0);
    eq_time = idt((!stressed) ? 0.0 : 1.0, 0.0);
  end // if calculate

  // Output of  stress data
  @(final_step)
    if (calculate) begin
      // saturation after a certain time
      eq_stress_time_int =
        (eq_stress_time >= tsat_dp) ? tsat_dp : eq_stress_time;
      dp = (eq_time > 0.0)
        ? pow(abs(eq_nbti_dp) * eq_stress_time_int/eq_time, n_dp)
        : 0.0;
      // the computation of parameter changes is done right here
      delta_vfb = dp * tage/eq_stress_time;
      if (-delta_vfb) begin
        $fwrite(update_file, " <instance name=\"%M\">\n");
        $fwrite(update_file, "  <parameter name=\"%s\"", "vfb");
        $fwrite(update_file, "  value=\"%1.8g\" delta=\"%1.8g\"/>\n",
                    Vfb, -delta_vfb);
        $fwrite(update_file, " </instance>\n");
      end
      $fclose(update_file);
    end // if calculate

end // analog

endmodule // mnbti
```

Example Circuit

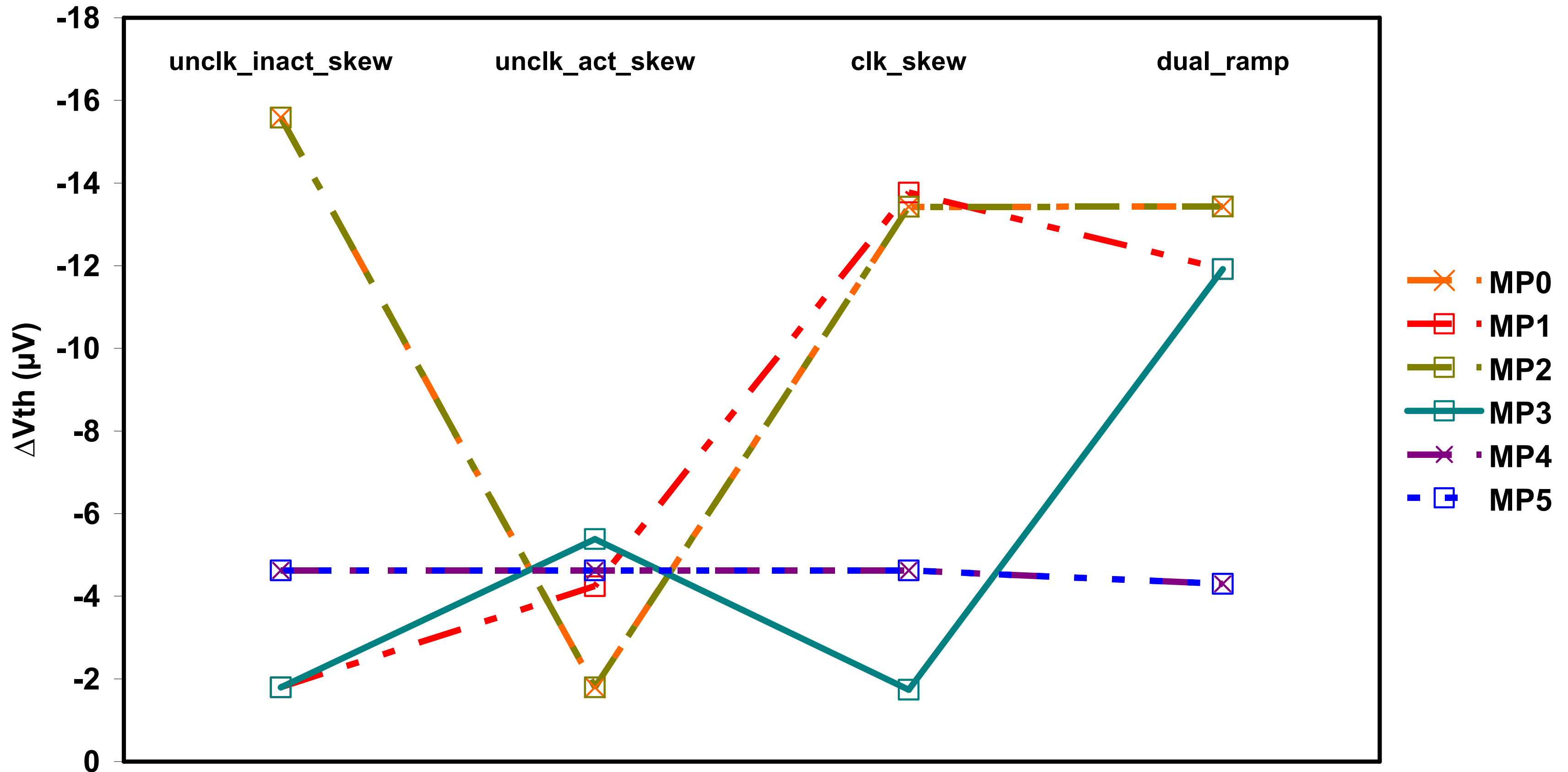
- Latched comparator for SAR ADC in 65nm CMOS process
- Design inverted to use PMOS i.s.o. NMOS and vice-versa



Experiments

- Four situations:
  1. Regular operation, clock active, slow triangle waveform input
  2. Regular operation, clock active, constant DC skewed input
  3. Standby operation, clock inactive, constant DC skewed input
  4. Powerdown, clock inactive, constant DC skewed input
- Supply voltage 1.2V
- Junction temperature 65ºC = 338 K
- Common mode input = 0.8V

Simulation results



Conclusions

- An open framework for circuit-level reliability simulation
  - Using Verilog-A for modelling of the degradation effects
  - Simple postprocessing yields aged parameter sets
  - Impact of degradation on circuit performance can be readily determined
- Reliability model of NBTI effect to be developed further for dynamic behavior
  - Recovery information is collected and subtracted from final result
- Dynamic reliability requires different simulation approach
  - Currently not possible to reproduce “J”-curves for recovery.
  - Not necessary for circuit-level reliability