Phase Change Memory Modeling Using Verilog-A

Yi-Bo Liao, Yan-Kai Chen, Meng-Hsueh Chiang

Department of Electronic Engineering, National Ilan University

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Outline

- Introduction
  - Phase change memory (PCM)
- Motivation
- Modeling using Verilog-A
- Results

Introduction

- Non-volatile memory (NVM) has been very popular for data storage.
- Phase change memory is promising for the next generation memory device, with the following features:

  1) Good scalability

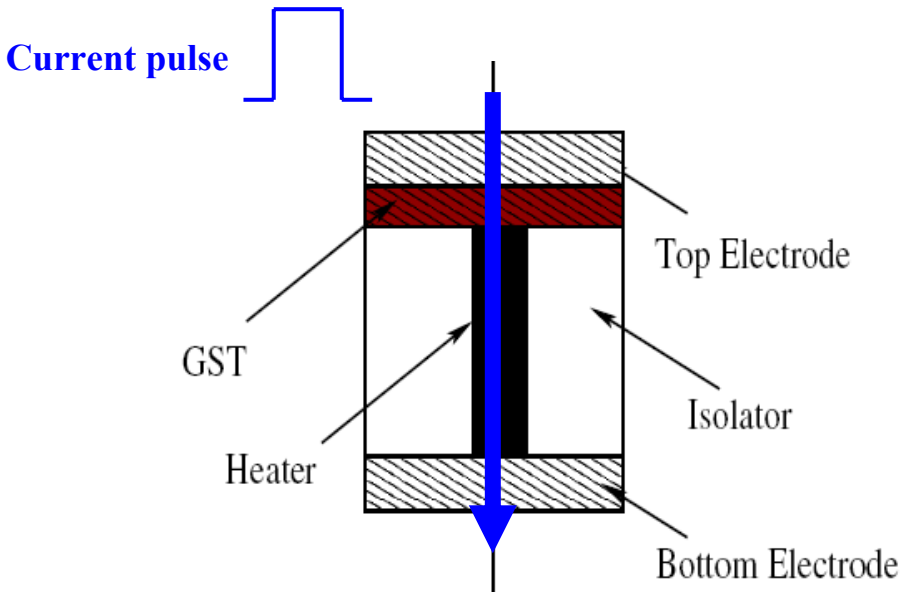
  2) Fast read/write (<100ns)

  3) Low power operation

  4) Good reliability (>10^6)

Phase Change Memory (PCM)

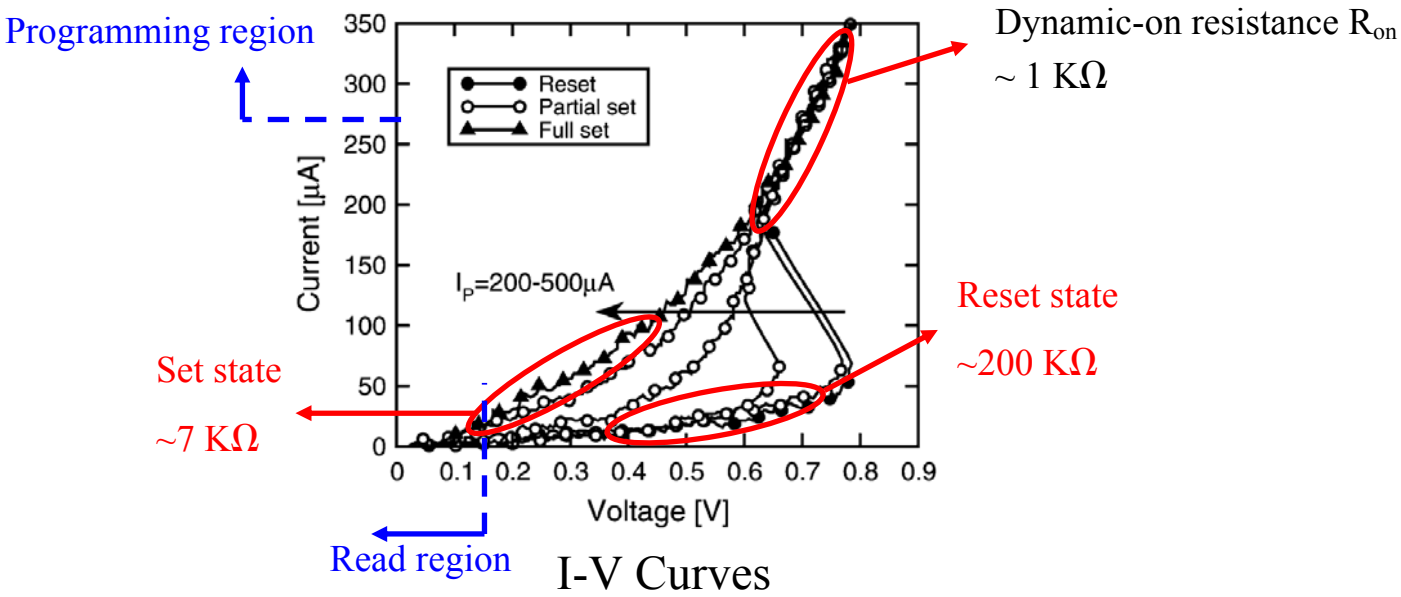
- PCM first presented by S. Ovshinsky in 1968.
- The material is based on $Ge_2Sb_2Te_5$(GST).
- The phase state can be changed by the heat (current pulse).



Ref. M. Gh. Mohammad, L. Terkawi, and M. Albasman, "Phase Change Memory Faults," *Proceedings of the 19th International Conference on VLSI Design*, 2006.

Phase Change Memory (PCM)

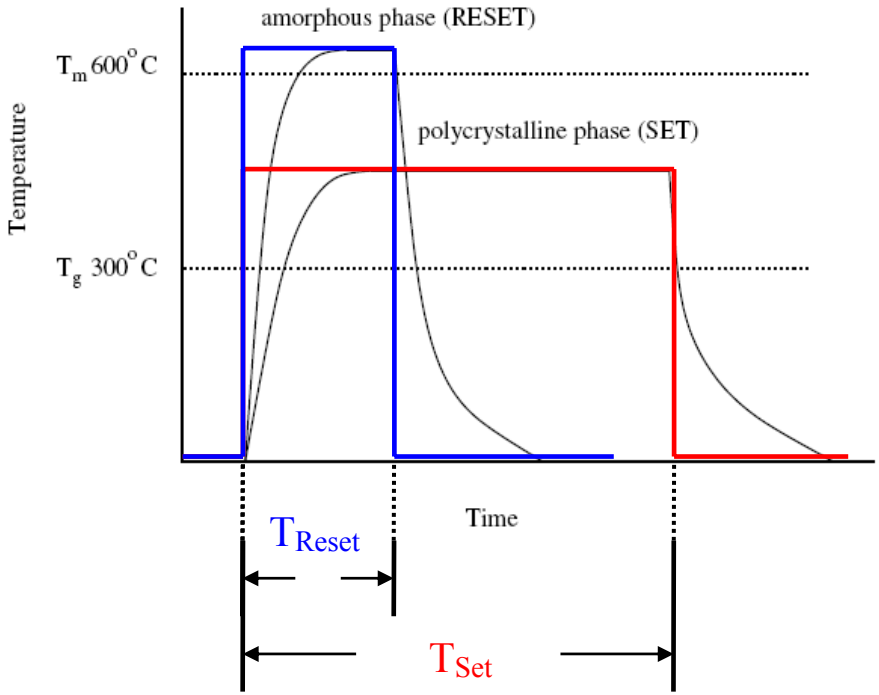
- PCM has two static states (phases)
  - Crystalline state (Set state) → Low resistance
  - Amorphous state (Reset state) → High resistance



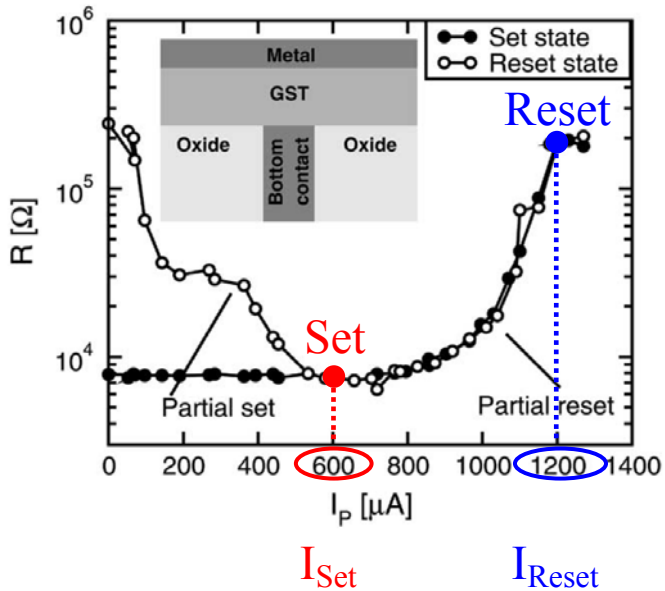
Ref. D.Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer, and R. Bez, "Analysis of phase distribution in phase-change nonvolatile memories," *IEEE Electron Device Letters*, Vol. 25, pp. 507-509, July 2004.

Phase Change Memory (PCM)

- PCM state will be changed by current pulse
  - Programming to Set state
  - Programming to Reset state



R-I Curves



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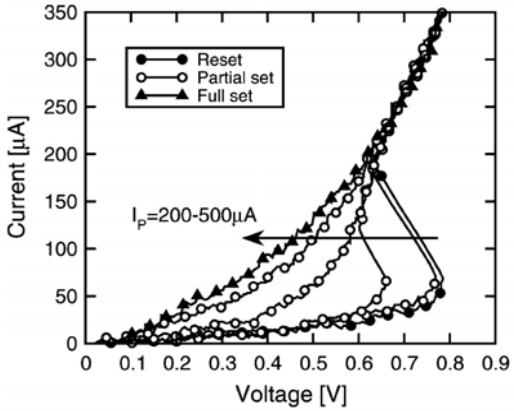
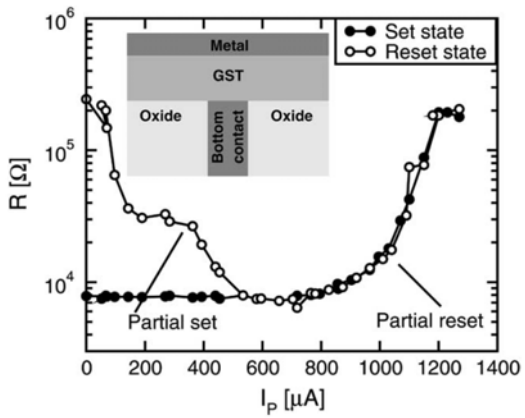
Extract Data

- The typical parameters of the proposed PCM model





Parameter	Value
Static resistance of Set (R_{Set})	7KΩ
Programming current of Set(I_{Set})	600μA
Programming time of Set (T_{Set})	100ns
Static resistance of Reset (R_{Resett})	200KΩ
Programming current of Reset (I_{Reset})	1200μA
Programming time of Reset (T_{Reset})	50ns
Holding voltage (V_h)	0.45V
Threshold voltage (V_{th})	0.78V
Dynamic-on resistance (R_{on})	1KΩ

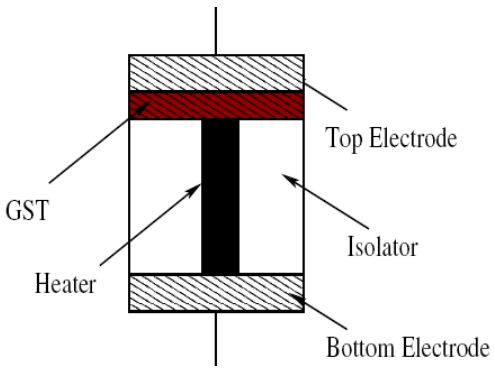
Ref. D.Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer, and R. Bez, "Analysis of phase distribution in phase-change nonvolatile memories," *IEEE Electron Device Letters*, Vol. 25, pp. 507-509, July 2004.

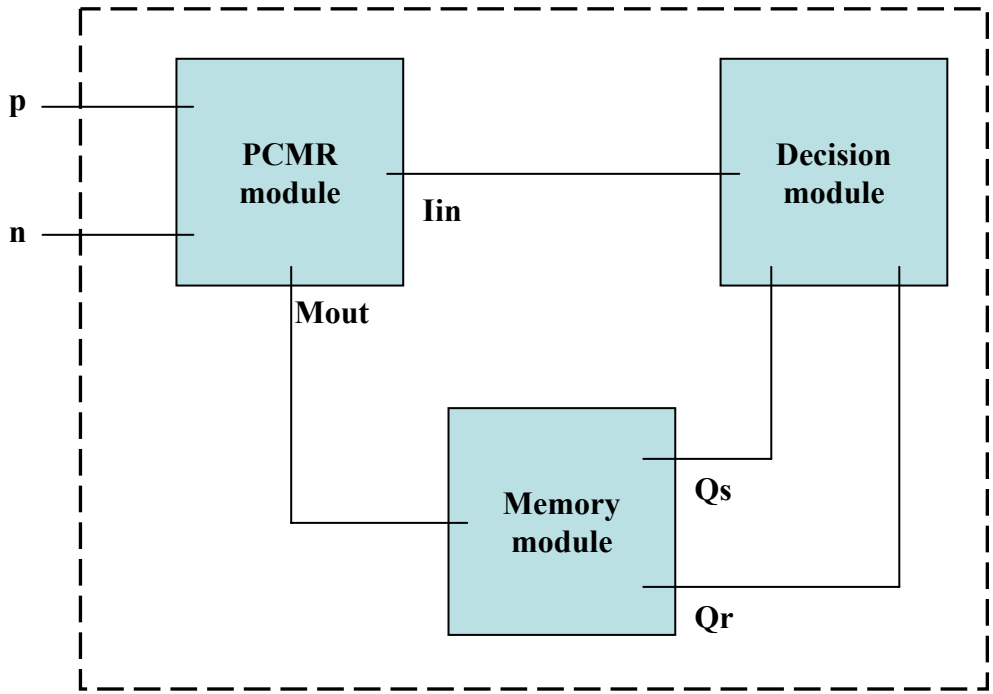
Motivation

- PCM has a very nonlinear I-V relation, especially with the snapback characteristic.
- Convergence problem in SPICE simulator
  - When using too many dependent sources/switches
- Verilog-A provides a simple tool for behavior modeling and for implementing nonlinear equations.

Modeling

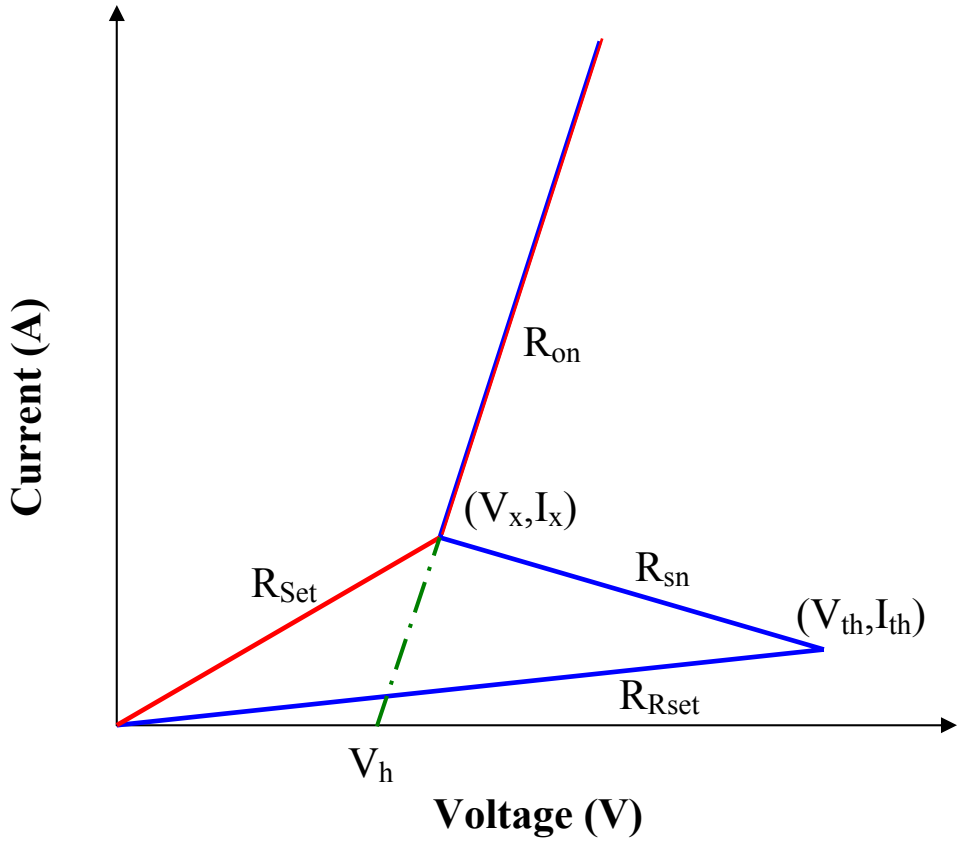
- The model block chart





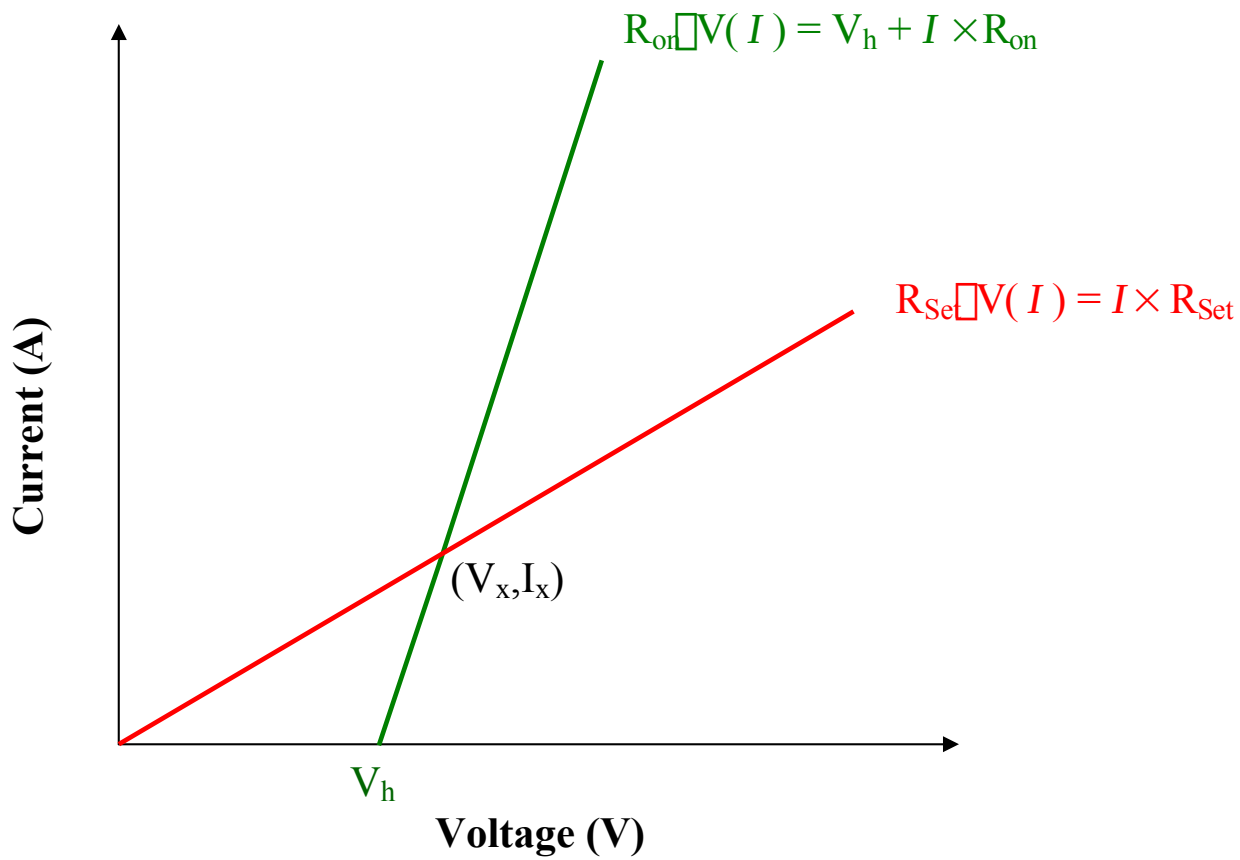
PCMR Module

- To describe the I-V curves of the PCM
- There are two independent I-V curves



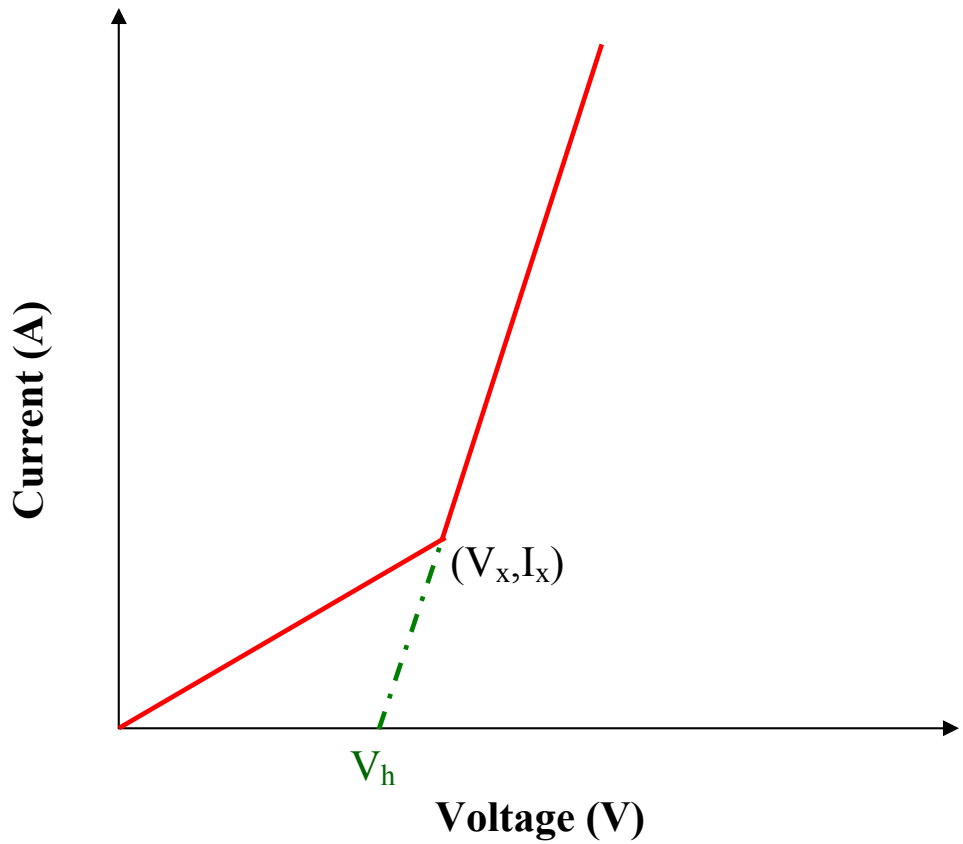
PCMR Module

- The I-V curve of the Set state



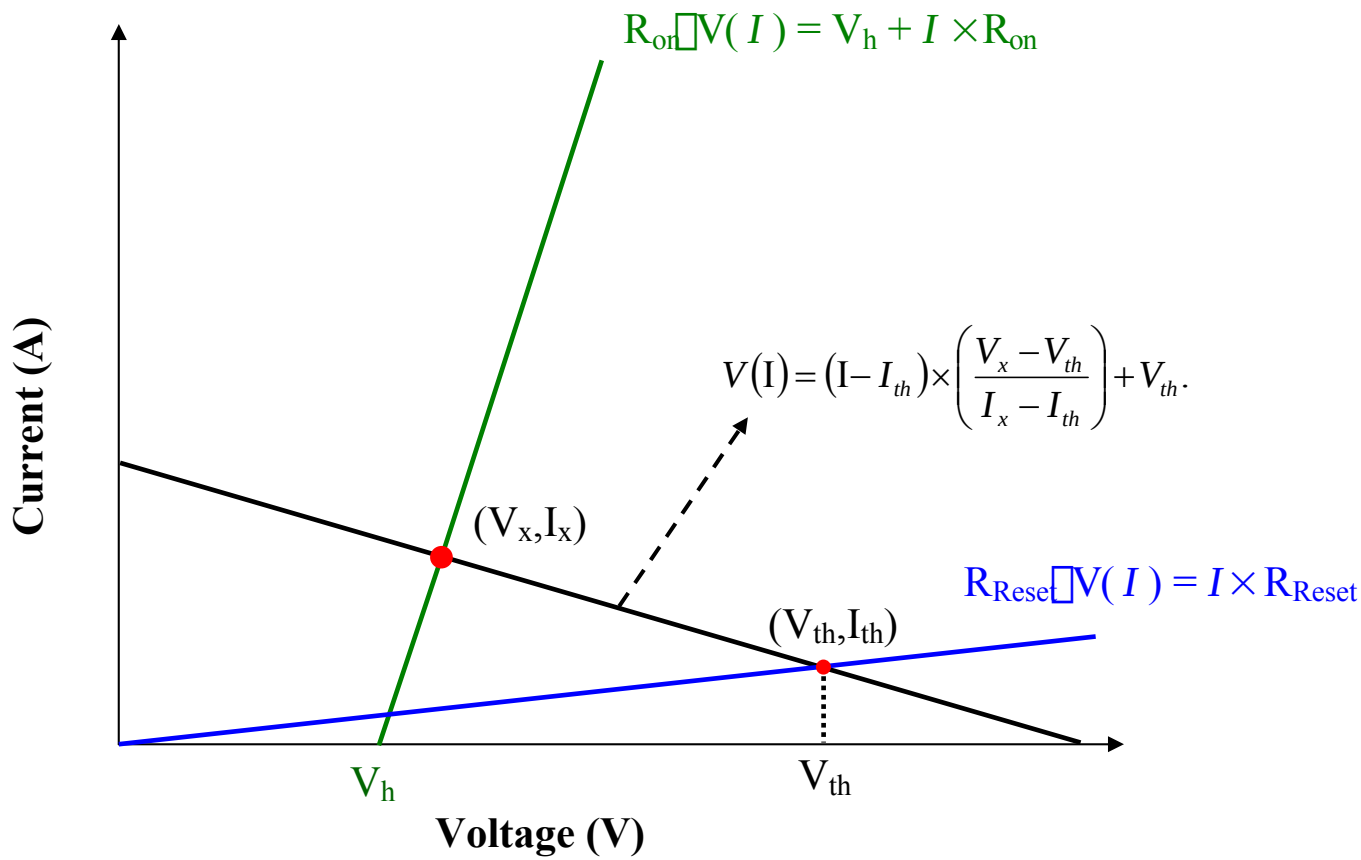
PCMR Module

- The I-V curve of the Set state



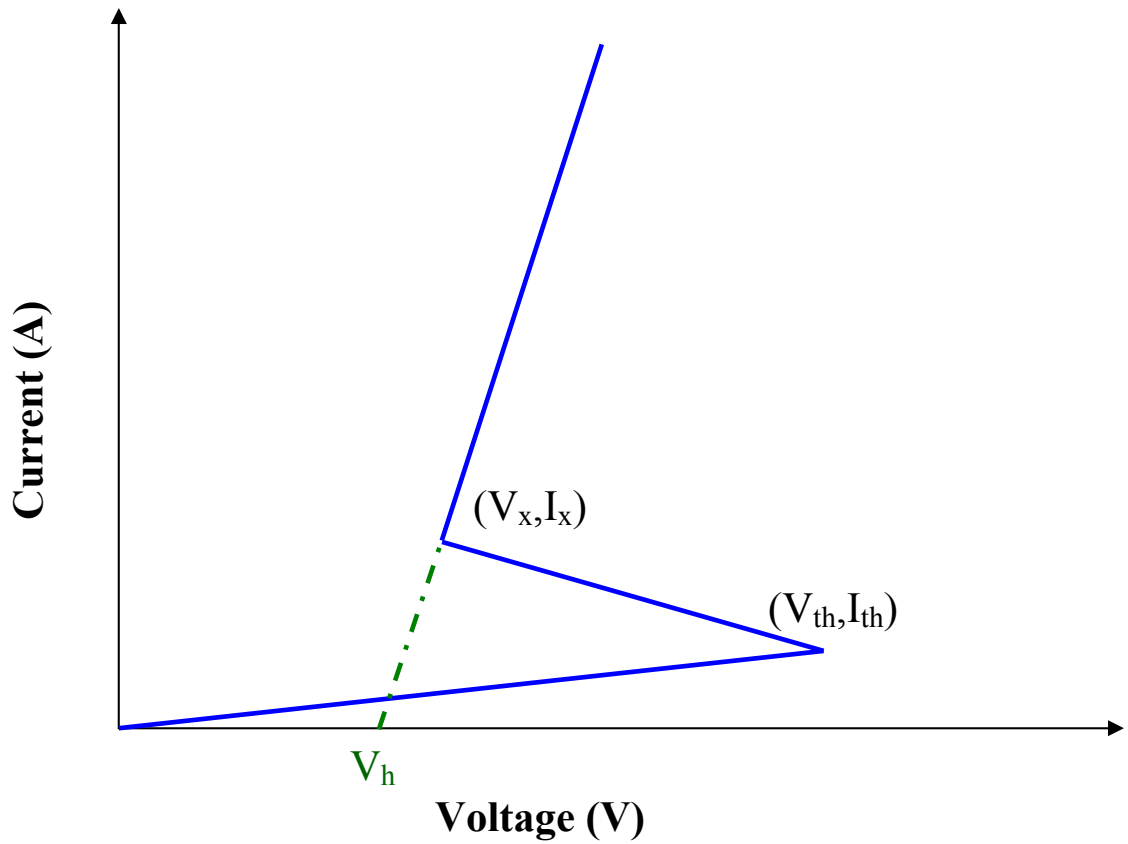
PCMR Module

- The I-V curve of the Reset state



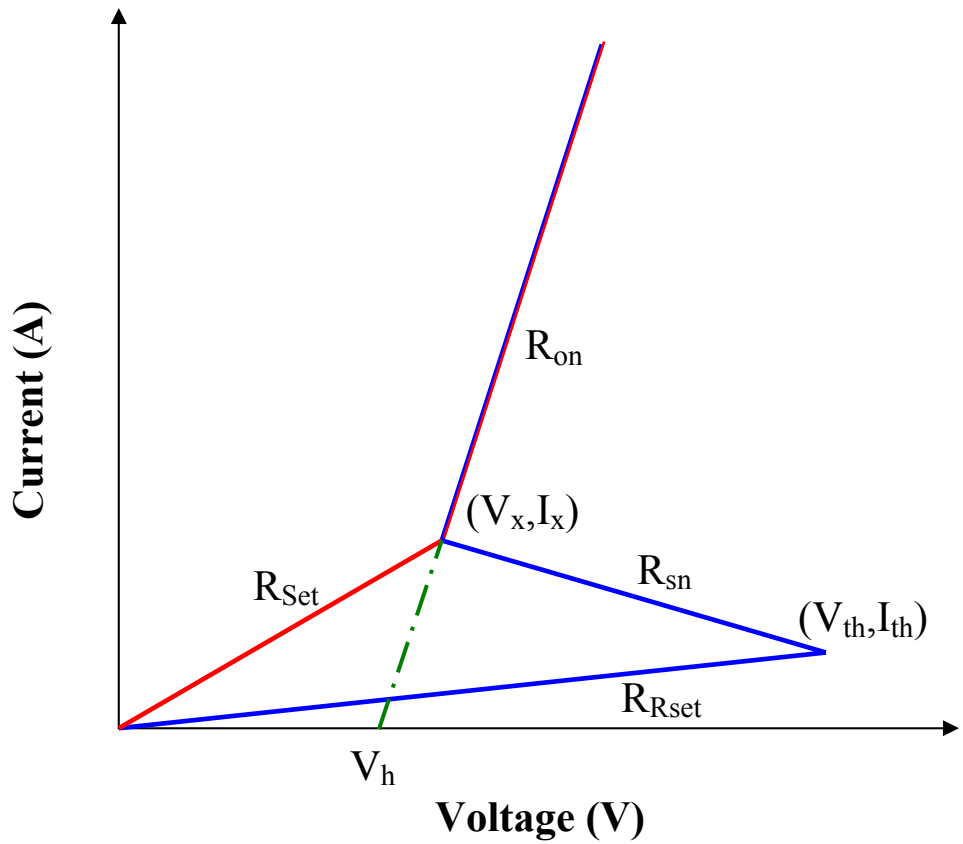
PCMR Module

- The I-V curve of the Reset state



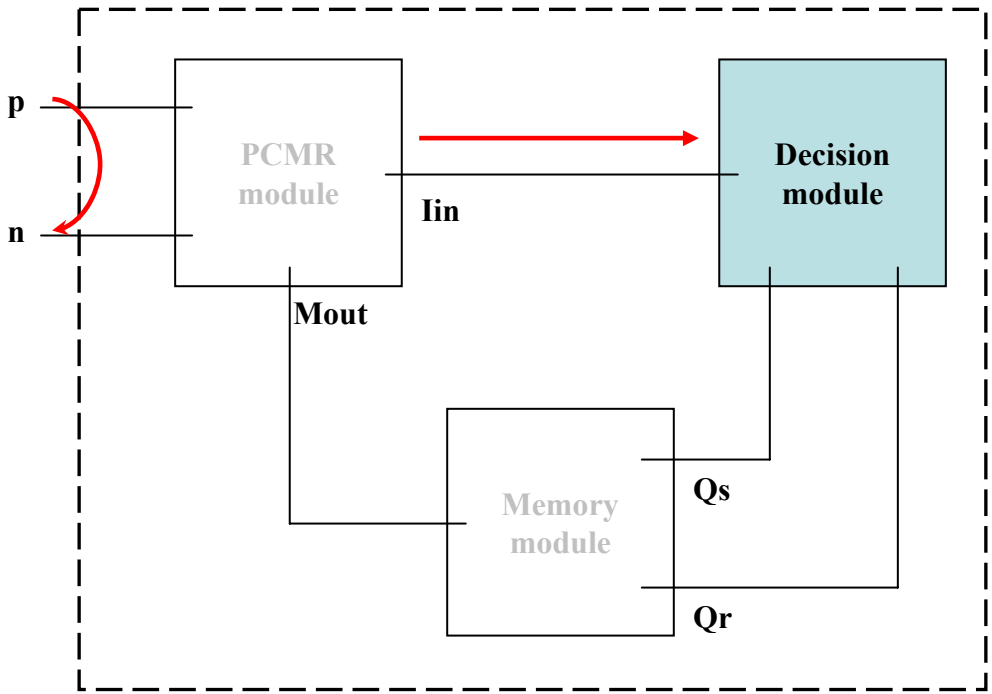
PCMR Module

- Complete I-V curves
- The Set curve or Reset curve were selected by “Memory module”



Decision Module

I (Iin,gnd) <+ I (p,n);

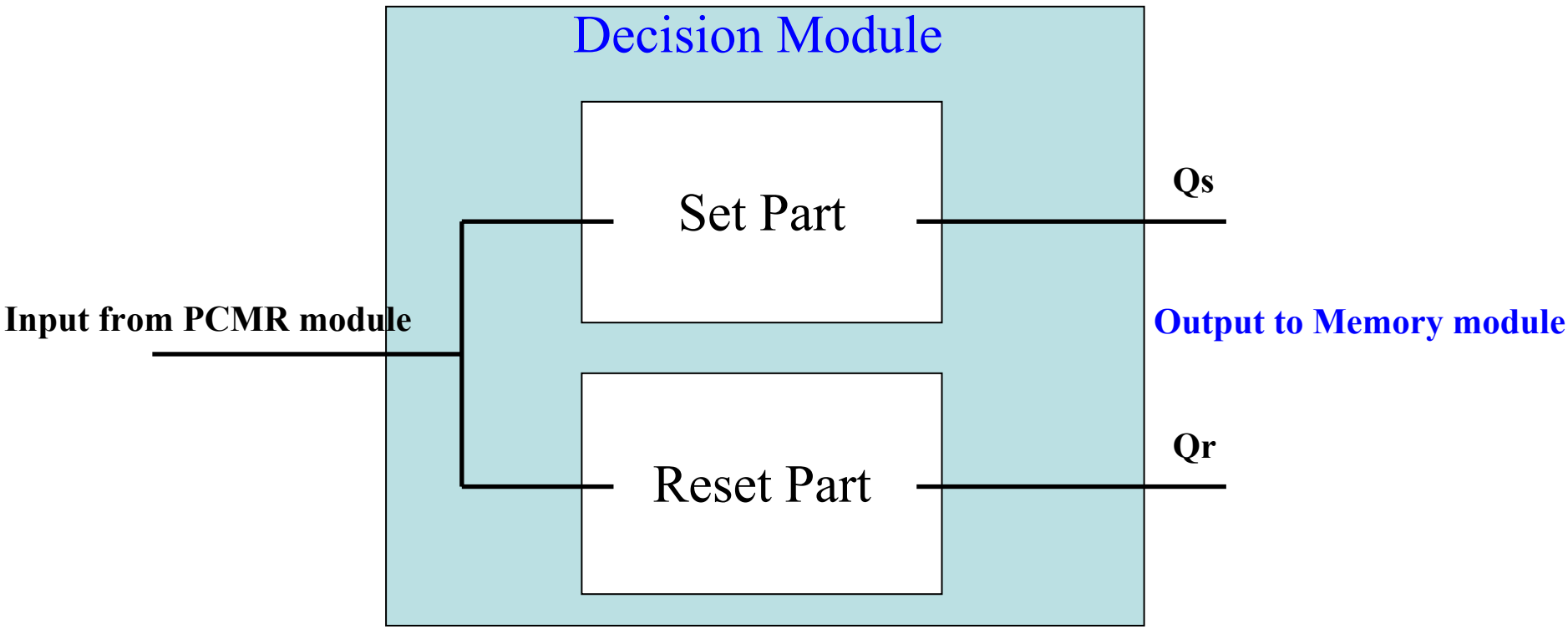


Decision Module

- To determine the current pulse amplitude and width
- Using CCR (Current Control Resistance) to determine the pulse amplitude
- Using RC circuit to determine the pulse width

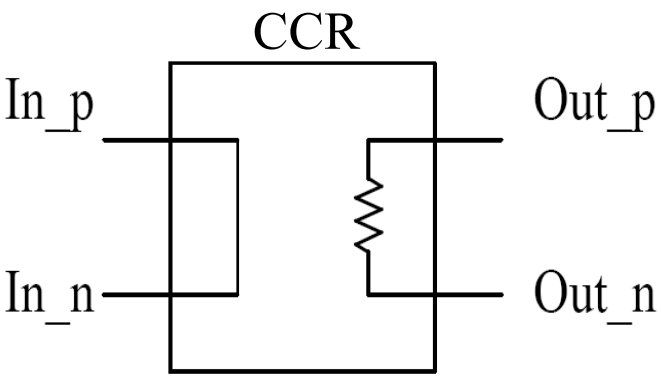
Decision Module

- The Set and Reset programming conditions are determined respectively

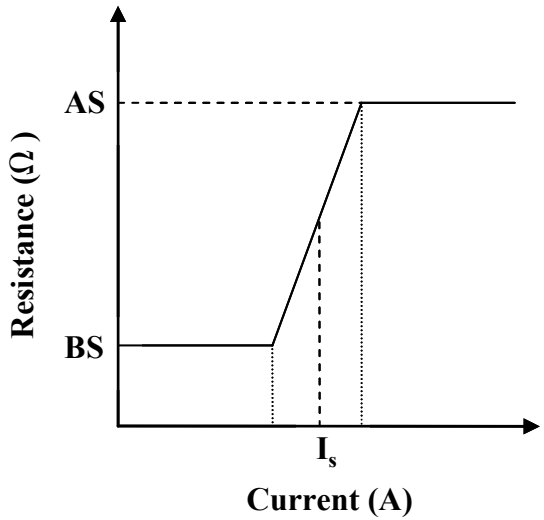


Current Control Resistance (CCR)

- Fermi equation: Smoothing function



$$R(I) = BS + \frac{AS - BS}{1 + exp[(I_s - I) \times F]}$$

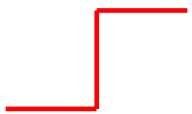


RC Circuit Implement by CCR

- RC circuit, implemented with CCR

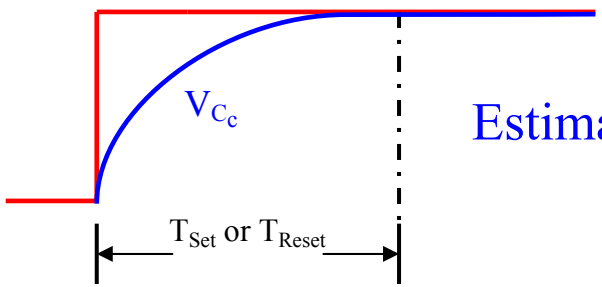
$$t = R_{rc} C_c \, ln\left[\frac{V_{rc}}{V_{rc} - V_{C_c}(t)}\right].$$

Case I. Iin<Is (I_{Set} or I_{Reset})

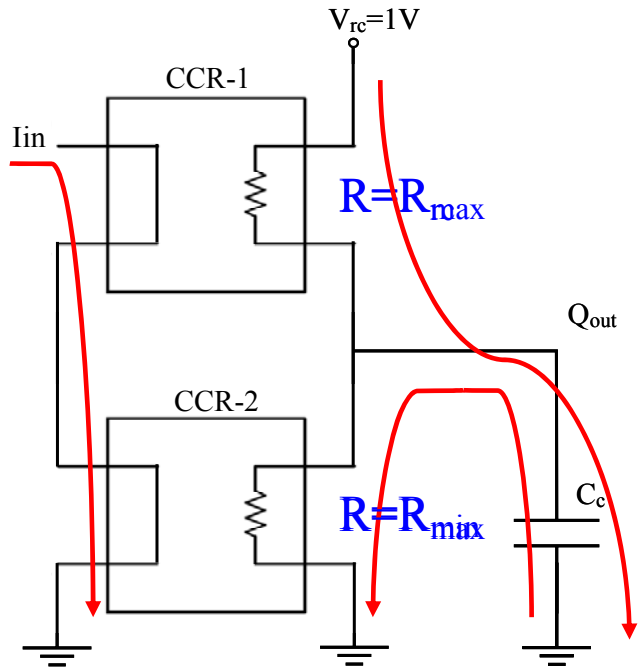


Do not estimate the time

Case II. Iin>Is (I_{Set} or I_{Reset})



Estimate the time



Memory Module

- Using VCR and capacitor to record the state

- Qr = High voltage

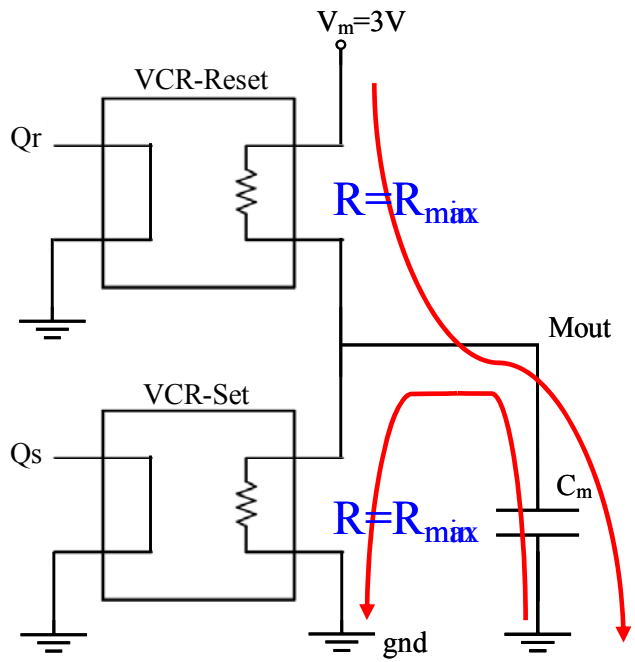
Programmed to Reset state

Mout =3V (High stage)

- Qs = High voltage

Programmed to Set state

Mout =0V (Low stage)



Modeling

- The model block chart

- Qr=High stage

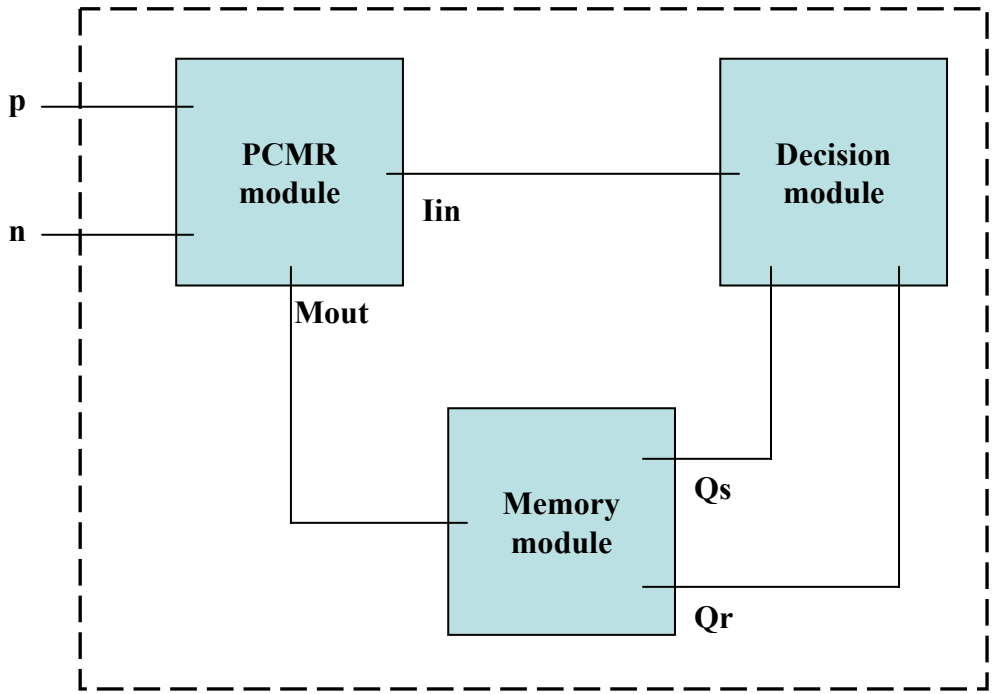
→Mout=High stage

→Reset curve will be selected

- Qs=High stage

→Mout=Low stage

→Set curve will be selected

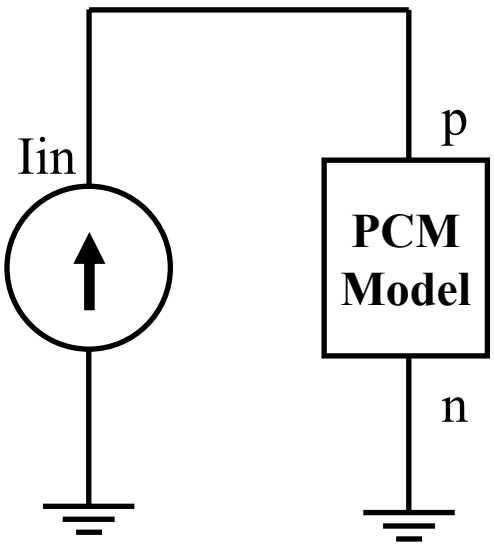


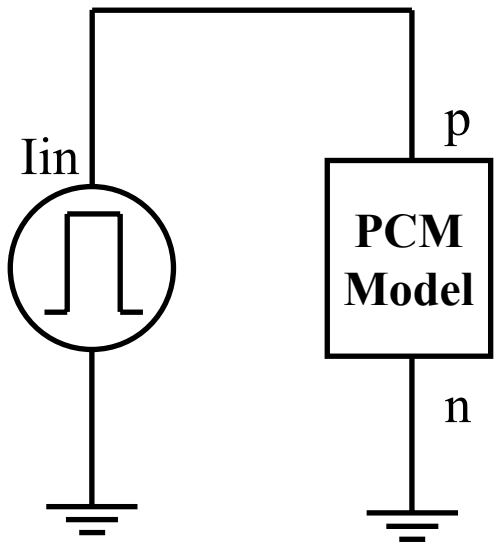
Simulation Results

- Verilog-A model evaluation using HSPICE

- DC sweep analysis

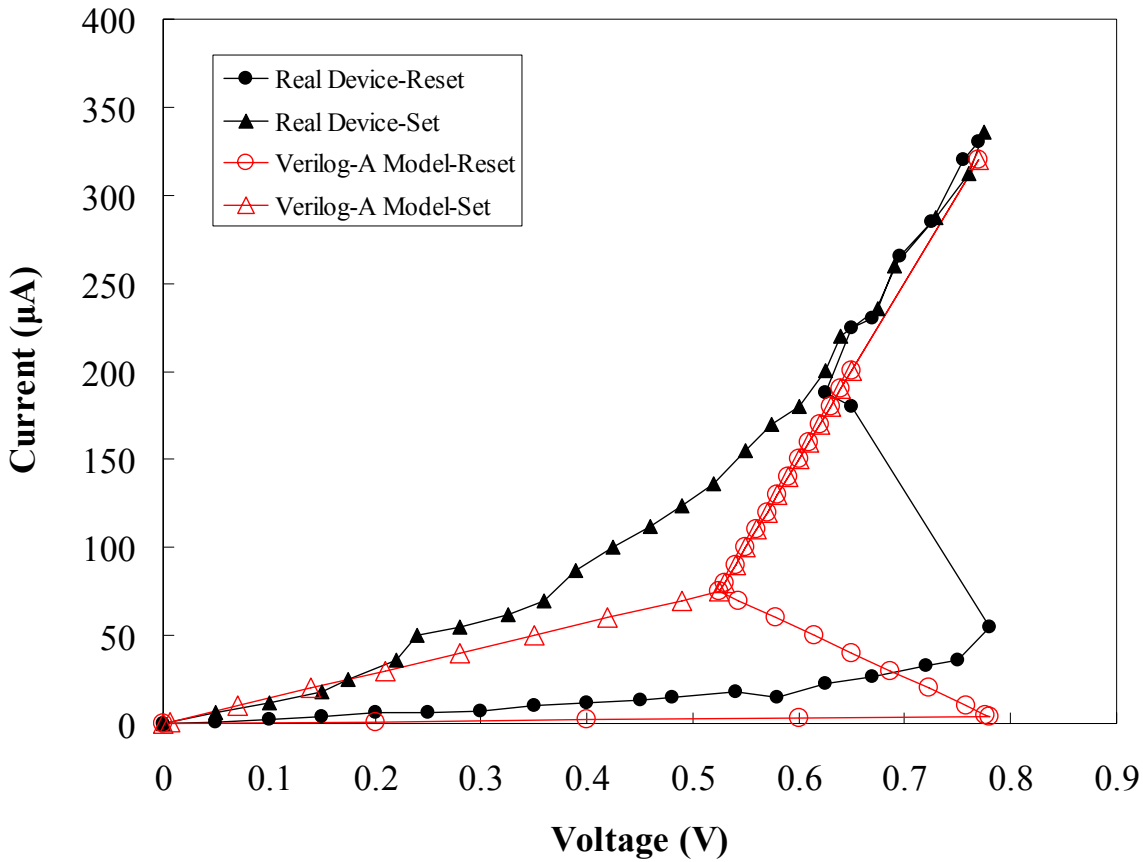
- Transient analysis





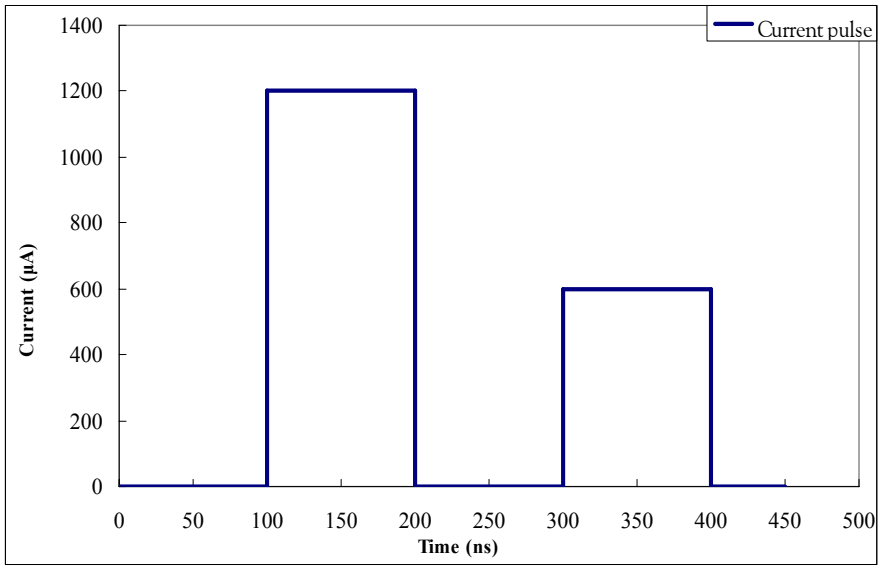
Simulation Results

- DC sweep analysis (I-V curves)

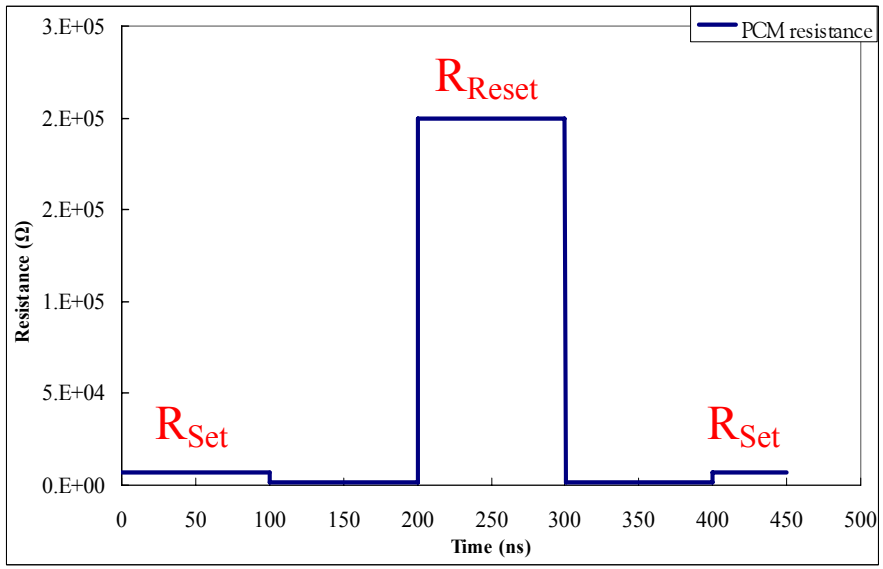


Simulation Results

- Transient analysis
- Input the current pulse to change the PCM resistance



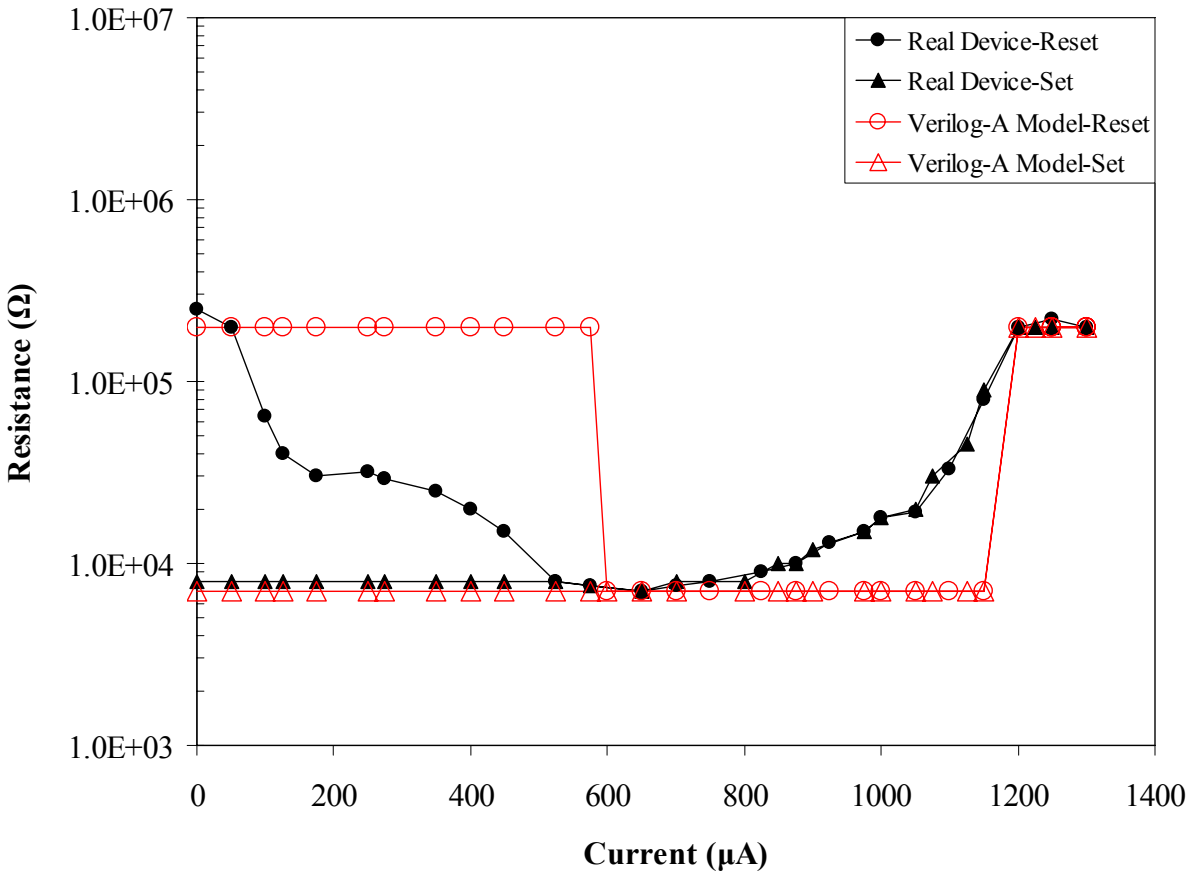
Input current pulse



PCM resistance

Simulation Results

- R-I curves



Conclusions

- We have presented a compact PCM model using Verilog-A.
- The model is predictive, yet simple to use.
- The model can be implemented in any circuit simulators with the Verilog-A option.
- PCM modeling with Verilog-A is flexible and has good convergence based on our simulation.

Thanks For Your Attendance