Flash Memory Cell Compact Modeling Using PSP Model

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ABSTRACT

In this work, a new compact Flash memory cell model is developed using Verilog-A. The PSP MOS description is used as a basis for the formulation of the conduction channel behavior. The floating gate potential is implicitly computed with an added charge neutrality relation that ensures a good convergence in DC analysis. In order to perform transient simulations, as programming or erasing operations, injection current equations have been implemented. In this presentation, the model is run in ELDO simulator and is characterized with ICCAP software. It has been validated on an advanced STMicroelectronics' technology. The final objective of this work is to provide an accurate and scalable design tool.

1. INTRODUCTION

Nowadays, an essential part of the Non-Volatile Memory market is linked to Flash memory cells [1]. In order to present an answer to design needs, realistic Flash cell models have to be implemented, considering the numerous physical effects which can impact the component performances. From a designer point of view, it can be quite convenient to include an accurate cell model in circuit simulations. For that reason, the first concern is to use a compact modeling approach [2] to integrate common circuit simulators. This choice allows multi-cell simulations and facilitates design analysis.

In the presented work, a well known compact MOS formulation, the PSP model [3], is chosen to describe the conduction channel of the Flash Memory cell. As it is written with Verilog-A language, the PSP code is flexible and can be easily modified. In order to obtain a Flash cell structure, this model is coupled with a charge neutrality equation, which implicitly computes the floating gate potential [4]. From this relation, Flash cell behavior can be simulated in DC analysis, while the resulting threshold voltage of the cell depends on the amount of charge inside the floating gate. Hot carriers [5] and Fowler-Nordheim [6] injection current equations have been added, enabling the model to perform transient simulations, as programming or erasing operations.

Some recalls about Flash memory cells can be found in section 2. The structure of the proposed model is detailed in section 3. Then, section 4 presents a characterization procedure to extract experimental fitting parameters. Simulation results are presented in section 5. Finally, section 6 gives some perspective and concluding comments.

2. BACKGROUND

The structure of the Flash memory cell (Fig.1) includes the usual MOS transistor electrodes: source, drain, bulk, and control gate. The floating gate is an additional poly-silicon layer in the oxide, between the control gate and the bulk. During a programming or an erasing operation, the use of high voltages enables electrons to pass through the thin oxide between the bulk and the floating gate.

Channel Hot Electrons (CHE) effect is caused by the combination of strong vertical and horizontal electric fields in the structure. This involves the presence of electrons with high velocity in the conduction channel, and a negative charge injection from the drain side of the channel to the floating gate. The Fowler-

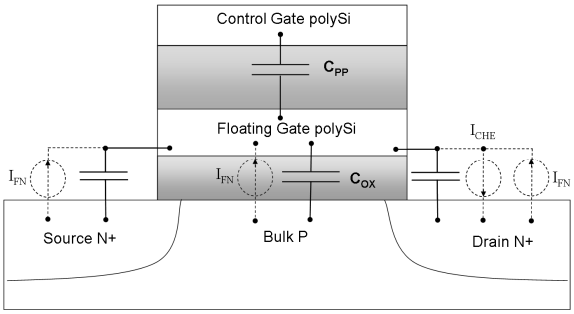

Figure 1: Capacitive structure and main injection currents of the Flash memory cell.

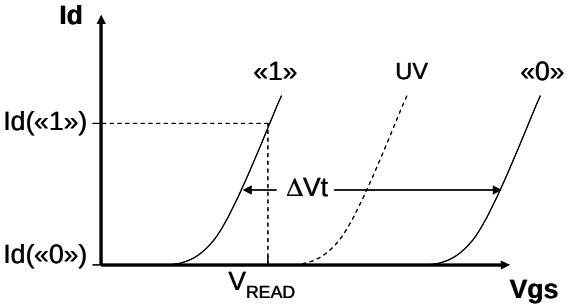

Figure 2: I-V curves of the Flash cell in erased, programmed and UV mode.

Nordheim injection (FN) results from a high vertical electric field that enables the negative charge evacuation.

During a reading operation, the drain current resulting from a standard polarization depends on the amount of charge in the floating gate. If the charge of the floating gate is strongly negative, the Flash cell is programmed (0), and there is no drain current. Otherwise the cell is erased (1), and the same polarization leads to drain current (Fig.2).

The floating gate effect modifies the threshold voltage V_T of the cell, following the relation [1]:

$$V_T = V_{Tuv} - \frac{Q_{FG}}{C_{PP}} \quad (1)$$

where V_{Tuv} is the threshold voltage after UV erasing, Q_{FG} is the charge in the floating gate, and C_{PP} is the capacitor related to the control gate and the floating gate. V_T can be arbitrarily defined as the control gate voltage that leads to a 1µA drain current.

3. PSP-BASED FLASH CELL MODEL

The PSP MOS model is a recent surface-potential-based description that includes many effects as mobility reduction, velocity saturation, impact ionization or GIDL current [3].

Moreover, this model is effective concerning drain and source overlaps, and a JUNCAP formulation [7] is used for the diodes of the structure. With its analytic works and its physical bases, the PSP model presents a good compromise to provide the conduction channel behavior with reasonable time consumption.

Considering traditional Flash cell architecture, it appears that a MOS model is adapted to describe what happens between source, drain, bulk, and floating gate electrical nodes (Fig.1). Then, the ONO capacitor, C_{PP}, is added to the initial PSP model, entailing a split between the control gate and the floating gate [8]. The amount of charge in the floating gate must be taken into account to obtain the floating gate potential. Consequently, the PSP model is coupled with the charge neutrality equation formulating the charge in the floating gate:

$$Q_{FG} = Q_{GI} + Q_{GS} + Q_{GD} + C_{PP}\left(V_{FG} - V_{CG}\right) \quad (2)$$

where V_{FG} and V_{CG} are respectively the floating gate and the control gate potentials. Q_{GI}, Q_{GS} and Q_{GD} are the charge parts of the floating gate related respectively to the intrinsic zone and to the source and drain overlap extrinsic zones. The values of Q_{GI}, Q_{GS} and Q_{GD} depend on V_{FG} and are computed using the PSP formulation. Finally, equation (2) results in an implicit computation of V_{FG}. With this formulation, the new model can provide the Flash cell behavior in DC analysis. The threshold voltage of the cell is set to programmed or erased mode by varying Q_{FG}.

In transient simulations, if high voltages are used, it is assumed that Q_{FG} is not constant by reason of the charge injection through the tunnel oxide. Then, the model is subject to an additional relation:

$$Q_{FG} = Q_{FG\,0} + \int I_{FG}\, dt \quad (3)$$

where Q_{FG0} is the initial charge in the floating gate, and I_{FG} is the sum of all injection currents through the oxide. Channel Hot Electrons and Fowler-Nordheim tunneling injections are taken into account, following the formulations described in [5] and [6]:

$$I_{CHE} = A_D . I_{AVL} . e^{\frac{-A_{D\,exp}}{E_{TUND}}} \quad (4)$$

$$I_{FN} = \alpha . S . E_{TUN}{}^2 e^{\frac{-\beta}{E_{TUN}}} \quad (5)$$

A_D, A_{DEXP}, α and β are optimized parameters, E_{TUN} is the electrical field through the oxide, called E_{TUND} at drain side, and S is the FN injection surface. The avalanche current I_{AVL} is provided by the PSP model in the case of a saturated channel.

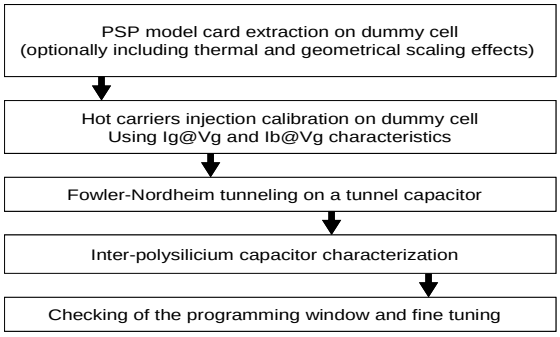

Figure 3: Characterization procedure diagram.

4. CHARACTERIZATION PROCEDURE

A diagram presenting the different characterization steps can be found in figure 3. The first characterization step is dedicated to the PSP model card extraction, using a dummy cell, with contacted floating and control gates [9].

This procedure gives the possibility of including temperature and geometrical scaling rules that are described in the model. In this

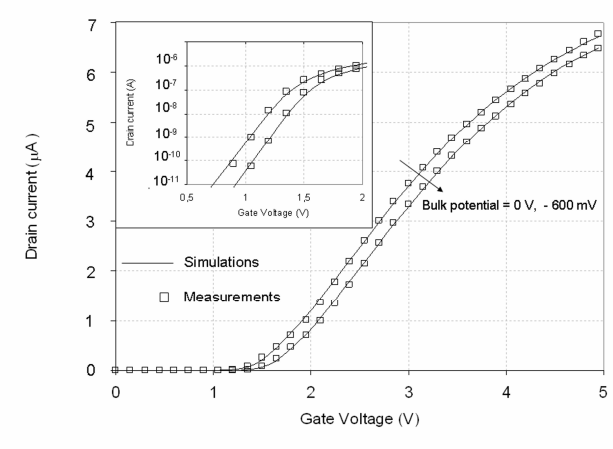

Figure 4: Id-Vg dummy cell characteristics.

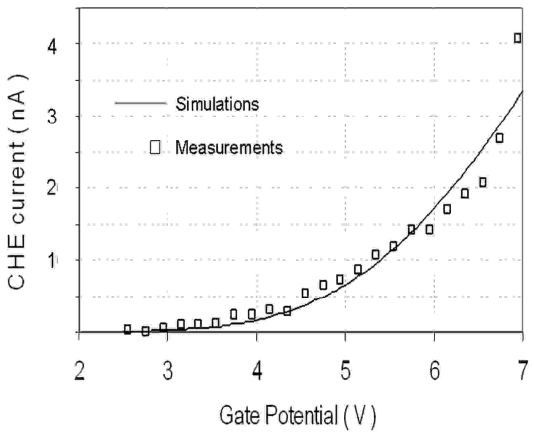

Figure 5: Ig-Vg dummy cell characteristic with high Vd.

case, the PSP model card must be extracted for many dummy cells, with various lengths and widths, at various temperatures. Then, each local model card is linked to other ones thanks to a global parameter set. Figure 4 illustrates the concordance obtained between measurements and PSP simulations on dummy cell drain current characteristics. The modification induced by the negative bulk potential shows a fine modeling of the body effect.

The next step relates to injection current calibration. Concerning hot carriers (CHE), the optimization is achieved by using gate current measurements on a dummy cell (Fig.5), with high drain and gate voltages. The avalanche current that appears in equation 4 has been previously calibrated during the first step, while it is related to the bulk current characteristics (Fig.6). The Fowler-Nordheim tunneling current is characterized on a high surface capacitor whose thickness matches the tunnel oxide thickness of the cell (Fig.7). According to the available characterization components, α and β parameters can be also extracted for overlap extrinsic zones. Direct and inverse injection case can be calibrated independently.

After an UV erasing operation, Q_{FG} is supposed to be equal to zero, simplifying the equation (1). Then, the real cell characteristic is used to extract the C_{PP} value. The last step of the

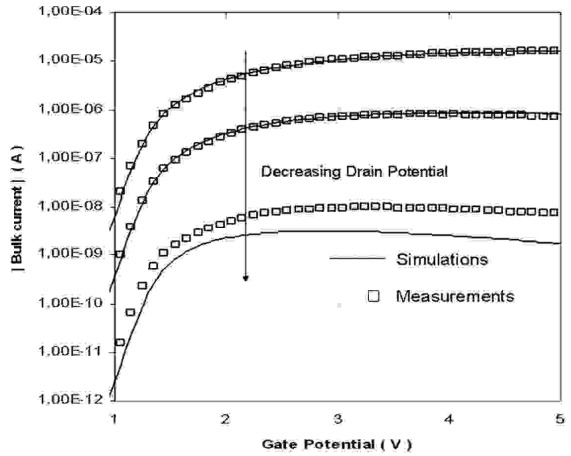

Figure 6: Ib-Vg dummy cell characteristics.

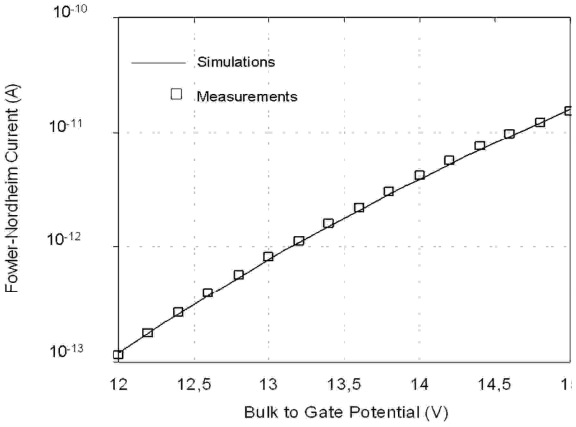

Figure 7: Fowler-Nordheim tunneling characteristic.

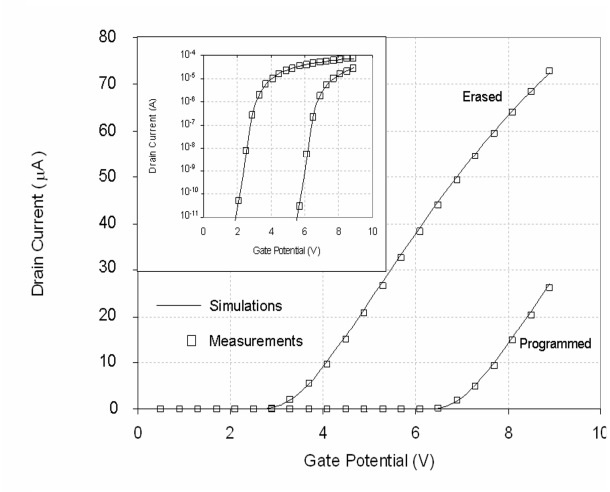

Figure 8: Drain current of the cell as function of control gate voltage in programmed and erased modes.

characterization consists in checking the whole model by comparing simulations and real cell characteristics, and by fine tuning specific parameters if necessary. The simulations of the erased and programmed modes are compared to measurements, in order to determine the initial charge Q_{FG0} related to each mode (Fig.8). Finally, the simulated and measured evolutions of V_T during a CHE programming operation are compared (Fig.9). The error observed at the end of operation is lower than 500mV.

5. SIMULATIONS

In consequence of the additional floating gate node, the convergence of the Flash cell model is slower than the convergence of the single PSP model. Approximately, observations show that the duration increases by 5% in a DC simulation with constant Q_{FG}, and by 70% in a transient simulation with varying Q_{FG}.

The final model is suitable to estimate values that are unreachable with direct measurements, as the floating gate potential V_{FG} or the injection currents. It facilitates the analysis of fast operations, as

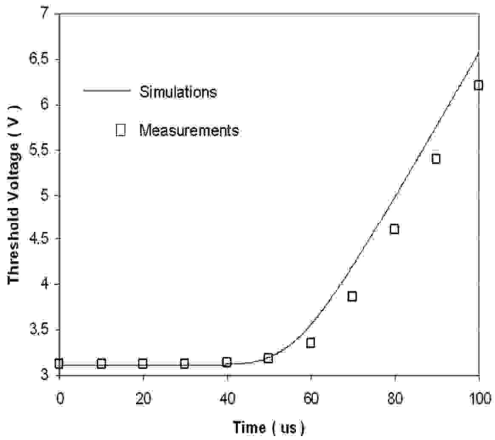

Figure 9: V_T evolution during a 100µs programming operation.

short programming phases. Moreover, the model enables the evaluation of the instant electrode currents, providing a good qualitative approach to consumption problems.

The curves of figure 10 present the evolution of several variables of the model during a 5µs programming operation. The first simulation is performed with a ramped V_{CG}, which leads to increasing V_{FG} and I_{CHE}. The second simulation is performed with a constant V_{CG}, which carries decreasing V_{FG} and I_{CHE}. Those results concord with theory [10].

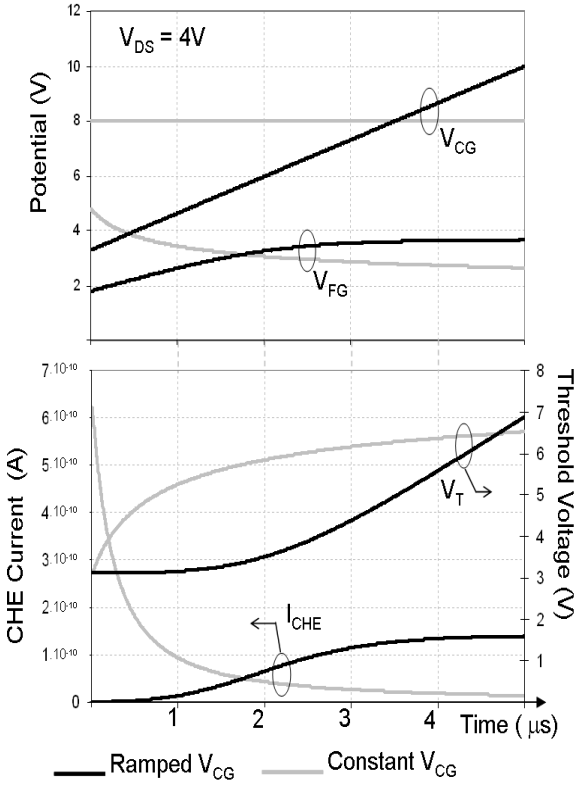

Figure 10: Simulations of the CHE programming operation by applying a ramped and a constant V_{CG}.

6. SUMMARY

A PSP-based Flash memory cell description is proposed. This compact approach is needed to include an accurate electrical behavior of Flash cells in memory design simulations. From the PSP initial code, the floating gate is formulated thanks to a charge neutrality relation. By adding the injection current equations, users can perform both the DC and the transient analysis. The model has been implemented in ELDO simulator and characterized using ICCAP. It has been validated on an advanced STMicroelectronics' technology and aims to perform multi-cell simulations, analysis about consumption or injection rates. The flexible nature of the code makes it possible to introduce other effects. It can be adapted for various researches, as reliability or temperature concerns.

7. REFERENCES

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APPENDIX: Verilog-A code added to PSP

Listing 1. Additional declarations.

```
// additional section in nodes declaration
output FG;  // floating gate node
```

```
output Igate;   // extra node to observe floating gate injection currents
output VT;      // extra node to observe threshold voltage value
electrical FG, Igate, VT;

// additional section in local parameters declaration
parameter real  Cpp=0;
parameter real  Qfg0=0;
parameter real  VTuv=0;
parameter real  Alpha_wr=0;
parameter real  Beta_wr=0;
parameter real  Alpha_er=0;
parameter real  Beta_er=0;
parameter real  Alpha_wr_d=0;
parameter real  Beta_wr_d=0;
parameter real  Alpha_er_d=0;
parameter real  Beta_er_d=0;
parameter real  Alpha_wr_s=0;
parameter real  Beta_wr_s=0;
parameter real  Alpha_er_s=0;
parameter real  Beta_er_s=0;
parameter real  AD1=0;
parameter real  ADexp =0;
parameter real  W1 =0;
parameter real  L1 =0;

// additional section in variables declaration
real   Ifn, Ifns, Ifnd, Ifnb, Etuns, Etund, Etunb, Etundx;
real   Iche, Ifg, INTE, Vcg, S1;
```

Listing 2. Additional equations.

```
// additional equations section in analog block
begin : VFGequation
    Ifg = ( Ifn – Iche ) ;
    INTE= idt( Ifg ) ;
    V( Igate ) <+ Ifg ;
    V( FG ) <+ ( INTE + Qfg0 – Qgd_ov – Qgs_ov – Qg ) / Cpp + Vcg ;
    V ( VT ) <+ VTuv – ( INTE + Qfg0 ) / Cpp ;
end

// additional equations in analog-evaluateStatic block
     // in “Initialization of some variable” part:
    //  Vgs = V( `Gint, S ) ;   // this line must be removed
    Vgs = V( FG, S ) ;
    Vcg = V( `Gint ) ;

    S1 = W1 * L1 – 2 * SOV ; // Floating gate to bulk surface

// in “Gate current” part (SWIGATE parameter must be set to 0):

          // electric field definitions:
Etuns = Vovs / TOX ;
Etund = Vovd / TOX ;
Etundx = ( Vgs - Vbs - VFB - ( phit*x_d ) ) / TOX ;
Etunb = ( Vgs - Vbs - VFB - ( phit * ( x_s + x_d ) / 2 ) ) / TOX ;

          // Fowler-Nordheim currents:
if ( Etund == 0 ) begin
  Ifnd = 0 ;
end else if ( Etund < 0 ) begin
 Ifnd = Alpha_er_d * SOV * Etund * Etund * exp( Beta_er_d / Etund ) ;
end else begin
 Ifnd = -Alpha_wr_d * SOV * Etund * Etund * exp( -Beta_wr_d / Etund ) ;
end
if ( Etuns == 0 ) begin
 Ifns = 0 ;
end else if ( Etuns < 0 ) begin
 Ifns = Alpha_er_s * SOV * Etuns * Etuns * exp( Beta_er_s / Etuns ) ;
end else begin
 Ifns = -Alpha_wr_s * SOV * Etuns * Etuns * exp( -Beta_wr_s / Etuns ) ;
end
if ( Etunb == 0 ) begin
 Ifnb = 0 ;
end else if ( Etunb < 0 ) begin
 Ifnb = Alpha_er_b * S1 * Etunb * Etunb * exp( Beta_er_b / Etunb ) ;
end else begin
 Ifnb = -Alpha_wr_b * S1 * Etunb * Etunb * exp( -Beta_wr_b / Etunb ) ;
end

Ifn = Ifns + Ifnd + Ifnb ;

          // Channel Hot Electron current:
  if ( Etundx > 0 ) begin
    Iche = AD1 * Iimpact * exp( -ADexp / Etundx ) ;
  end else begin
    Iche = 0 ;
  end
```