Occurrence and Simulation of Index-3 DAEs in VLSI Circuits

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***Abstract*—In this paper we present a circuit configuration that generates an Index-3 DAE. Previous index analyses of analog circuits have proved that the DAE set modeling the circuit is at most Index-2. We show that certain behavioral models for transistors can generate an Index-3 DAE when a particular structural condition is satisfied. Most BDF methods are unstable for Index-3 DAEs, the DAE set has to be preconditioned via constraint differentiation or regularization to reduce the Index of the DAE. We present an efficient regularization procedure that can be applied to the Index-3 DAE generated by the transistor model. The occurrence condition and the regularization procedure can be checked for and performed at the netlist level. We show with examples how the modification improves the simulation process in terms of accuracy of the solution and improved convergence properties.**

I. Introduction

An automatic extraction method such as Modified Nodal Analysis(MNA) generates a set of Differential-Algebraic Equations(DAE) from the circuit netlist. The DAE set is evaluated with Backward Difference Formula(BDF) methods, which predict the evolution of the system variables with the passage of time. The performance of the BDF methods is dependent on the $index$ of the DAE. BDF methods are known to be stable when presented with Index-1 DAEs [1]. Index-2 DAEs that occur in analog circuit models are known to contain beneficial structures for BDF methods [2]. Index-3 DAEs however are known to cause instabilities to the variable step size BDF methods [3]. If the index of the DAE set is available before the simulation process, a preconditioning procedure based on the DAE structure can improve the efficiency of the BDF method.

Reissig [4] first showed that the equation set modeling circuits containing only passive RLC components and transformers and gyrators is at most an Index-2 DAE. Encinas and Riaza removed the passivity condition from [4] to show that a more general class of analog circuits generates Index-1 or Index-2 DAEs [5]. Schwarz and Tischendorf present a structural condition for the occurrence of Index-2 DAEs in circuit configurations [2]. Soto and Tischendorf analyze the Partial-DAE(PDAE) system arising as a consequence of modeling the drift-diffusion equations in carrier transport [6]. They show that the PDAE discretized on a mesh generates an Index-1 or Index-2 DAE.

In this paper, we present the first case of an Index-3 DAE generated by a practical circuit configuration. Index analysis methods are directly dependent on the set of components included in the analysis procedure. While structural models are restricted to the results presented in the literature, behavioral models need not adhere to the same constraints. We show that a common transistor modeling technique, charge based current modeling, can generate an Index-3 DAE when certain connection configurations are satisfied by the circuit. The connection configuration is presented as a structural condition to enable its detection at the netlist level.

To reliably simulate Index-3 DAEs with BDF methods, an appropriate preconditioning procedure is necessary. These procedures aim to reduce the index of the DAE by differentiating part of the equation set or by regularization techniques [7]. Constraint differentiation involves choosing a subset of the DAE set and computing its Jacobian. The new DAE set will have a reduced index if the proper subset is chosen [5], [7], [8]. Computation of the Jacobian is an expensive procedure in circuit simulation, an alternate method without this procedure would be a favorable choice for index reduction. Regularization methods improve the solvability of Index-3 DAEs by adding stabilization terms to reduce the index [7], [9]. The modified DAE is under the constraint that the perturbed solution should be as close as possible to the original solution set. A procedure for regularization of VHDL-AMS models is presented in [10]. Regularization methods are usually linked to the particular structure of the DAE which it targets, and are not applicable to a general class of Index-3 DAEs. In this context, we present an efficient regularization procedure for the Index-3 DAE that is generated by the above mentioned circuit configuration. We show with examples how the regularization process improves the quality of the solution when compared to the original Index-3 DAE.

The rest of the paper is organized as follows: in section II we present some background on the index of a DAE and its computation. In section III we present a transistor model and the connection configuration that generates the Index-3 DAE. In the next section, we present a regularization method for this Index-3 DAE. Finally, we present results comparing the simulation of the regularized DAE with the original Index-3 version.

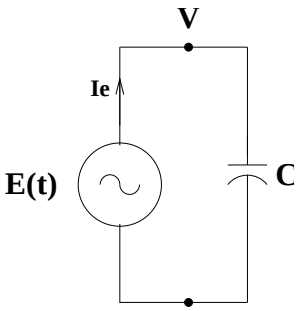

Fig. 1. Index-2 DAE Circuit

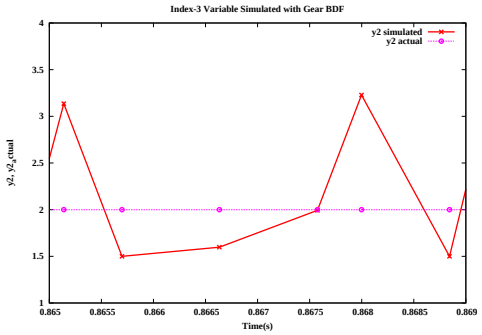

Fig. 2. Simulated vs. Analytical Index-3 Variable

II. DAE INDEX

The fully implicit nonlinear DAE can be written as

$$F(t, y, y') = 0 \tag{1}$$

The index of (1) is defined as the number of times that all or part of the DAE set have to be differentiated to represent it as an Ordinary Differential Equation(ODE) [1]. Gear presents an analytic procedure to compute this index in [11]. From (1), a subset $y'_1 = e_1$ of y' is solved for and the remaining equations are grouped as a subset g_1 of F. The first differentiation of g_1 allows to solve for y'_2, where y_2 is a subset of $y \backslash y_1$. The remaining equations, $F \backslash (g'_1 \cup e_1)$, are grouped as g_2. The procedure continues until y' is completely solved for. The number of differentiations that were performed is the index of the DAE F. We use this procedure to find the index of the circuit shown above. MNA generates the following equations:

$$\begin{aligned} -I_e + CV' &= 0 \\ V - E(t) &= 0 \end{aligned}$$

The first equation can be used to solve for V': $V' = I_e/C$. The second equation is differentiated to give $V' - E'(t) = 0$ and the value for V' is substituted to give $I_e/C - E'(t) = 0$. Since I'_e cannot be solved for from this equation, a second differentiation is necessary, finally giving $I'_e = CE''(t)$.

An Index-3 DAE discussed in [1] is as follows:

$$\begin{aligned} x'_1 &= x_2 \\ x'_2 &= x_3 \\ 0 &= x_1 - g_1(t) \end{aligned}$$

The analytical solution to this DAE is given by $x_1(t) = g(t)$, $x_2(t) = g'(t)$, $x_3(t) = g''(t)$. Fig. 2 compares the simulated value of the Index-3 variable with its analytical value. Cadence IUS58 was used for performing the simulation with the Gear2 BDF option. The simulated value deviates considerably from the analytical value. If this variable is part of a larger equation set, then the error could propagate to other variables in the system. In the next section, we present a component model and a connection configuration that suffers from a similar problem.

III. INDEX-3 DAE GENERATORS

Charge based current modeling is a common method of modeling transistor behavior. The channel currents and parasitics are characterized in terms of the charge present in the terminals of the transistor [12], [13]. The equation that models the current can be written as

$$I = \frac{dQ}{dt} = \frac{d}{dt}(\overline{V}) \tag{2}$$

$$I_j = \frac{dQ_j}{dt} = \sum_i \frac{\partial Q_j}{\partial V_{iS}} \frac{dV_{iS}}{dt}, \; i = G_f, G_b, D, B \tag{3}$$

$\overline{V}$ is the vector of system voltages in the DAE set. (2) can be directly included in a behavioral model of a component; (3) has to be modified to eliminate the partial derivative before it becomes part of an element stamp for MNA. We use the discretization methods discussed for SPICE or VHDL-AMS [14]. The final form of (3) can be written as

$$I_{V'} = \left[\frac{f(\overline{V})}{g(\overline{V})}\right] \frac{d\overline{V}}{dt} \tag{4}$$

We call these voltage controlled current sources as $I_{V'}$ sources. From the above discussion two important properties can be deduced: (1) The characteristic equation of the controlled current source is a function of the *derivative* of the terminal voltages and (2) this special form occurs if a charge based modeling method is used with the charges being expressed in terms of terminal voltages. In the rest of this section, we show how **the occurrence of an L-$I_{V'}$ *cutset* in the circuit is capable of generating an Index-3 DAE.**

Consider the simplest case of the cutset in Fig. 3, where the L and $I_{V'}$ components are incident at node j. The components modeling the transistor are enclosed within the oblong boundary. The dashed extensions to the branches represent connections to other parts of the circuit. The area of interest is the intersection of the $I_{V'}$ source component with an inductor L, external to the transistor model. For this configuration, MNA generates the following equations:

$$-i_1 - i_2 - i_3 + I_L = 0 \tag{5}$$

$$V_i - V_j = LI'_L \tag{6}$$

$$-I_L + I_{V'} = 0 \tag{7}$$

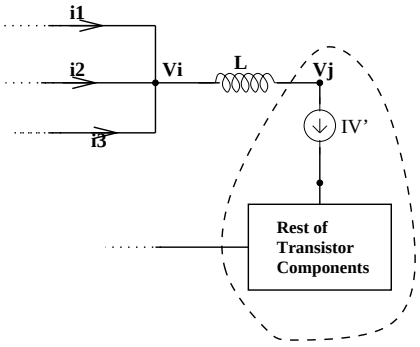

Fig. 3. Index-3 DAE Generator

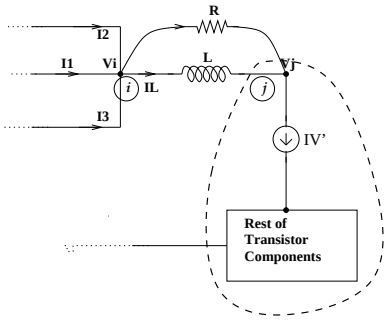

Fig. 4. Regularized L-$I_{V'}$ cutset

While applying Gear's procedure to determine the index of a larger circuit containing this configuration, (6) becomes part of y_1' because it can be used to solve for I_L'. There is no other occurrence of V_j in the DAE F and we see the following: $V_j \notin g_1$ and we also have $V_j' \notin e_1$. From the former relation, we can deduce:

$$(V_j \notin g_1) \implies (V_j' \notin g_{1,v_1} v_1') \tag{8}$$

From the above relations and g_1 from (3.2c) in [11], V_j' cannot be solved for from g_1' making necessary a second differentiation of some of the equations in F.

$$g_1' = y_2' \cup g_2(y_1, y_2, v_2, t) \tag{9}$$

The only occurrence of V_j is in (6) and this form is preserved in g_2. In g_2', some equation g_{2i}' will be of the form

$$\frac{V_i' - V_j'}{L} = g_{2i}'(y_1, y_2, v_1, v_2', t) \tag{10}$$

From this single equation, both V_j' and V_i' cannot be solved for simultaneously, necessitating a third differentiation to solve for V_j'- **from the definition of the DAE index, this implies the DAE F is Index-3.**

Some situations where both V_j' and V_i' are coupled in the form of (10) are enumerated below:

1) V_j' occurs only with V_i' making it possible to solve for one of them, but not both
2) The term V_j' disappears due to it numerical inverse occurring in (10)
3) The term containing V_j' becomes part of y_2 and does not appear in g_2(and hence neither in g_2')

The generator node however is the node j in Fig. 3 and a similar analysis applies to an L-$I_{V'}$ cutset generating an Index-3 DAE. This condition can be checked for from the netlist during the elaboration stage of a circuit simulator. In the next section we discuss a procedure to eliminate this cutset and reduce the index of the resultant DAE.

IV. Regularization of DAEs generated by L-$I_{V'}$ cutsets

Index reduction methods for DAEs are divided into two broad categories: constraint differentiation and regularization. Constraint differentiation involves differentiating the constraint set repeatedly until a suitable reduction in the DAE index has been achieved. Regularization methods perform the same task by adding terms to the DAE to improve stability and convergence properties. The solution space of the modified equation set has to be as close as possible to the original DAE set, and this condition determines the positioning and the values of the terms that are added. In this section we present an efficient regularization method that can reduce the Index-3 DAE generated by the L-$I_{V'}$ cutset to one of lower index. The two conditions for the regularizing term are discussed in the rest of this section.

A. Position of the regularizing term

The regularizing term is added to the original DAE set such that the L-$I_{V'}$ components do not form cutsets in the circuit configuration. Fig. 4 shows one such configuration that can eliminate the cutset. The advantage of adding a resistor is that it adds no additional variables to the MNA generated equations. Consider the following equations that MNA generates for nodes i and j:

$$\begin{aligned} -I_1 - I_3 - I_2 + I_L + \frac{V_i - V_j}{R} &= 0 \\ V_i - V_j &= LI_L' \\ -\frac{V_i - V_j}{R} - I_L + I_V' &= 0 \end{aligned} \tag{11}$$

The conditions enumerated in the previous section for the absence of V_j in g_1 are no longer true, and a similar analysis will show that the DAE is no longer Index-3.

B. Value of the regularizing term

We derive a value for the resistor that can be added such that the BDF method generates a solution vector whose value agrees well with that of the original DAE. Ideally an extremely high value for the resistor will limit the current in its branch, but from practical observations, this high value causes a blowup of other values in the system matrix. We present a bound for this resistor that is computed from the absolute tolerance(ATOL) of the current I_L, which in turn is obtained from the model file. The bound is such that it guarantees to keep the current through the resistor branch lesser than ATOL(I_L). By the definition of ATOL, it is the accuracy to which the quantity has to be computed. Hence if the current I_L

reduces by lesser than ATOL(I_L), the effect of the reduction can be ignored during the simulation cycle. This condition is satisfied locally, i.e., at each node where the component is added. Therefore multiple occurrences of L-$I_{V'}$ cutsets can be treated by choosing the the corresponding values from the node under consideration.

Consider node i in Fig. 4. If the condition

$$I_L \gg \frac{V_i - V_j}{R} \tag{12}$$

is satisfied, the resistor current is not significant. (11) contains the characteristic equation of the inductor, generated by MNA. Using this in (12) we get a new relation:

$$I_L \gg \frac{LI'_L}{R} \tag{13}$$

To produce a specific bound from (13), we introduce the quantity ATOL(I_L) into the equation. We limit the ratio of the resistor branch current with respect to I_L to ATOL(I_L).

$$\frac{I_L}{\frac{LI'_L}{R}} \geq \frac{1}{ATOL(I_L)} \tag{14}$$

Using a backward euler approximation for I'_L in (14) we get the following relation:

$$\frac{Rh_{MIN}}{L}\left(\frac{I_L^{(m+1)}}{I_L^{(m+1)} - I_L^{(m)}}\right) \geq \frac{1}{ATOL(I_L)} \tag{15}$$

h_{MIN} is the minimum value of the time step and is determined by the simulator. We propose the relation (17) which is dependent on the definition of ATOL. Using (17), we come up with a final bound for R:

$$\mathbf{R} \geq \frac{\mathbf{L} \cdot \mathbf{ATOL}(\mathbf{I_L})}{\mathbf{h_{MIN}}} \tag{16}$$

This numerical value of R guarantees that its addition does not affect the current in the other branches to an extent that the simulator notices a change, while improving convergence properties by reducing the index. All the quantities involved in this bound are available before the simulation process, hence a component of this value can be added prior to the simulation cycle. By the above arguments, this value of the resistance is the lowest possible value such that the BDF method produces the same result in its absence. The added advantage is that the additional occurrences of the variable V_j acts as a stabilizing term to improve the convergence properties of the BDF method. In the next section, we present some examples that reinforce this claim.

V. Experimental Results

Cadence IUS58(with the Gear BDF option) and DASPK were used for performing the simulations. Matlab restricts itself to Index-1 DAEs and hence could not be used; Mathematica employs a kernel derived from DASPK and the results are equivalent. The circuit configurations tested involved linear relations to model $I_{V'}$. Other standard components were included in the netlist, an L-$I_{V'}$ cutset was included as part of the test circuits to generate an Index-3 DAE.

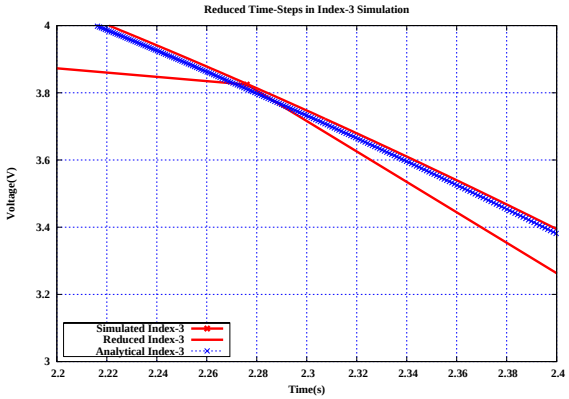

Fig. 5. Index-3 vs. Index-2 VHDL-AMS models

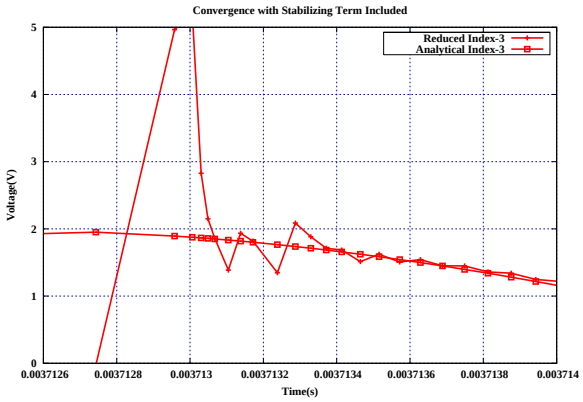

Fig. 6. Convergence of Regularized Variable

Fig. 5 compares the Index-3 and regularized variables from a VHDL-AMS model file. There is a noticeable divergence of the Index-3 variable from its analytical value. The regularized variable follows the analytical value more closely. An important effect noticed in this model was the number of solution points chosen: the Index-3 model was simulatable only with very loose tolerance levels. This led to an increased acceptance of erroneous solution points. This also explains the fact that only 25 solution points were chosen for the Index-3 model, compared to approximately 10^4 points for the regularized variable.

In Fig. 6 we compare the convergence properties of the regularized variable with its analytical value. The Index-3 variable could not be simulated in this case, even for extremely loose tolerance values. The regularized value was started off with inconsistent initial conditions, but still converged to its analytical value. This agrees with the convergence results of BDF methods for Index-1 or Index-2 DAEs which in turn verifies our claim that the DAE index is reduced by the regularization process.

Fig. 7 compares the Index-3 and regularized variable with its analytical value. The regularized value follows the analytical value very well, but the Index-3 variable accepts erroneous values due to the large tolerance values. Fig. 8 shows similar

$$\left(\frac{1}{ATOL(I_L)} \geq I_L^{(m+1)}\right) \wedge \left([I_L^{(m+1)} - I_L^{(m)}] \geq ATOL(I_L)\right) \implies \frac{1}{ATOL^2(I_L)} \geq \frac{I_L^{(m+1)}}{I_L^{(m+1)} - I_L^{(m)}} \tag{17}$$

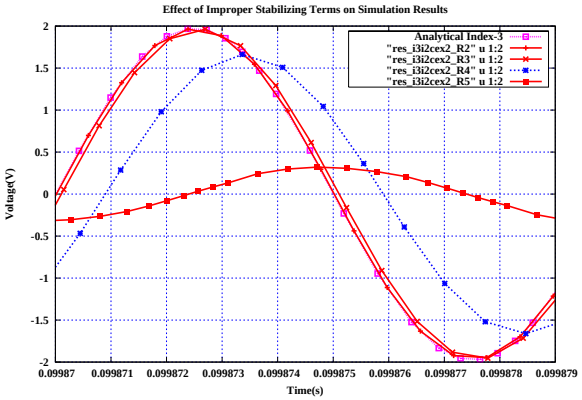

Fig. 9. Effect of Regularizing term on the reduced variable

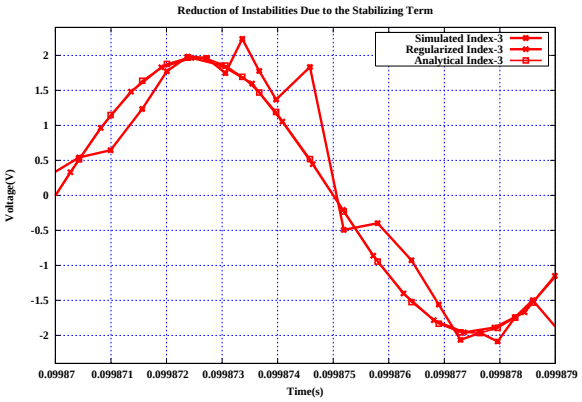

Fig. 7. Index-3 vs. Regularized Variable

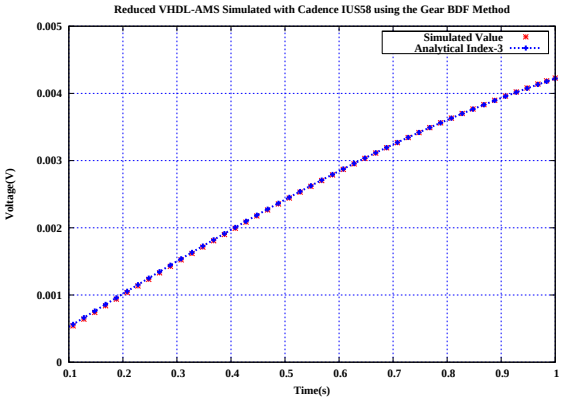

Fig. 8. Index2 vs. Analytical Value

results for another test case. The regularized variable follows its analytical counterpart closely. The Index-3 model in this case did not converge for even very high tolerance values.

Finally, Fig. 9 compares the effect of moving the bound away from that in (16). The value of h_{MIN} is many times smaller than the average time step of the simulation cycle, which allows the bound to be loosened during that time step. In this case, for values which exceeded the bound by up to 10^2, the simulated value is still close to its actual value. In most cases the computed value does not cause a blowup of the remaining system variables.

VI. Conclusion

We present a connection configuration that causes MNA to generate an Index-3 DAE to model the circuit equations. The occurrence is presented as a structural condition to detect its presence at the netlist level. A suitable regularization method is discussed to reduce the index of this DAE. The bound for this regularizing term is computable prior to the simulation process. Examples are shown where the addition of the regularizing term determined by this bound improves the simulation results in terms of accuracy and convergence properties.

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