# Issues on View Switching for RF SoC Verification

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## ABSTRACT

The main focus of this work is the functional verification of radio frequency systems on chip (RF SoCs). Different modeling approaches, like baseband modeling, analog modeling and event driven modeling, and their applications for verification are discussed. The possibilities and problems to use the Hierarchy Editor (HED) to switch between different modeling approaches on the fly in the top level schematic are discussed. Especially the cross domain connectivity issues between different model abstraction levels, like event driven modeling and analog modeling, are described in detail. Some suggestions for the circuit partitioning for verification purposes are given. This paper concludes with a suggestion for a possible extension of the Verilog HDL and the connect module insertion algorithm for the EDA industry.

## 1. INTRODUCTION

Verification is becoming a key component in today's design of highly integrated circuits. Due to the implementation of more and more digital functionality, like self adjusting and reconfiguration of the formerly analog-only circuit blocks, the clear separation between purely analog digital baseband signal path for large SoCs can no longer be maintained. While verification of digital-only designs is common and the EDA industry provides a whole bunch of tools for it, functional verification of analog or mixed signal designs is still treated poorly in state of the art design flows. A functional top level verification of sophisticated mixed signal systems prior tape-out phase is very tough, but getting more and more inevitable.

New Simulation techniques, like harmonic balance or periodic steady state analysis, increase the simulation performance in specialized analog RF circuits, but they are generally not suitable for mixed-signal simulations in large SoC circuits with lots of digital counterparts. Therefore, they are of no use for final full chip functional verification [2]. The only way of reliable functional verification leads back to transient system simulation, which is very time consuming, even with modern computational performance.

Hardware Description Languages (HDLs) offer a possibility to describe the desired behavioral of particular system block by substituting the abstract relations between the system components with simpler mathematical constructs. The aim of modeling the behavioral of the circuit blocks is to abstract the circuit description with sufficient accuracy to reduce the Simulation time. A successive insertion of optimized and therefore faster simulatable models allows a fast and reliable functional verification on top-level.

System engineers and circuit designers pursue a common goal: a functional system. On the one hand the circuit designer focuses on noise figure, frequency response and nonlinearity of the individual circuit, which can be handled with optimized analog simulators, like spectre. The system engineer on the other hand only thinks in terms of bit error rats (BER) or even package error rates (PER), which need huge number of received bits for a precise calculation, which leads to very long transient simulation times.

Due to the different concerns at the system functionality from circuit designer and system engineer, it is very important to provide one "Golden Schematic" for both of their verification purposes. A switchable top level test bench, with different model and signal abstraction levels, comes very handy in this case. In the following, approaches to partition the top level schematic for the verification of the system are given, different model abstractions are discussed and the problems resulting from them are described in detail with suggested solutions.

## 2. TARGET AND PROBLEM DESCRIPTION

Figure 1 shows a simplified top level schematic of a generic low-IF receiver chain, which consists of matching network, LNA, LO, mixer, polyphase filter and ADC. For the verification purpose, the entire system is divided gradually on basis of the top level schematic into individual isolated subsystems. In our case, the system can generally be partitioned into 2 parts: the RF part, which includes matching network, LNA, mixer and LO, and the IF part with polyphase filter and ADC. Each circuit block has its own specification and verification focus, which must be taken care of during modeling.

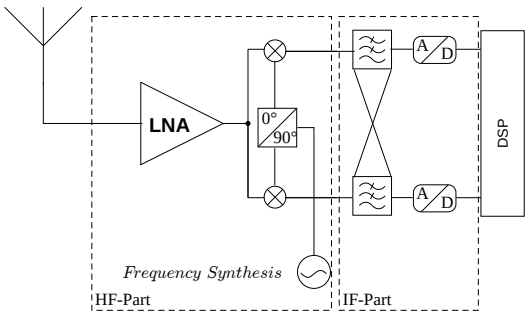



**Figure 1: A simplified low-IF receiver chain.**

For functional verification, it is important to be able to switch between different model abstraction levels. This comes in very handy, when being able to do a top level simulation with abstract models written in HDL, accomplished with only a small portion of the design on transistor level. This can be done with EDA Tools like the hierarchy editor (HED) from Cadence Design Systems [4]. With this feature, some critical problems on view switching for the verification arise. After a brief introduction of different modeling methods, the problems and the suggested solution will be discussed in detail.

# 3. ISSUES ON VIEW SWITCHING

There are different modeling methods to describe the behavior of a circuit block. The analog domain modeling is considered to be the first abstraction from the schematic. It consists of a functional mathematical description of the major behavior of a circuit.

With HDLs like Verilog-A, it is possible to create the description of the circuit using continuous time equations. The analog models are fully compatible with both the analog simulator like spectre and mixed signal simulator. The time steps during the simulation are determined by the highest frequency in the circuit, here: the carrier frequency. For high frequency circuits, the benefit from analog modeling is therefore not sufficient for longterm transient simulations.

Verilog-AMS supports a double precision data type (wreal), which enables the simulation in the digital domain with analog accuracy, therefore it is possible to separate the high frequency signal path into the digital domain [2]. Only changes fulfil the manually predefined sensitivity requirements trigger the analog simulator (event driven), thus it leads to a better simulation time benefit compare to the analog modeling method.

Since the carrier frequency can be assumed as a constant value with no information for the system, we can use the baseband modeling approach to stripe the carrier frequency from the original signal. Normally, a modulated signal can be described as:

$$X(t) = A(t) \cdot \cos(\omega_0 t + \theta(t)) \tag{1}$$

with the envelope $A(t)$, time-varying phase $\theta(t)$ and carrier frequency $\omega_0$. Its quadrature decomposition is then:

$$X(t) = X_I(t)\cos(\omega_0 t) - X_Q(t)\sin(\omega_0 t) \tag{2}$$

with the in-phase component:

$$X_I(t) = A(t)\cos(\theta(t)) \tag{3}$$

and the quadrature component

$$X_Q(t) = A(t)\sin(\theta(t)) \tag{4}$$

The complex baseband-equivalent signal for the original passband signal $X(t)$ is in this case:

$$X_{bb}(t) = X_I(t) + jX_Q(t) \tag{5}$$

The transformation from baseband-equivalent signal to the passband signal can be achieved using:

$$X(t) = \Re\{X_{bb}(t) \cdot e^{j\omega_0 t}\} \tag{6}$$

The information, which is necessary to describe a passband signal using its baseband equivalent are $X_I(t)$, $X_Q(t)$ and the carrier frequency $\omega_0$. Baseband modeling method leads to great speed improvement because of the neglect of the high frequency signal. To enable the possibility to switch between different model abstraction levels, the models must ensure pin compatibility with top level schematic, which is currently not possible by using baseband modeling approach with major HDL like Verilog-AMS. This is the main reason, why the baseband modeling approach is of only limited use for the bottom up verification [1].

One possible workaround for differential circuits diverts differential nets from their intended use to carry I- and Q-signals [5]. This workaround is limited by the original circuit design, it does not solve the mentioned problem, if the circuit is single ended. Also, using models with different pin definition is often false friendly, leading to unreliable verification results. Other approaches like analog domain modeling (continuous time) and event driven modeling (discrete time) [2] guarantee the pin compatibility, but there are still some issues that should be considered for the verification purpose. Figure 2 shows a typical scenario to accompany

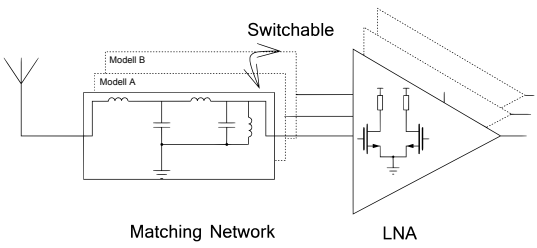



**Figure 2: View switching as provided by the Hierarchy Editor (HED). Here: a example with LNA and matching network.**

a LNA verification. The sub circuit is separated into two small portions: matching network and LNA. Each model can be implemented in different domain, like analog model for matching network and event driven model for LNA or vice versa. Unlike the analog modeling method, the event driven modeling approach can't model frequency depended load using impedance(like capacitor) or using Laplace transfer functions. An appropriate connect module (CM) has to

be inserted to join the two different modeling domains. The default connect module from Cadence Design Systems uses a resistance to convert analog signals into discrete event (digital domain) and vice versa [2]. Under the assumption that the impedance is matched at the center frequency, gives us the possibility to do a sufficient system simulation in the band of interest. However, this doesn't take the critical impact of RF impedance matching into consideration and is therefore not sufficient for simulation with blockers or wide band signals.

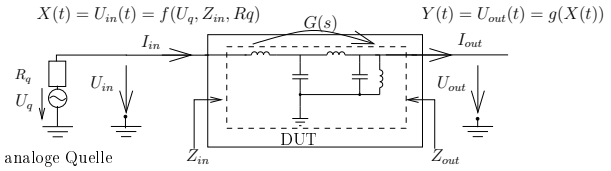



**Figure 3: Example of a analog model and the definitions of its input and output impedance**

One possible solution is to provide a connect modules with complex impedance definition. Let's consider the difference between the analog model and event driven model at first: Figure 3 shows an analog model representation with its input and output impedances, which are defined by the relationship of voltage and current at the input and output nodes based on Kirchhoff's law. The model can be described using following functions:
The input impedance:

$$Z_{in}(s) = \frac{U_{in}(s)}{I_{in}(s)} \tag{7}$$

The transfer function:

$$G(s) = \frac{U_{out}(s)}{U_{in}(s)} \tag{8}$$

and the output impedance:

$$Z_{out}(s) = \frac{U_{out}(s)}{I_{out}(s)} \tag{9}$$

A wreal wire contains only a single value. Therefore, only voltage or current from an analog model can be interpreted in a wreal wire [2]. Due to this information loss, a proper input or output impedance cannot be clearly defined in the event driven model.

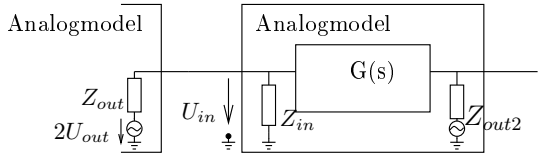



**Figure 4: Interface between two analog models.**

For connection between pure analog models (like figure 4), if the complex output and input impedance of adjacent models are matched ($Z_{out} = Z_{in}^*$), then the voltages are:

$$U_{in} = 2 \cdot U_{out} \frac{Z_{in}}{Z_{out} + Z_{in}} = U_{out} \tag{10}$$

Any change in the output or input impedance leads to change in the voltage characteristics. In this case, mismatched impedances based on circuit redesign or incomplete models can be proofed during the verification phase.

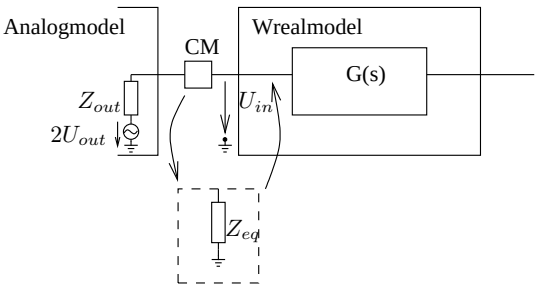



**Figure 5: Connect module between analog model and event driven model.**

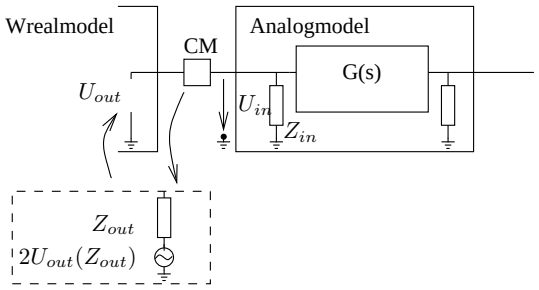



**Figure 6: Connect module between event driven model and analog model.**

Figure 5 and 6 show the standard implementation of the mentioned different connect modules.

From analog domain to digital domain (Fig. 5), the input of event driven model works like an open clamp, thus it appears that the input voltage of the event driven model is $U_{in} = 2U_{out}$, if both models are connected directly. The connect module should provide an equivalent load impedance $Z_{eq}$ at the input wire of event driven model. The default connect module from Cadence Design Systems "'E2R"' (electrical to wreal) has an input port resistance $Z_{in}$ of 50 Ω which is not sufficient to cover all the analog to event driven cross domain connection possibilities (mostly, $Z_{in}$ and $Z_{out}$ are frequency dependent).
Similar to the problem mentioned above, if there is a cross domain connection between a event driven model and a analog model (Fig. 6), the output of an event driven model works like an ideal voltage source. In this case $U_{out}$ and $U_{in}$ at the interface of the adjacent models are always the same. A change in the voltage characteristic due to mismatching based on design error cannot be detected. Therefore a connect module has to be inserted between both models. The connect module converts the output voltage of the event driven model in an equivalent, non-ideal voltage source like Fig. 6. The default CM "R2E"(wreal to electrical) uses a voltage source with a series resistance of 200 Ω, which is either not sufficient to cover individual cross domain connection possibilities.

A parametrizeable connect module that contains the input and output impedance information of the models at transistor level has to be implemented for keeping the correct connectivity at the interface. With the proper "E2R" CM, the input voltage of the adjacent event driven model is $U_{in} = 2 \cdot U_{out} \frac{Z_{eq}}{Z_{eq}+Z_{in}}$. For a parametrizeable "'R2E"' CM, the output voltage of the event driven model should be converted to $2 \cdot U_{out}(Z_{out})$. At the state of art, the manual implementation of connect modules is limited from the numbers of cross domain interfaces with different complex impedances at the top level schematic and their complexities. It is not feasible for a short and reliable verification phase, because the manual implementation of CMs can be very time-consuming and very error-prone.

The following source code (listing.1, listing.2) shows a suggested CM implementation. The frequency dependence of the load is modeled with a Laplace transfer function.

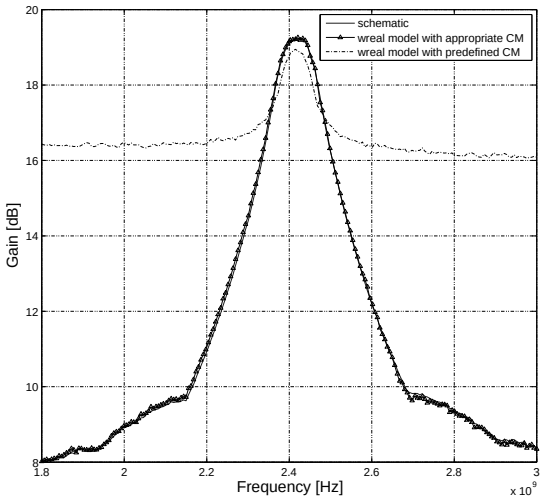



**Figure 7: LNA gain mismatch caused by different connect modules.**

A possible solution to the problems mentioned above at the current state of the art can only be based on a well thought out verification plan with meaningfully partitioned top level schematic.

```
connectmodule E2R (Ain, Dout);
input Ain;
electrical Ain;
wreal Dout;
real Dreg;
assign Dout = Dreg;
...
always @(absdelta(V(Ain), vdelta, ttol, vtol))
        Dreg = V(Ain);
analog begin
//parametrizeable impedance
//Zin_num and Zin_denom are based on block specs!
V(Ain)<+laplace_nd(I(Ain),{Zin_num}, {Zin_denom});
end
endmodule
```

**Listing 1: Electrical to wreal connect module example.**

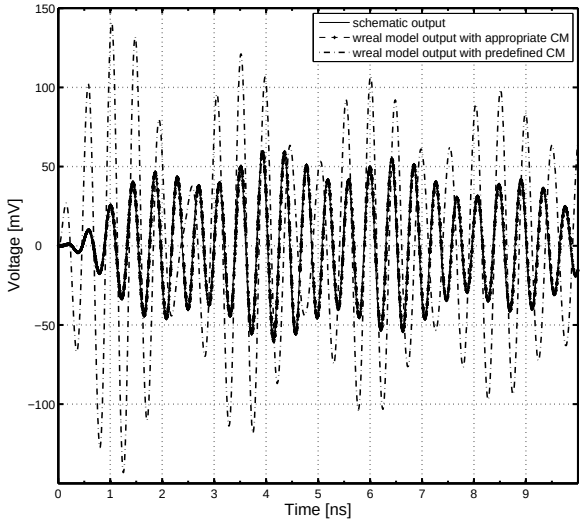



**Figure 8: transient response of LNA using different connect modules.**

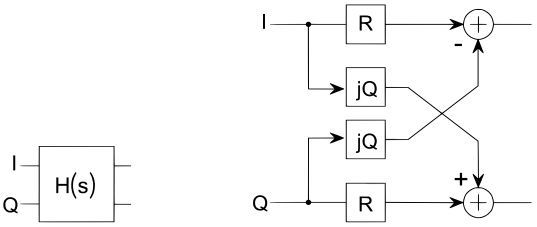
```
connectmodule R2E (Aout, Din);
input Din;
wreal Din;
output Aout;
electrical Aout;
real Vstate;
...
always @(Din) begin
assign Vstate=Din
analog begin
//parametrizeable impedance(or admittance.)
//Yout_num and Yout_denom are based on block specs!
I(Aout)<+laplace_nd(Vstate, {Yout_num},{Yout_denom});
end
endmodule
```

**Listing 2: Wreal to electrical connect module example.**

For verification of the IF-part, other effects and their impacts on the system as mentioned above should be considered. A polyphase filter for example can be described in different ways: Figure 9 shows different modeling possibilities for a widely used polyphase filter (PPF). While figure 9(a) represents the highest abstraction level, it is impossible to implement it into widely available HDL like Verilog-AMS, because its lack of definition of complex numbers. Figure 9(b) shows a realization of the transfer function using a real signal flow graph. Although this is a common way to implement the functionality in a system simulator using following equations:

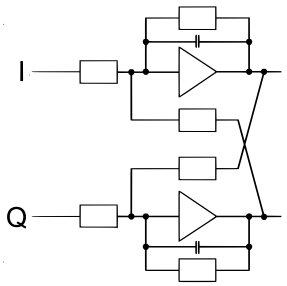
$$R = \frac{H + H^*}{2} \text{ and } jQ = \frac{H - H^*}{2} \tag{11}$$

As one can see, in partitioning (a) and (b) it would be sufficient to describe the transfer function of the filters. With this description, it is possible to do a system simulation without considering the non-idealities of a polyphase filter, which depends on the relation to the actual filter schematic im-




(a) Transfer function.

(b) Real signal flow graph.




(c) Schematic implementation.

**Figure 9: Partitioning possibilities of a polyphase filter.**

plementation. A modeling approach that is based on the schematic realization itself is shown in figure 9(c). In this case, additional specifications for the OpAmps (slew rates, GBW, supply voltages, offsets, etc.), are required. Some critical non-idealities of filters that have been implemented with OpAmps are showed in figure 10. The Impact of its parasitic capacitance ($C_p$), the finite DC gain ($A_v$) and especially the finite Gain Band Width ($GBW$) [9] on the system has to be modeled [8]. With the knowledge of the key

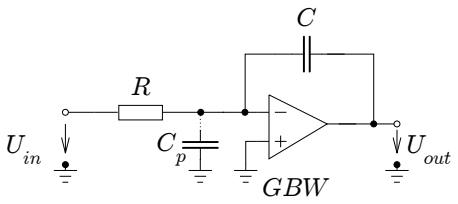



**Figure 10: Simplified OpAmp non-idealities in an polyphase filter cell.**

non-idealities, some negative effects of the OpAmp can be modeled with following descriptions:

- gain error $GE$:

$$GE = \frac{2\pi \cdot GBW}{\frac{1}{R \cdot C} + 2\pi \cdot GBW} \tag{12}$$

- parasitic pole $S_{LP}$:

$$S_{LP} = \frac{C}{C + C_p} \cdot (\frac{1}{R \cdot C} + 2\pi \cdot GBW) \tag{13}$$

For verification purposes, these nonidealities have to be mapped into the transfer functions that are simulated during block-design (Fig. 9(b)). This leads to the necessity to model the load of the polyphase filter. Only with this approach, the impact of the polyphase filter on the system like settling time or co-channel blocker can be estimated. It is therefore crucial, to define (based on designers and verification engineers experience) the test bench possibilities of the partitioned circuit blocks to estimate the necessary specifications at first.

For a receiver chain with low bandwidth like figure 1, the verification target of the HF-part should be defined at the very beginning of a verification process: For pure PER or BER simulation without the consideration of blockers or interferers, only event driven modeling is needed. In this case, the high frequency part is separated into the digital domain, the analog simulator is only triggered for predefined voltage changes at the output stage [2]. An event reduction algorithm should be implemented at the output of mixer model, because of the large frequency difference between input (RF) and output (IF) of mixer results a large event number at the output stage [6]. The achieved speed up with event driven modeling is not as good as the baseband modeling approach [2]. But as mentioned above, with event driven modeling, the pin compatibility with the top level schematic can be guaranteed. This leads to a less error prone and therefore more reliable verification.

# 4. RECOMMENDATION FOR HDL AND EDA EXTENSION

For a fast verification process, the event driven modeling is a better way to solve the pin compatibility problem with great speed up, but the manual definition of its connect modules at the cross domain interface like mentioned above leads to a high time-consuming and error-prone verification process. This problem can be solved by implementation an automatic parameterizable connect module insertion function: The parameter of the load or the input impedance of the adjacent circuit can be automatically modeled with its specification defined at the pins of the models. This extension would lead to a faster and more reliable verification process.

# 5. CONCLUSIONS

In this work, the assets and drawbacks of different modeling technique like baseband modeling, analog modeling and event driven modeling are discussed. The trend to speed up the verification process of RF analog circuit is to separate the carrier frequency during simulation, either into the digital domain, which is realized with event driven modeling or just neglect it during analog simulation like baseband modeling approach. Different key aspects for the verification of RF and IF-part of a generic low-IF receiver structure are given. Some problems depend on HDL or EDA feature are shown, and some possible suggestion to improve them are made. For a feasible and reliable functional verification process, it is very important to combine different modeling techniques to achieve the most accurate behavioral description of the Circuits and th systems. In addition to the suggestion, a meaningful planned design and verification process can bridge the gap between system engineers and circuit designers. This could be a very important step for the large

SoCs design.

## Acknowledgment

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