Behavioural Performance and Variation Modelling for Hierarchical-based Analogue IC Design

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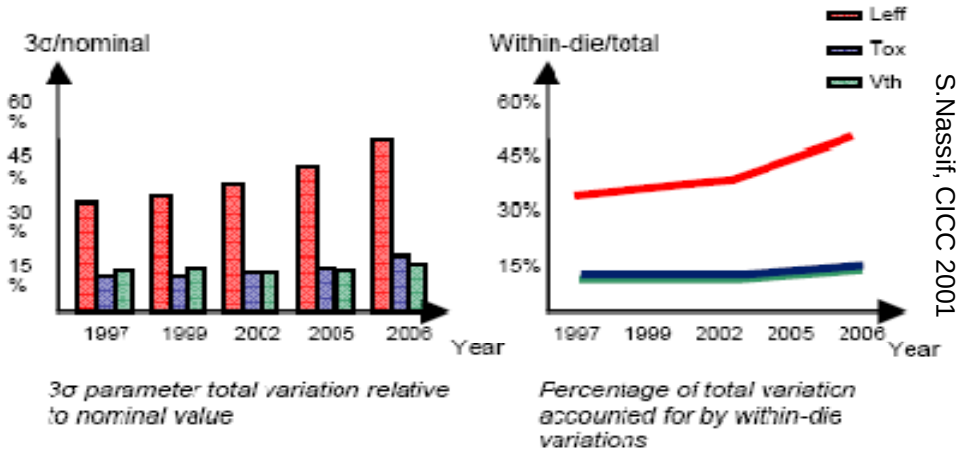
Outline

- Introduction
- Background
- Design algorithm
- Experimental results
- Conclusions

Introduction

- **Silicon Technology Development**
  - Reduction of transistor size
  - Mixed signal emphasis
  - Analogue circuits must use the same transistors as their digital neighbours
  - Device model getting more complex

- **Variation**
  - On-chip variation is getting worse
  - Circuit yield falls below specifications
  - Yield must be considered early on (DFY)

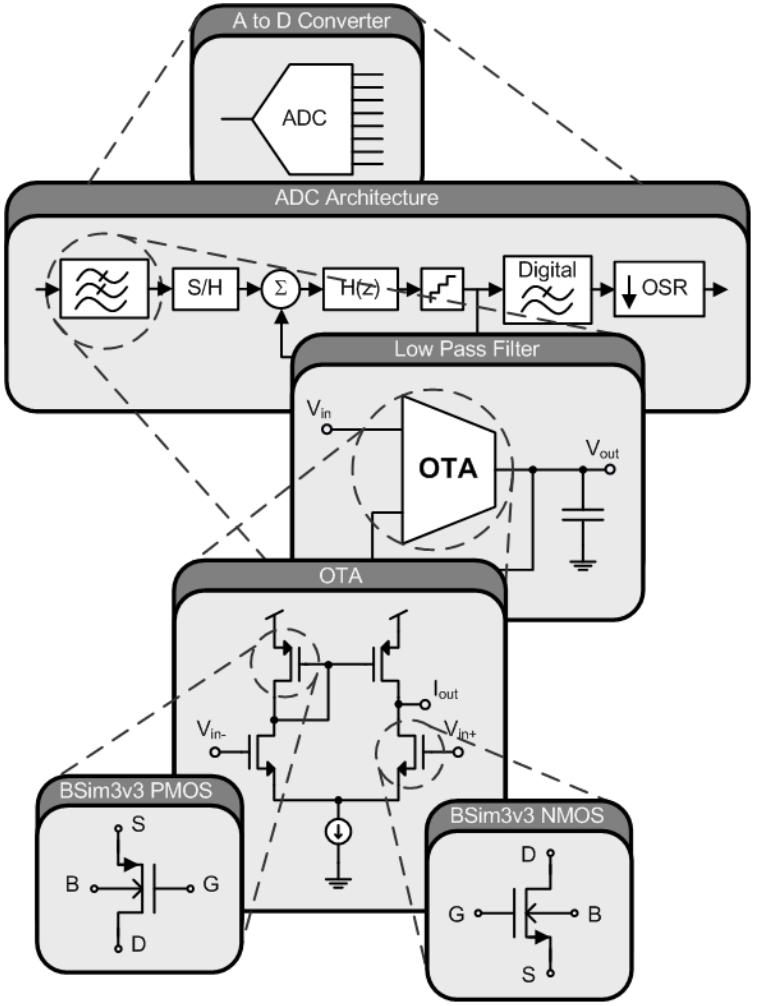


3σ parameter total variation relative to nominal value

Percentage of total variation accounted for by within-die variations

Introduction

- **What is analogue IC Design ?**
  - Topology selection, circuit sizing & biasing to meet specifications
- **Design Evolution**
  - Hand-calculation → automatic sizing (CAD)
  - Models complexity has led to simulation based optimization
- **Hierarchical-based design**
  - Breaking large systems into sub-blocks to simplify the design task
  - Speeds up the design flow by encouraging design reuse



Typical system design hierarchy

Introduction

- **Research Motivation**
  - Analogue circuit design automation is important to reduce design cycle time for mixed-signal circuits
  - Yield must be considered early on in the design process due to the increasing impact of process variation
  - Automation techniques can be used in hierarchical-based designs to solve the problem for large circuits
- **Research Objectives**
  - Develop a methodology for analogue circuit design that considers yield as one of the design parameters
  - Develop a circuit model that characterizes analogue circuit performance and yield
  - Apply the developed circuit model in a hierarchical-based design of a larger circuit

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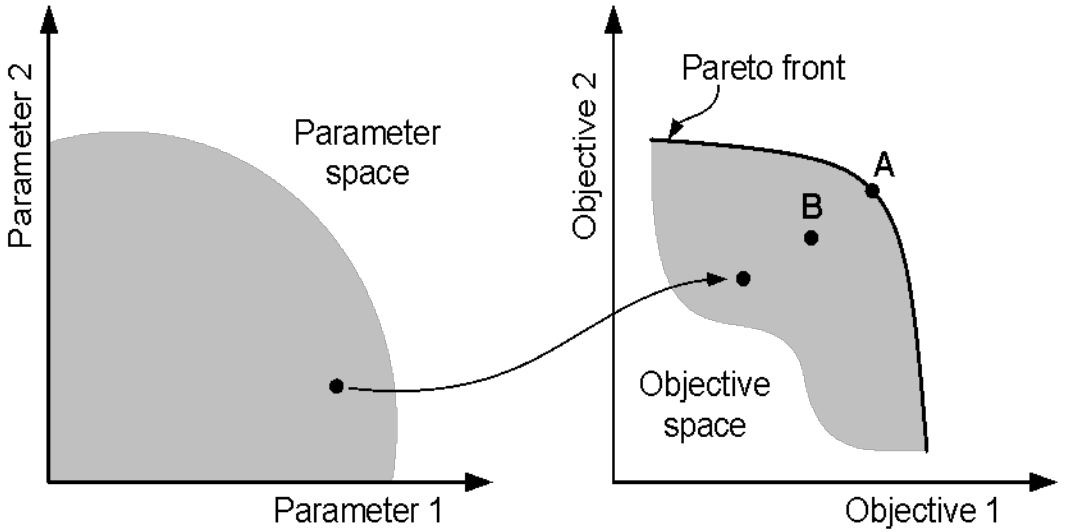
Background - MOO

- **Multi Objective Optimisation**
  - Optimisation formulation for more than one objective

$$Minimise / Maximise \; f_m(x),\; m = 1,2...M$$

$$Subject\ to\ g_j(x) \geq 0,\; j = 1,2...J$$

  - The outcome : set of optimal solutions ⇨ PARETO FRONT



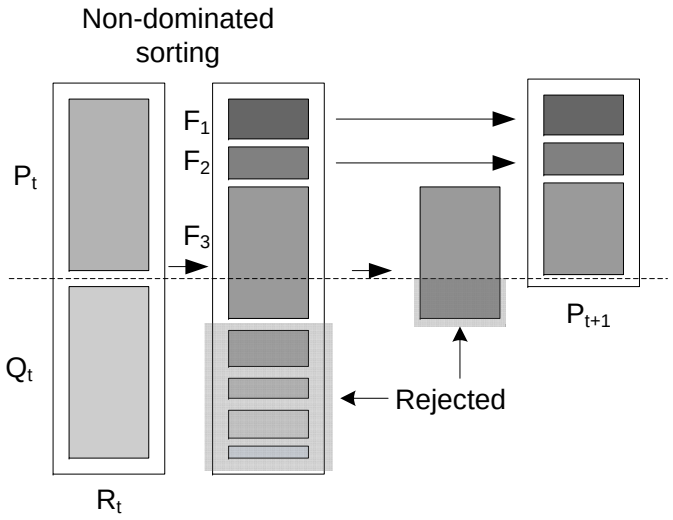
Background – Optimisation Algorithm

- **Non-dominated Sorting GA–II (NSGA-II)**
  - Uses elite preserving strategy to ensure that good design solutions found early on can be directly carried over to the next generation
  - Uses diversity preserving mechanism to ensure diversity among the solutions points

NSGA Algorithm

- Generate initial random population, size N.
- Create offspring population.
- Combine parent and offspring population to form R_t. ($R_t=P_t \cup Q_t$)
- Perform non-dominated sorting and identify fronts, F_i (i=1,2...etc)
- Set new population, $P_{t+1} = 0$, and fill P_{t+1} with F_i ,($P_{t+1} \cup F_i$) as long as $|P_{t+1}|+|F_i|<N$.
- Perform crowding sort and place most widely spread solution in P_{t+1}
- Create offspring populaiton Q_{t+1} from P_{t+1} and repeat until last number of generation.

NSGA-II Algorithm

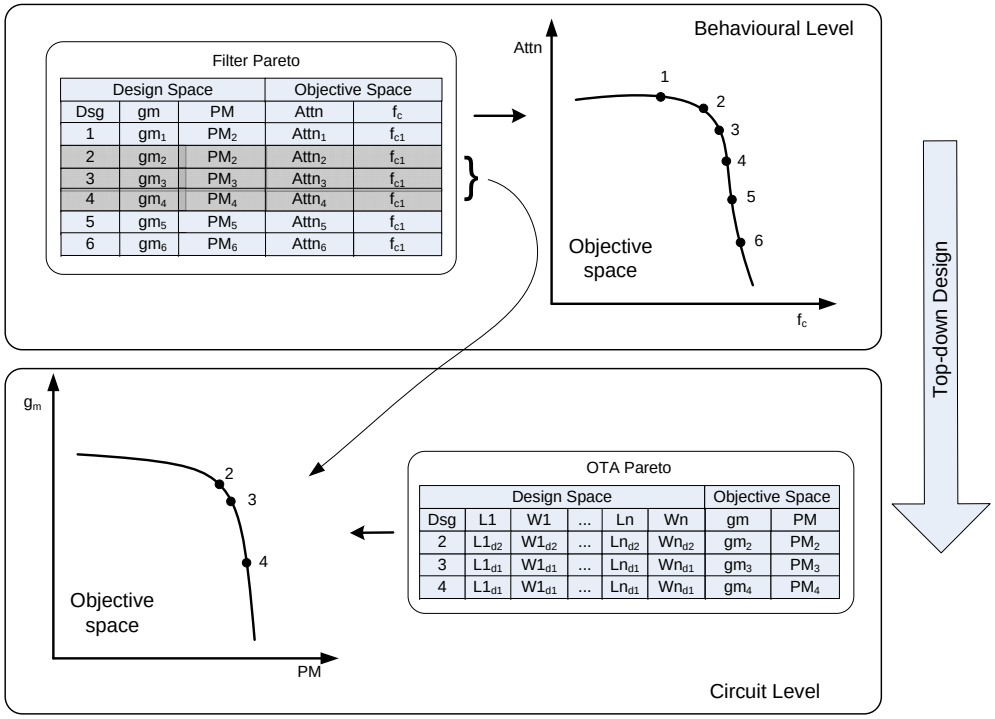


NSGA-II Strategy

Background – Hierarchical-Based Design

- **Hierarchical Based Design**
  - Top-down design & Bottom-up verification
  - Important Aspects are circuit decomposition & specification propagation

- **Optimisation Steps**
  - Behavioural-level MOO to determine design parameters that meet system level specification
  - Circuit-level MOO to determine circuit parameters to meet behavioural level design parameters



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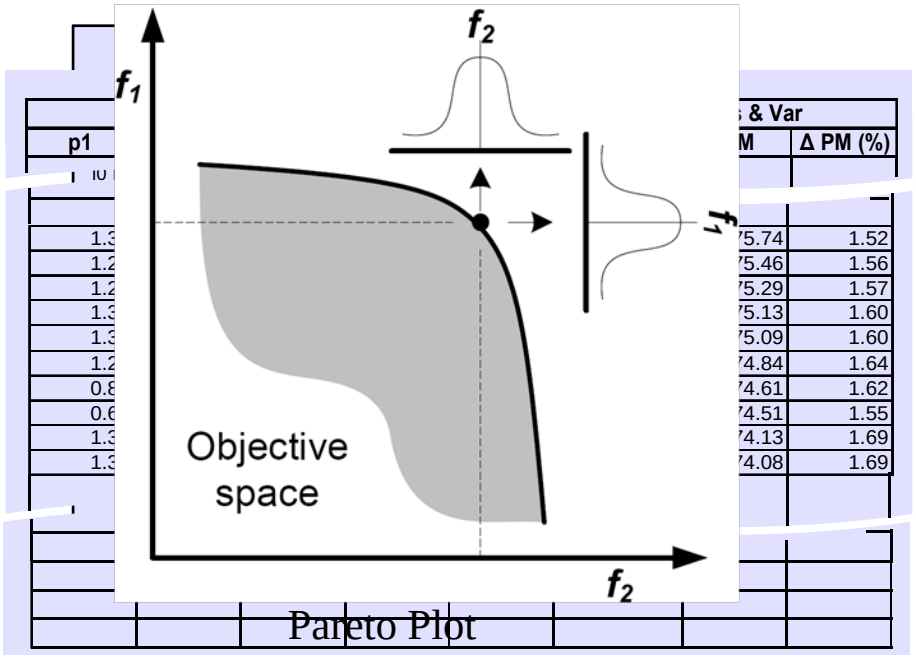
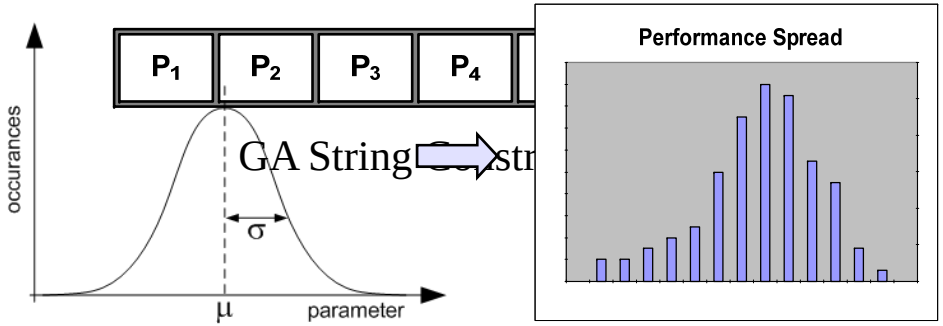
Design Algorithm

- **Algorithm for performance and variation model**



Pareto Plot

Performance and Variation Lookup Table



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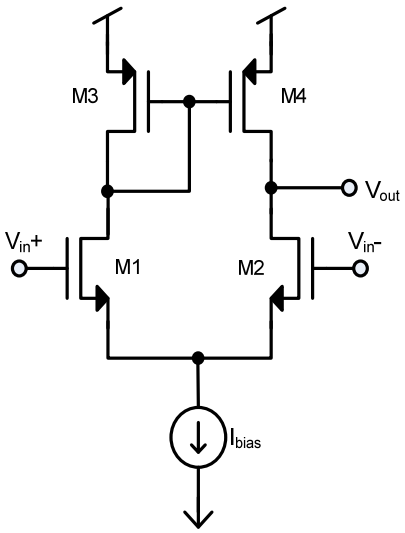
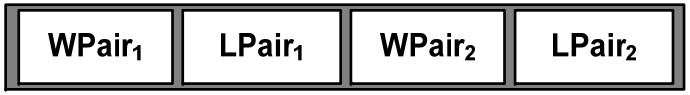
Experimental results

- **Performance & Variation Model Development**
  - Simple OTA is used as the target circuit
  - Simulations were performed with Spectre and 120nm foundry models
- **Design Setup & Multi Objective Optimization**
  - 4 designable parameters
    - Width & Length (M1&M2), Width & Length (M3&M4)
  - 3 performance functions: gm, ro & pm
  - Design parameter ranges:
    - Length : 0.12µm - 4µm
    - Width : 0.12µm - 120µm
  - MOO parameters :
    - No. of generations : 50
    - Population size : 400
    - Total samples : 20,000

OTA Topology



GA String



Experimental results

- **Performance and Variation Modelling**
  - Outcome of the MOO is a set of optimal solutions (Pareto-front)
  - Number of Pareto solution points: 211 solutions
  - Monte Carlo simulation with 200 samples was performed on all Pareto-front points to determine their variations
  - Each performance and variation are stored in a lookup table.

Design:	gm :	Δgm:	ro :	Δro:	pm:	Δpm :
2	109µ	0.75%	382k	0.75%	87.9	1.74%
3	109µ	0.75%	384k	0.75%	87.8	1.73%
19	110µ	0.74%	371k	0.74%	88.0	1.73%
34	111µ	0.75%	497k	0.74%	85.3	1.71%
35	111µ	0.73%	375k	0.75%	87.9	1.73%
61	112µ	0.73%	458k	0.74%	86.1	1.71%
209	120µ	0.70%	486k	0.74%	82.7	1.70%
211	120µ	0.70%	743k	0.72%	74.9	1.69%

Performance and Variation Lookup table samples

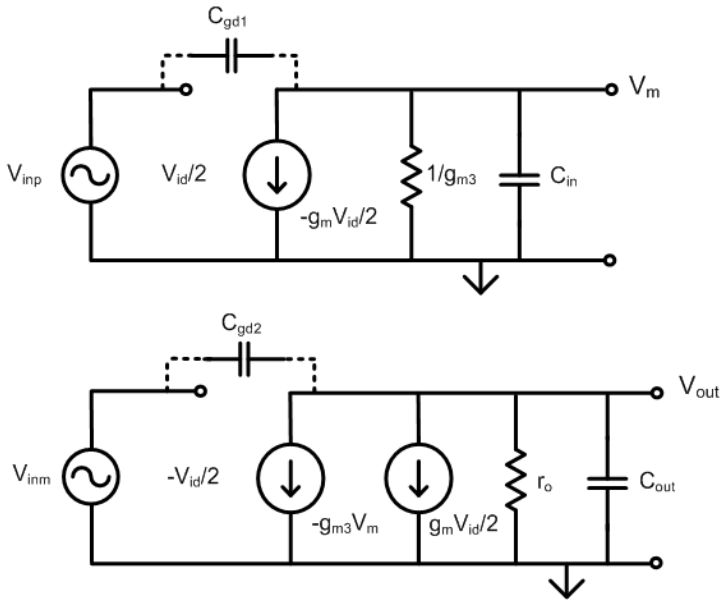
Experimental results

- **Verilog-A Lookup Table**
  - Table_model() function defines the OTA performance & variation

```
analogue begin
 gm_delta = $table_model (gain, "gm_delta.tbl", "3E");
 ro_delta = $table_model (ro, "pm_delta.tbl", "3E");
 pm_delta = $table_model (pm, "pm_delta.tbl", "3E");
 gm_prop = ((gm_delta/100)*gm)+gm;
 ro_prop = ((ro_delta/100)*ro)+ro;
 pm_prop = ((pm_delta/100)*pm)+pm;
 p1 = $table_model (gm_prop,ro_prop,pm_prop
 "p1_data.tbl","3E,3E,3E");
 p2 = $table_model (gm_prop,ro_prop,pm_prop
 "p2_data.tbl","3E,3E,3E");
 p3 = $table_model (gm_prop,ro_prop,pm_prop
 "p3_data.tbl","3E,3E,3E");
 p4 = $table_model (gm_prop,ro_prop,pm_prop
 "p4_data.tbl","3E,3E,3E");
 fptr=$fopen("params.dat");
 $fwrite(fptr, "\n Generated Design Parameters\n ");
 $fwrite(fptr, "%e %e %e %e", p1,p2,p3,p4);
 $fclose(fptr);
 $display ("params: = %e %e %e %e", p1, p2, p3, p4);
End
```

Experimental results

- **OTA Behavioural Model**
  - A behavioural OTA model is developed from the small signal model
  - All parasitic capacitances are included to accurately model the high frequency behaviour
  - The behavioural model is used for the system level design



OTA small signal model

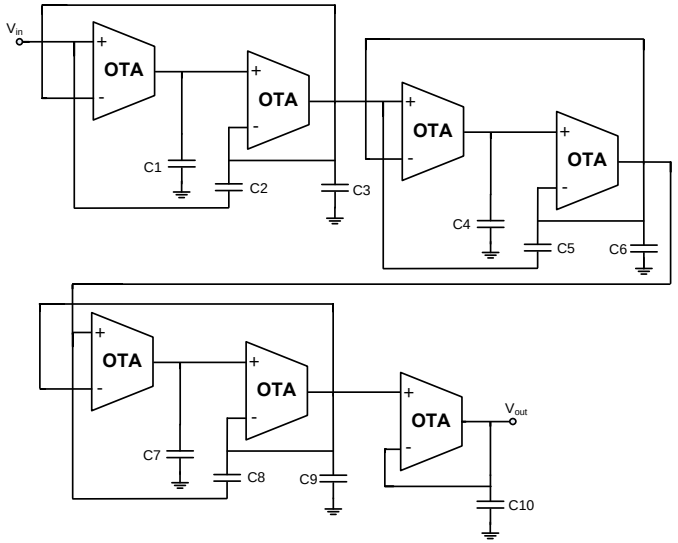
```
Module ota(inp, inm, out)
    ….
    parameter real gm = 60e-6;
    parameter real ro = 1e+6;
    electrical inp, inm, out, vm;
    real vin;
analog begin
    // high frequency model
    vin = V(inp,inm);
    I(vm) <+ -gm*(vin/2);  // gm transistor M1
    I(vm) <+ cin*ddt(V(vm)); // cin is input cap
    I(vm) <+ cgd1*ddt(vin/2); // miller effect of cgd1
   …
    I(out) <+ -gm3*V(vm);
    I(out) <+ -gm*(vin/2);
    …
    V(out) <+ I(out)*ro;
    …
end
endmodule
```

Listing 2. OTA Behavioural Model

Experimental results

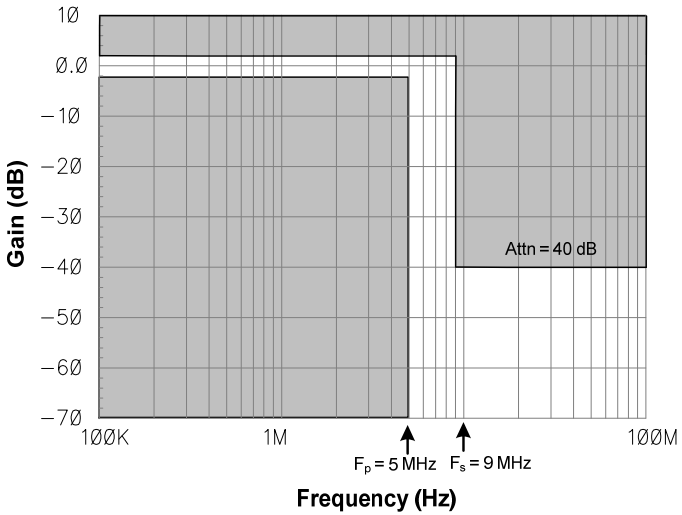
- **Hierarchical Optimization**
  - System level application: 7th order Video Filter
  - Designable parameters: transconductance (gm) & capacitor values
  - MOO parameters :
    - Population size : 600
    - No. of Generation : 50

GA string



7th order elliptic filter schematic

Filter Specification



Experimental results

- **Hierarchical optimization**
  - Filter multi objective optimisation
    - Outcome of MOO: Pareto-points
    - Sample solutions that meet filter specifications
    - Ensure gm is achievable with topology (refer to lookup table)

Design:	gm (μ) :	Attn (dB):	Fp(MHz):	Fs(MHz):
11	122.3	40.3	6.1	8.3
22	131.6	47.4	5.4	7.5
15	108.9	45.9	5.3	7.3
70	113.8	55.1	5.7	8.9
61	130.4	61.7	5.7	8.9

Filter Pareto Samples

Experimental results

- **Hierarchical-optimisation (continued)**
  - Interpolate OTA variation & determine min & max performance
  - Apply OTA min & max values to determine filter performance
  - Select a solution that meets the specifications

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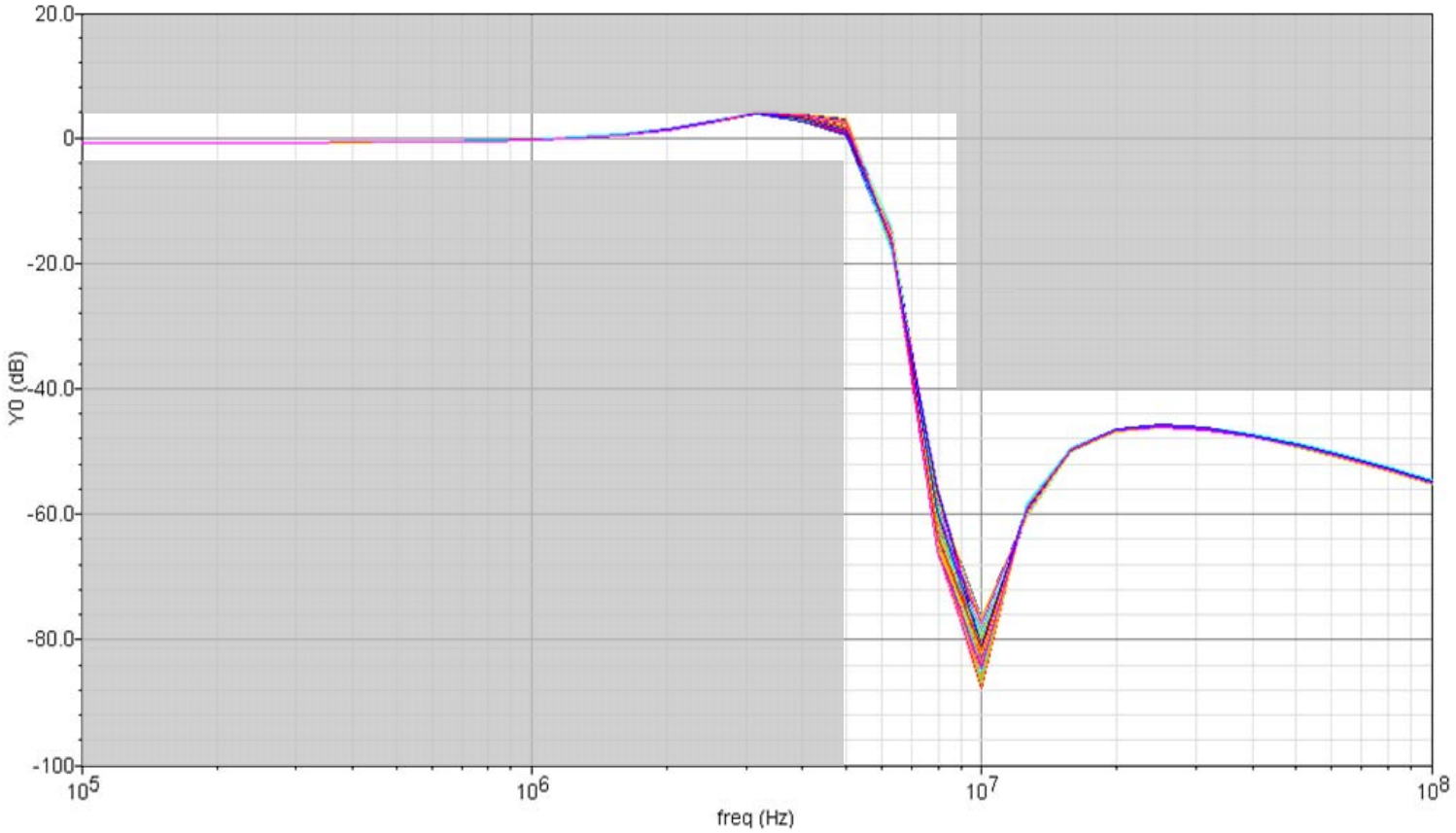
OTA Lookup Table

Experimental results

- **Transistor level verification & Monte Carlo plot (gm = 108.9μS)**



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Conclusions

- A new approach for analogue circuit design has been proposed that include yield as one of the parameters
- A model that combines performance and variation of an analogue system has been developed
- A lookup table is developed using Verilog-A for the performance and variation model
- The method has been implemented in hierarchical-based design of 7^{th} order filter
- Transistor level simulation verifies the behavioural performance and variation model used in the system level design

Questions?

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Another example

- **Ripple <0.5dB, cutoff 4.5MHz, stopband 9MHz, att 40dB**