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Behavioural Modelling for Stability of CMOS SRAM Cells Subject to Random Discrete Doping

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Outline

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- **Background**
- **Effects of $R_{andom}D_{iscrete}D_{oping}$ on CMOS SRAM**
- **VHDL-AMS Behavioural Model Development**
- **Verification by SPICE**
- **Conclusions**

➢ Background — Variability

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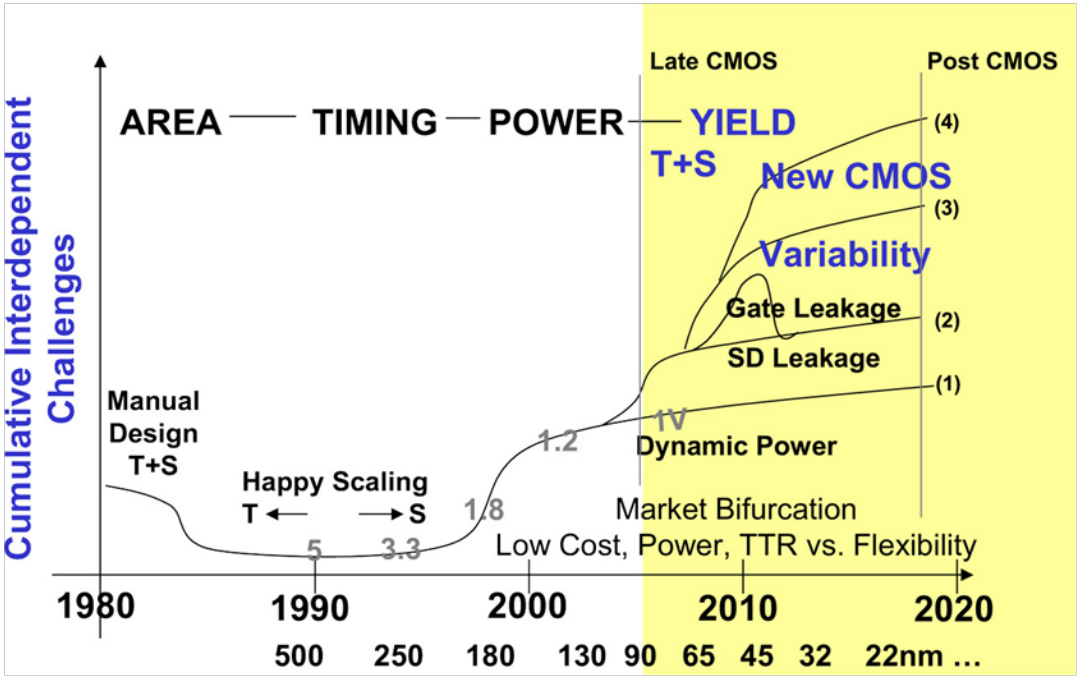
Variability is becoming a major challenge in the near future



G. Declerck, VLSI Technol. Symp., 2005, p. 6-10

➢ **Source of variability**

Intrinsic,
Atomic-level differences between devices, Irrespective of layout and environment.

Extrinsic,
--lot to lot;
--wafer to wafer;
--across wafer;
--chip to chip;
--within a chip.

➢ Background — Variability (Cont.)

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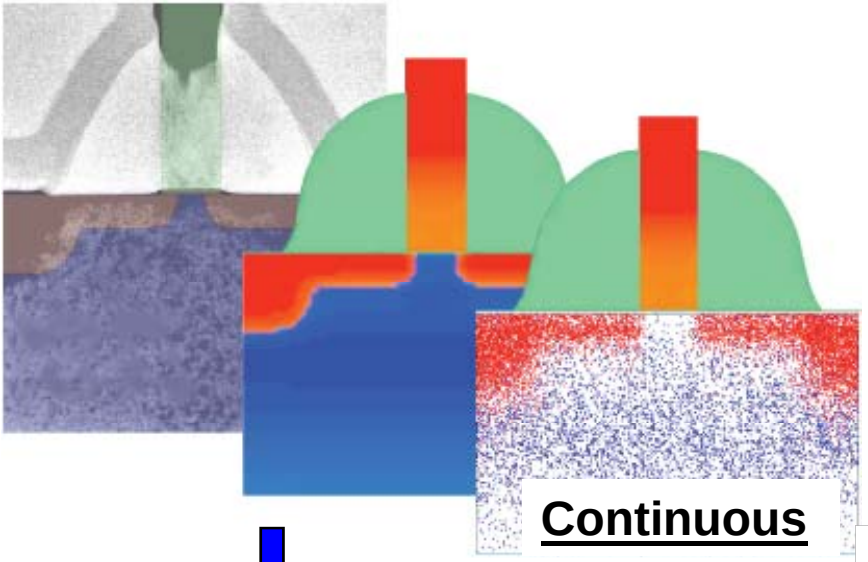
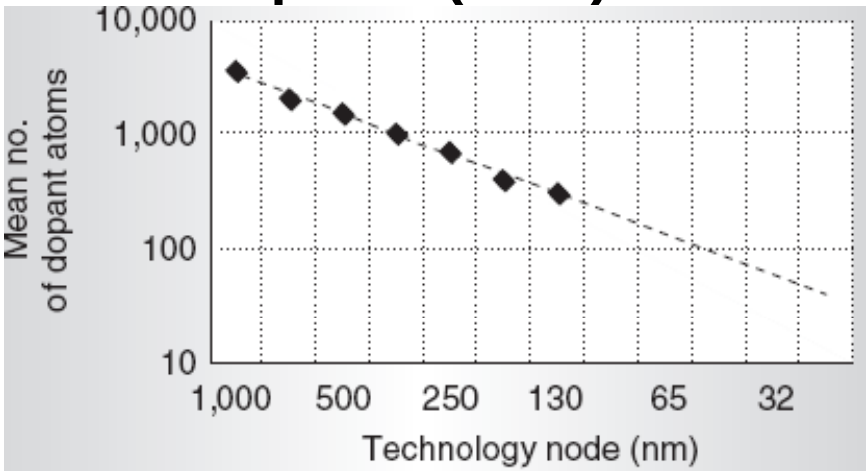
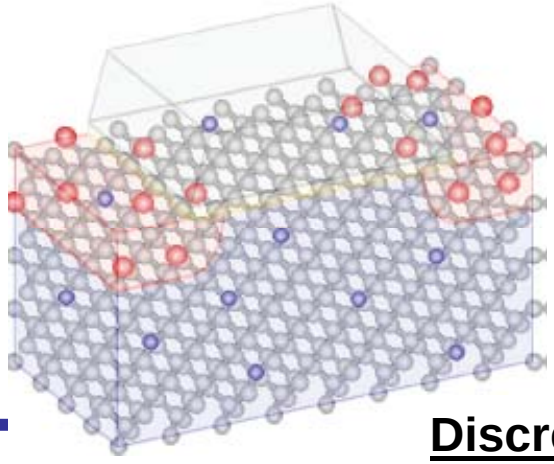
✓ Intrinsic Variability — **Random Discrete Dopants (RDD)**



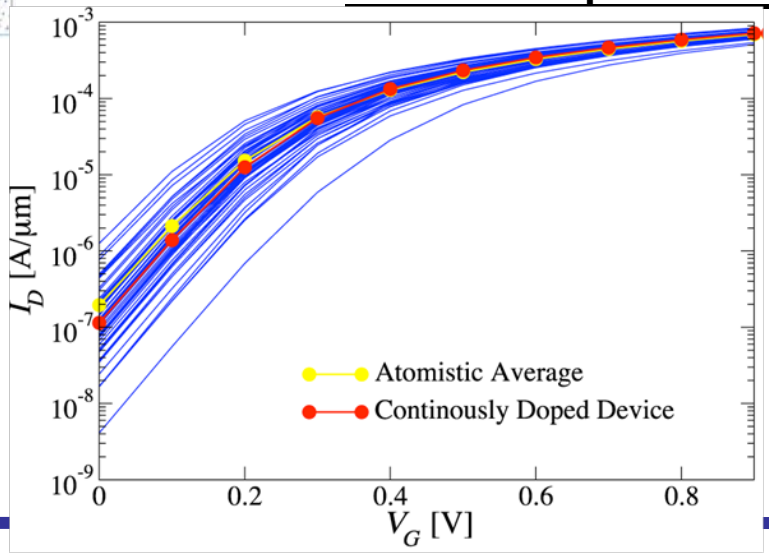
Continuous



Random Dopant Fluctuations



Discrete



I_{ds} and V_{th} Variations

➢ Background — Variability (Cont.)

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✓ Intrinsic Variability — **Line Edge Roughness (LER): L_g, Interconnect;**
— **Oxide Thickness Fluctuations (OTF): Leakage;**
— **Poly Silicon Grain Boundaries.**

Fluctuation (mV)	V_{th} (Ave)	σV_{th}	Calc. σV_{th}
RDD	**133**	**33.2**	
LER	126	19	
OTF	122	1.8	
RDD&LER	126	38.7	38.2
RDD&OTF	123	33.9	33.3
LER&OTF	113	22.8	19.1

Source	σV_{th} (mV)	Comment
RDD&LER& OTF	40	35nm, Simulation
H. Fukutome	49	40nm
F. Arnaud	63	65nm

Effects of RDD, LER, OTF on 35 nm conventional MOSFET,
From Glasgow Device Modelling Group Reports

➢ Background — Modelling Hierarchy

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- Transistor-Level (TCAD) and Circuit-Level (SPICE) simulation get more details with longer simulation time, models are existing.
- Gate (Verilog) and RTL (VHDL) focus on digital system modelling, limited analogue and mixed-signal modelling.
- A trade-off for accuracy and speed is Analogue Behavioural Modelling (ABM), Verilog-AMS or **VHDL-AMS**.

➢ VHDL-AMS

A. Behavioural models are **simple**, **fast, continuous,** but no existing models

B. Model developing: By **fitting** simulation results of cell behavioural to extract model parameters.

C. To describe the cell behavioural by VHDL-AMS.

➢ Background — SRAM Cell

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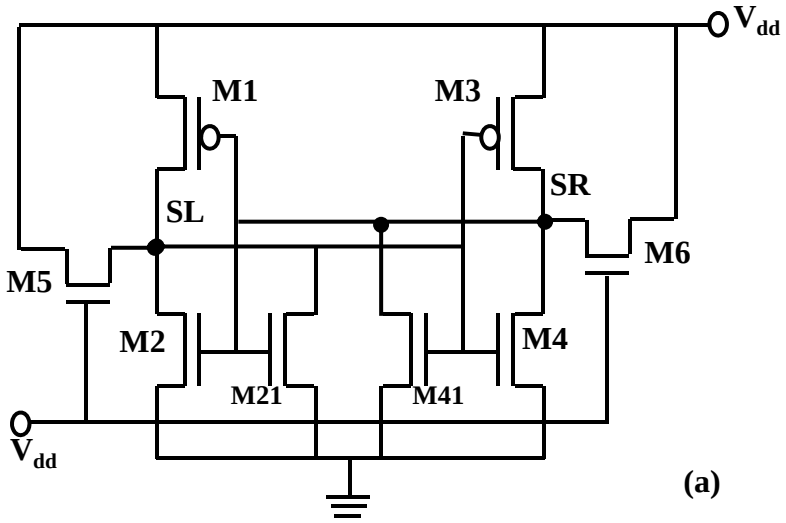
✓ One of the most important components in modern microprocessors and SOCs,

✓ Be considered as the benchmark circuit for developing of CMOS technology.

✓ Stability characterized by the static noise margin (**SNM**) during read period, which accounts for the ability of the cell to maintain stable data under parasitic noise and device mismatches.

✓ **SNM** is affected **by Random Doping.**



Bias configuration For SNM

➢ Effects of RDD on CMOS SRAM

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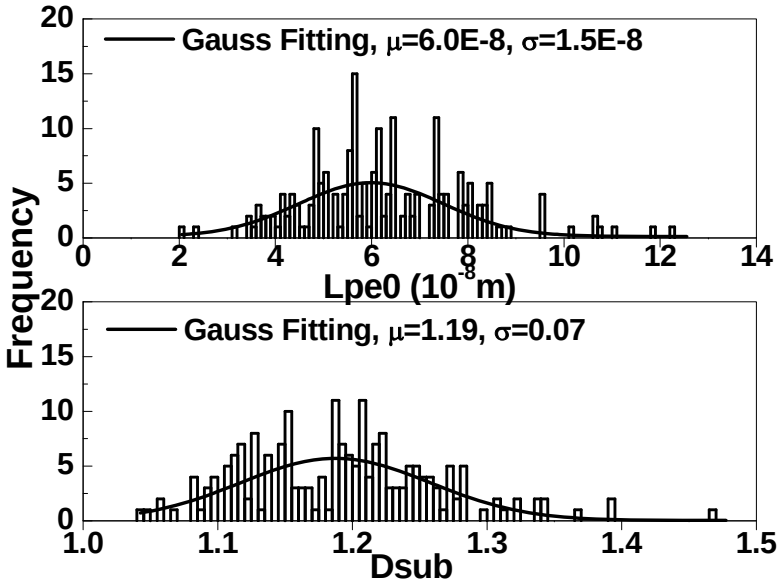
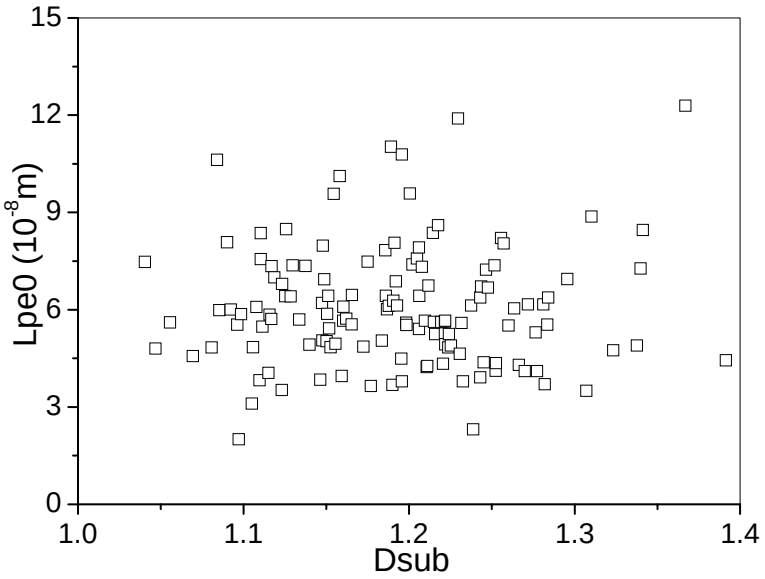
RDD Related 35nm bulk Devices BSIM4 Model Parameters

Lpe0: Lateral non-uniform doping parameter at Vbs=0,
Dsub: DIBL coefficient exponent in subthreshold region**,**
Voff, a1, a2, Rdswmin and **nfactor.**

Main contributions to ΔVth





Parameters	Skewness	Kurtosis
Lpe0	0.6997	0.85
Dsub	0.6648	1.19

Data from Device Modelling Group of Glasgow, 200 35nm Compact Models

➢ Effects of RDD on CMOS SRAM (Cont.)

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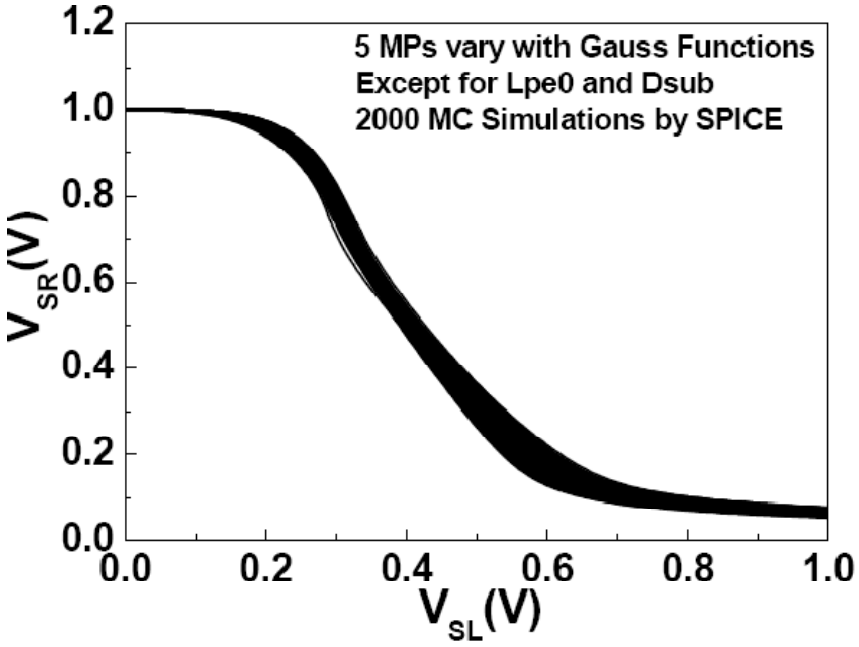

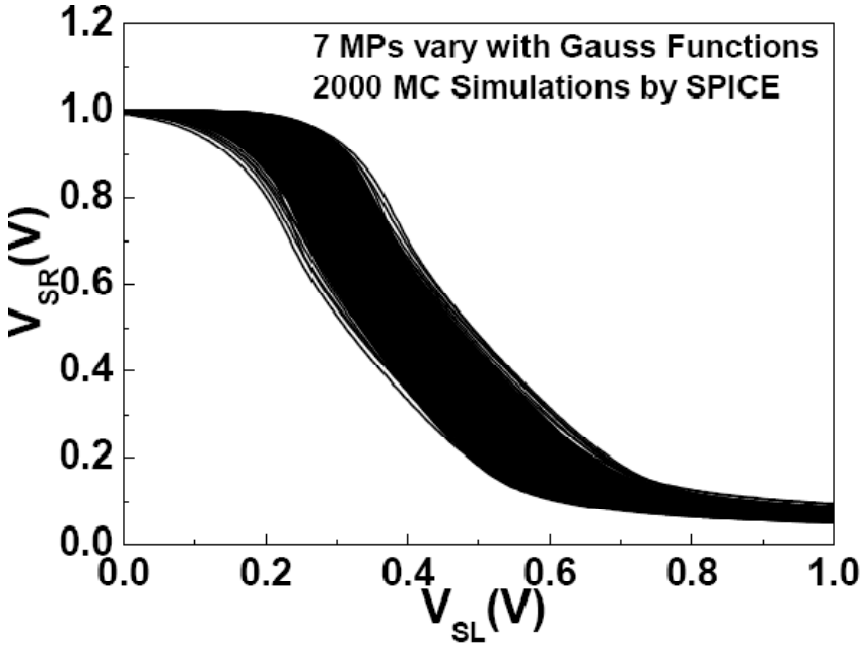

With Voff, a1, a2, Rdswmin and nfactor variations

With all RDD parameters variations

Simulation method

- ➢ Doing Monte Carlo simulations by H-SPICE,
- ➢ All the devices are set differently.

➢ Effects of RDD on CMOS SRAM (Cont.)

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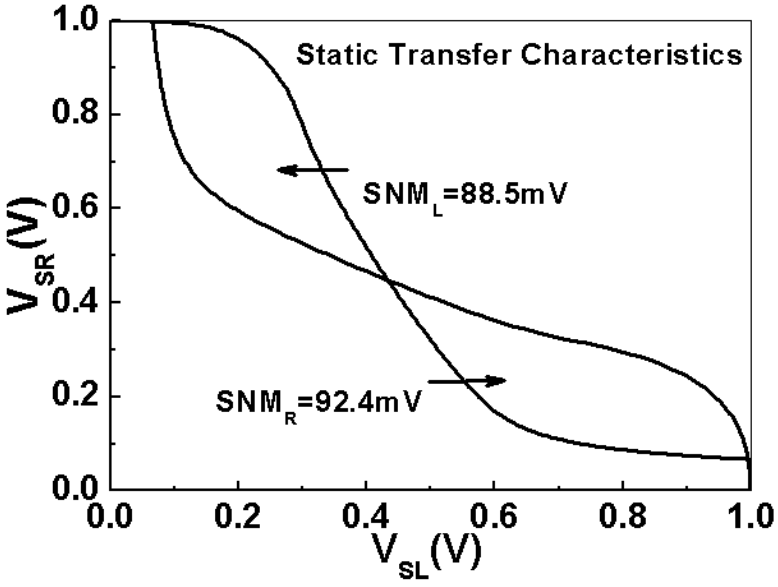

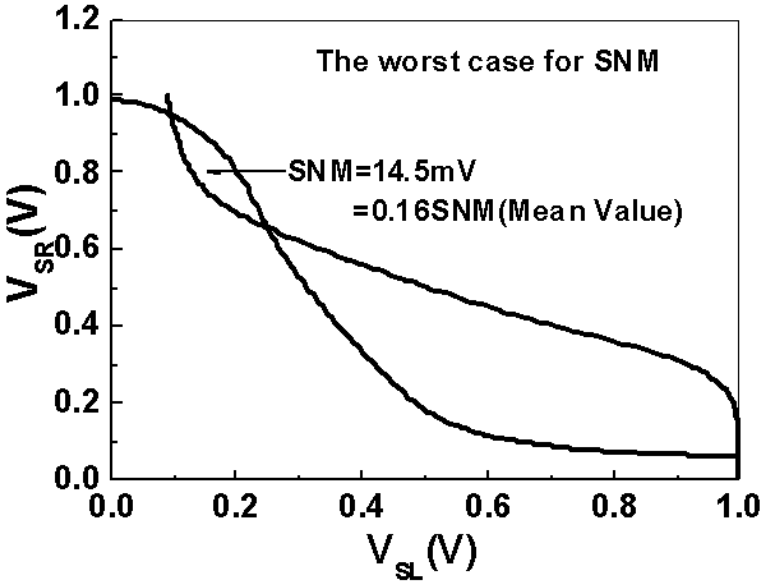

SNM Definition

The smaller area formed by two Static Transfer Characteristics By sweeping V_{SL} or V_{SR}.

The worst case for 2000 MC simulations

➢ VHDL-AMS Behavioural Model Development

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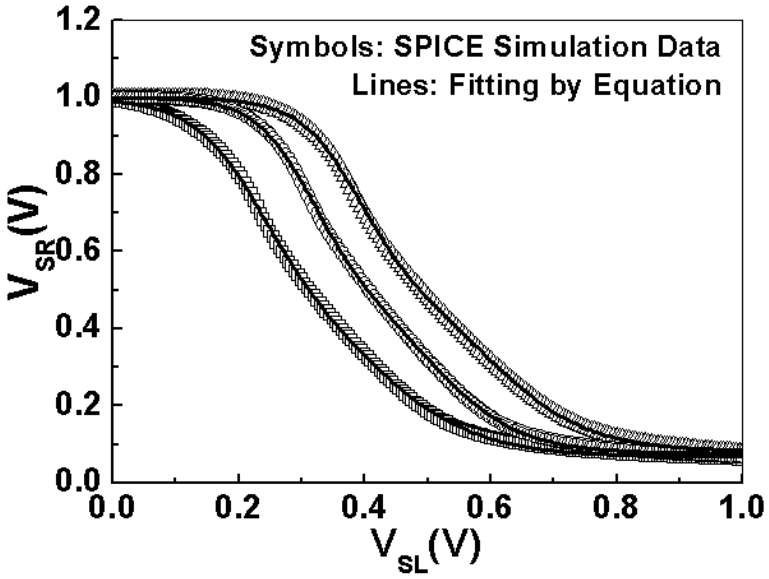
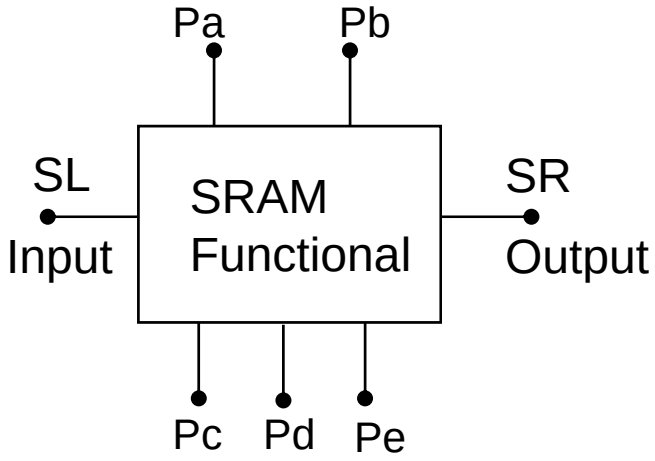
SRAM STC Behavioural:

Two-level **Sigmoidal** function
5 fitting parameters (FPs)



The SRAM Behavioural Model for RDD:

- Electrical input and output terminals,
- Five signal inputs for fitting parameters,
- Not all FPs are independent, only Pb.



$$V_{SR} = P_a + \frac{1-P_a}{2\times\left[1+e^{(V_{SL}-P_b)/P_c}\right]} + \frac{1-P_a}{2\times\left[1+e^{(V_{SL}-P_d)/P_e}\right]}$$

➢ VHDL-AMS Behavioural Model Development (Cont.)

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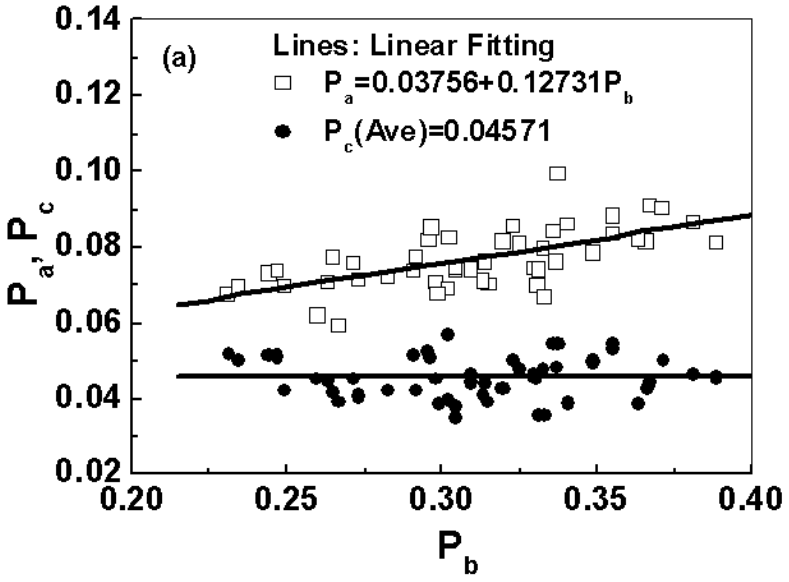

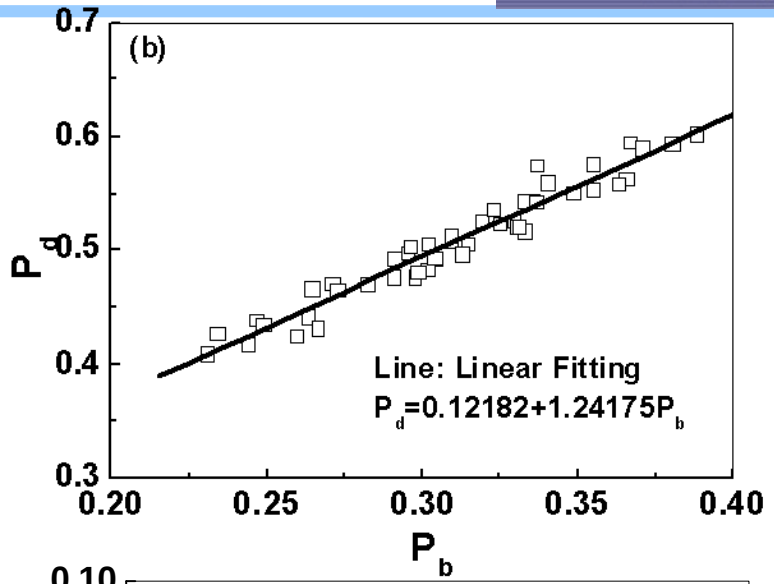

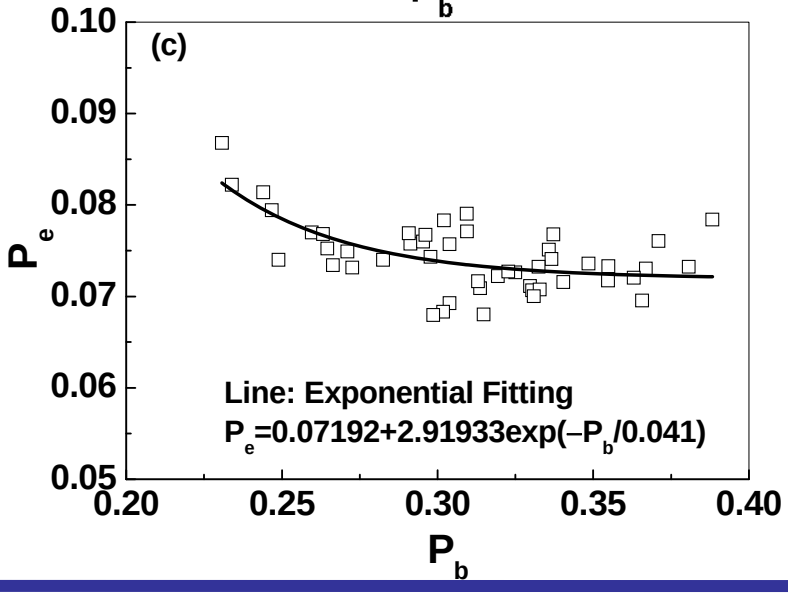

Correlations between Fitting parameters,

➢ VHDL-AMS Behavioural Model Development (Cont.)

Part I Main part

```
entity SRAM is
   port(terminal L,R:electrical);
end entity SRAM;
architecture Behavioural of SRAM is
  quantity Vin across L;
  quantity Vout across Iout through R;
  signal Vs1,Vs2:real:=0.0;
  signal Pa,Pb,Pc,Pd,Pe:real:=0.0;
begin
p0:process is
   variable s1 : positive;  variable s2 : positive;
   variable x1,x2 : real;              -- Uniform random variables
begin
UNIFORM(s1,s2,x1);  UNIFORM(s1,s2,x2);
Vs1<=sqrt(-2.0*log(x1))*cos(2.0*math_pi*x2);
                                    --Box-Muller Method
Vs2<=0.305+Vs1*0.021;
pa<=0.03756+0.12731*Vs2;
pb<=Vs2;
pc<=0.04571;
pd<=0.12182+1.24175*Vs2;
pe<=0.07192+2.91933*exp(-Vs2/0.041);
end process p0;

Vout==Pa+(0.5-0.5*Pa)/(1.0+exp((Vin-Pb)/Pc))+(0.5-
       0.5*Pa)/(1.0+exp((Vin-Pd)/Pe));
break on Pa; break on Pb; break on Pc;
break on Pd; break on Pe;
end architecture Behavioural;
```

Part II Input Voltage

```
entity Vinput is
generic(vhi,vlo:voltage;thi,tlo:real);
port(terminal L, R: electrical);
end entity Vinput;
architecture behaviour of Vinput is
quantity V across I through L;
signal pulse:voltage:=0.0;
begin
v==pulse'ramp(1.0E-9, 0.0);
pulse_proc: process
begin
pulse<=vlo; wait for tlo;
pulse<=vhi; wait for thi;
pulse<=vlo; wait for 0 ms;
end process;
end architecture behaviour;
```

Part III Testbench

```
entity test_sram is
end entity test_sram;
architecture test of test_sram is
terminal L,R: electrical;
alias ground is ELECTRICAL_REF;
begin
Vin0: entity Vinput generic map (1.0, 0.0, 1.0E-9, 0.0) port map
       (L, ground);
Sram0: entity SRAM port map (L,R);
end architecture;
```

➢ Model Verification by SPICE

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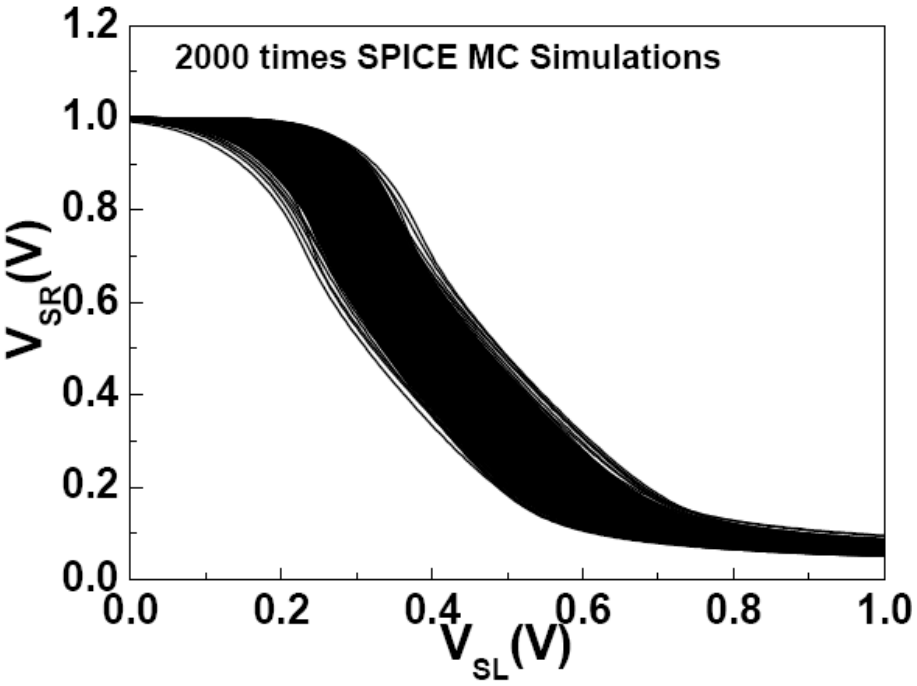

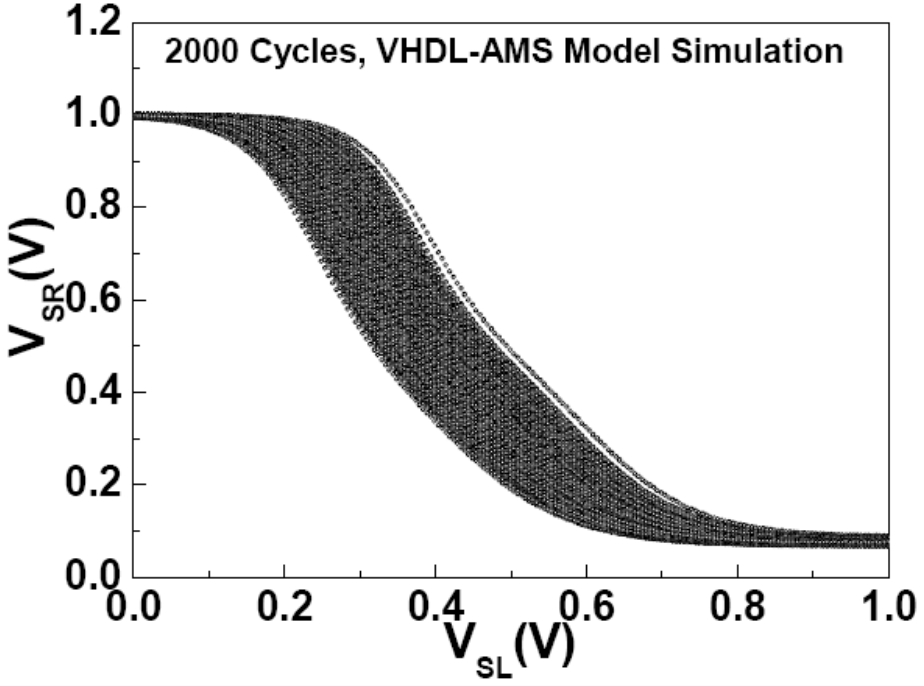

STCs Comparison between SPICE and VHDL-AMS Model

➢ Model Verification by SPICE (Cont.)

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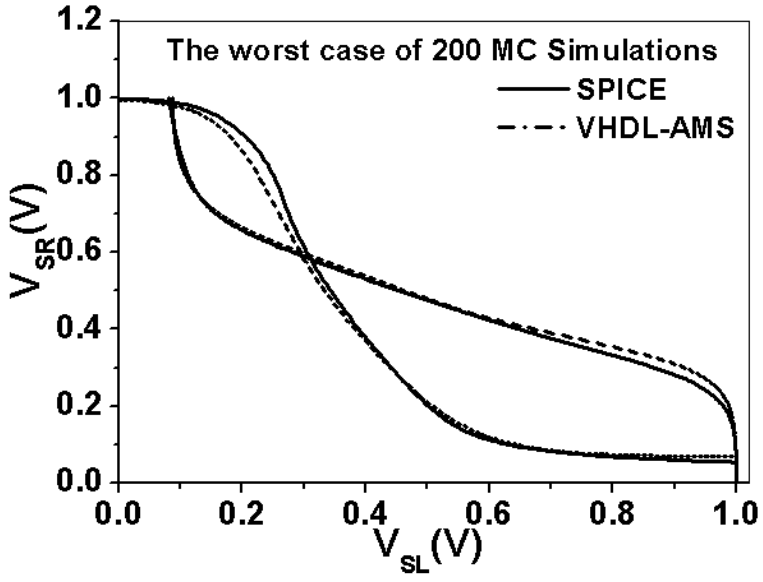
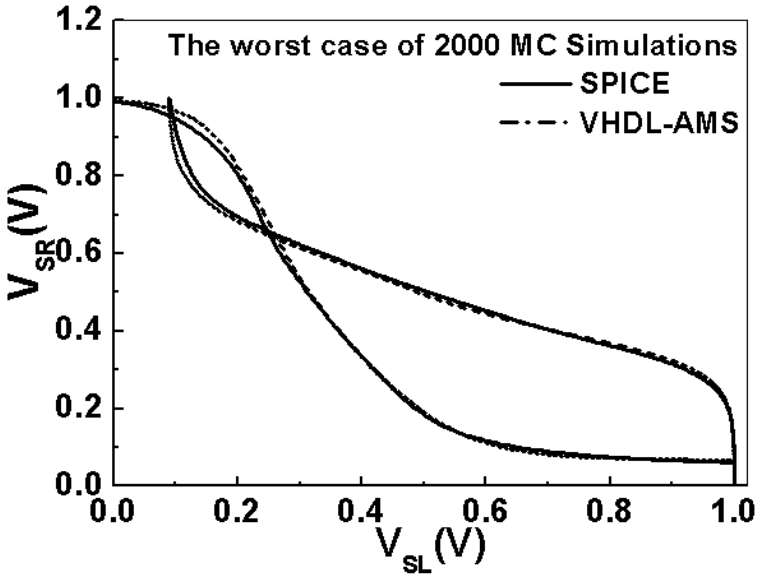
Worst cases of STCs Comparison between SPICE and Behavioural Model





Run times Comparison for SPICE and Behavioural Model

Simulation cycles	200	2000	20000
SPICE	7.3s	70.95s	893.93s
VHDL-AMS	2.0s	15.0s	145.0s
Ratios	**3.7**	**4.7**	**6.2**

➢ Conclusions

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- **Device variability is increasing with Dimensions scaling down,**

  Random discrete doping (**RDD**) is one of the main variability sources,
  RDD results in Vth, Ids variations,
  Stability of **35 nm CMOS SRAM** digital cells such as **SNM** is impacted by RDD.

- **VHDL-AMS Behavioural model is developed for SRAM subject to RDD,**

  STCs can be described by **two-level Sigmoidal** functions,
  Parameters are extracted to develop behavioural model,
  Behavioural Model is implemented by VHDL-AMS.

- **Model verification and Contribution of this work**

  The **accuracy** and **efficiency** are confirmed by comparing with SPICE simulation,
  One can get useful information of SRAM stability resulting from RDD by proposed Model without doing transistor-level simulation.

THANKS FOR YOUR ATTENTION !

Questions/Answers ?