

Powering Embedded CMOS Logic on MEMS-based Micro-Robots

Jung H. Cho
Lehigh University
jung.cho@lsi.com

Mark G. Arnold
Lehigh University
marnold@cse.lehigh.edu

Abstract

A hypothetical new digital-design paradigm called Field Programmable Robot Arrays (FPRAs) has been introduced in [1] which raises a number of problems that need to be solved for successful implementation. An FPRA combines CMOS reprogrammable logic with micro-robots having constrained motion and sensing capabilities. The goal of the FPRAs is to build digital-logic structures by physical motion as well as the electronic reconfiguration (commonly used in prior programmable logic). In this paper, we present the development of a circuit for powering the digital logic portion of FPRAs. We assume for physical motion the FPRA uses MEMS-based scratch drive actuator (SDA) micro-robots like those developed by Donald et al. [2] as a foundation to build other features needed to develop FPRA. We validate this by developing Verilog-A model of an electrostatic actuator and simulating in Cadence AMS (Analog Mixed Signal) environment.

1. Introduction

There has been much research to study and develop MEMS scratch drive actuators (SDAs). The application of this device is common in the fields of mirrors, optical gratings, variable capacitors, and accelerometers. By utilizing these extensive researches on electrostatic actuation, a new breed of untethered micro-robot has been introduced [3]. By using this approach we can now envision building a micro-robot which is capable of interacting with similar robots, self-reconfiguring and using multiple robot assembly to engage in larger tasks. Such microrobots will provide a research platform for self assembly of complex structures from simple robotic components in environments where external control is not feasible, such as in medical and space-based applications. The MEMS micro-robot built by Donald et al. [2] has a dimension of $60\mu\text{m}$ by $250\mu\text{m}$ by $10\mu\text{m}$.

Figure 1 shows the structure of this device. This device propels using scratch drive actuation [3]. The use of cantilevered steering arm was introduced to provide turning capability. The power is delivered externally through electrodes which can be multi-voltage level encoded to take advantage of hysteresis built into SDA to control forward and turning motions. Combining the SDA and digital logic on a single chip is a real challenge for the realization of FPRA. Our first step towards this long-term goal is to demonstrate the feasibility of a regulated power supply for the digital circuit on board an SDA. In section 2, we propose a solution which can be used to supply power to digital logic. This solution will be supported in our future research to demonstrate the fabrication process. CMOS-MEMS process integration is a key technology which needs to be further developed. The most widely used fabrication is a hybrid approach which is a modular assembly of CMOS and MEMS devices [9]. This brings consequence of low performance, cost of assembly and packaging cost. Monolithic integration is available and can be used to integrate SDA and digital circuits. One of the approaches recommended by Witvrouw [9] is to process the integrated circuit first and the micro-systems (SDA) last and typically on top of the circuitry. This approach will allow a sound integration plan to build the FPRA on silicon.

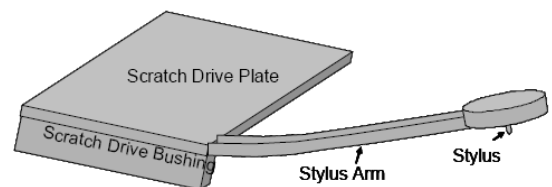


Figure 1: Illustration of MEMS Micro-robot

2. FPRA

A single FPRA consists of the following components: sensors, Scratch Drive Actuator (SDA) [2], drive

scheme, and logic arrays. In this paper, we focus on using the capacitive voltage stored when voltage is applied across the actuator and using this voltage to supply digital logic.

2.1 SDA mechanical and electrical model

To demonstrate power delivery to digital circuitry onboard MEMS microrobot, we start with developing Verilog-A model of SDA. It models the electrical and mechanical domains based on equations developed from input function of a parallel plate capacitor connected to a spring and a voltage source (Figure 2) [6]. The equation used in the model is a two port model which converts electrical energy domain to mechanical energy domain (Figure 3).

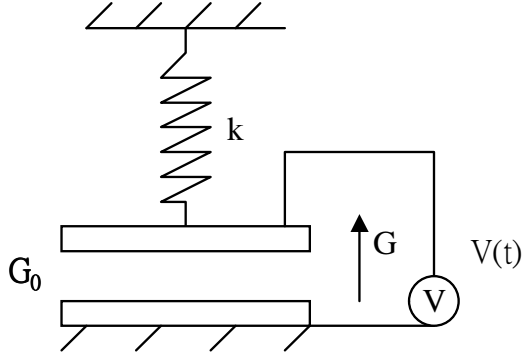


Figure 2: Electrostatic Actuator model; G_0 =Initial gap, k =spring constant [6], G =Gap change function, V =Voltage applied

The model of the parallel plate is based on basic equation

$$C = \frac{\epsilon_0 A}{G} \quad (1)$$

where A = area of the plate and G = gap distance. To capture the potential energy caused by electrostatic force using

$$E_p(q) = \int_0^q e dq \quad (2)$$

where e refers to voltage and q refers to charge. Since $Q = CV$ and $V = Q/C$, we can convert equation (2) to function of Q and G .

$$E_p(Q) = \int_0^Q \frac{Q}{C} dQ = \frac{Q^2}{2C} = \frac{Q^2 G}{2\epsilon_0 A} \quad (3)$$

Change in energy can be captured by

$$dE_p = \left. \frac{\partial E_p}{\partial G} \right|_Q dG + \left. \frac{\partial E_p}{\partial Q} \right|_G dQ \quad (4)$$

$$\text{where } \left. \frac{\partial E_p}{\partial G} \right|_Q = \frac{Q^2}{2\epsilon_0 A} \quad \text{and} \quad \left. \frac{\partial E_p}{\partial Q} \right|_G = \frac{QG}{\epsilon_0 A} \quad (5)$$

these equations. Then force and voltage can be written as

$$F = \left. \frac{\partial E_p}{\partial G} \right|_Q \quad (6)$$

$$V = \frac{Q}{C} = \left. \frac{\partial E_p}{\partial Q} \right|_G$$

After applying (6) into change in energy equation, it would be

$$dE_p = FdG + VdQ = \frac{Q^2}{2\epsilon_0 A} dG + \frac{QG}{\epsilon_0 A} dQ \quad (7)$$

Since Figure 2 is used as a model where voltage is used as input function for the plate capacitor therefore,

$$E_p^* = QV - E_p \quad (8)$$

$$dE_p^* = QdV + VdQ - (VdQ + FdG)$$

$$\Rightarrow dE_p^* = QdV - FdG$$

$$\therefore dE_p^* = \left. \frac{\partial E_p^*}{\partial V} \right|_G dV + \left. \frac{\partial E_p^*}{\partial G} \right|_V dG \quad (9)$$

$$\Rightarrow Q = \left. \frac{\partial E_p^*}{\partial V} \right|_G \quad F = - \left. \frac{\partial E_p^*}{\partial G} \right|_V$$

$$E_p^* = \int_0^V QdV = \int_0^V CVdV = \int_0^V \frac{\epsilon_0 A}{G} VdV = \frac{\epsilon_0 AV^2}{2G} \quad (10)$$

Then Q and F can be resolved by using (10).

$$Q = \frac{\partial E_p^*}{\partial V} \Big|_G = \frac{\epsilon_0 A}{G} V \quad (11)$$

$$F = -\frac{\partial E_p^*}{\partial G} \Big|_V = \frac{\epsilon_0 A V^2}{2G^2} \quad \left(= \frac{Q^2}{2\epsilon_0 A} \right) \quad (12)$$

Now these equations (11) and (12) can be used to quantify energy involved actuating and they are also applied to get displacement function of G. And this displacement is used along with input voltage to generate current through the plate capacitor. This is shown in Figure 4.

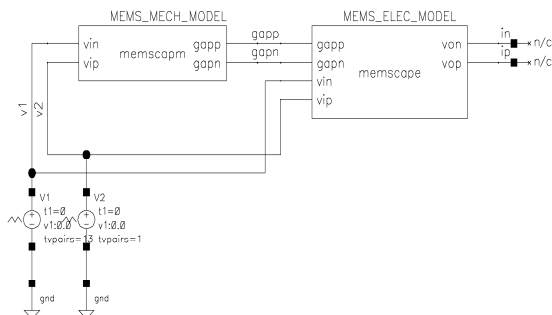


Figure 3: Verilog-A model block diagram of an electrostatic actuator

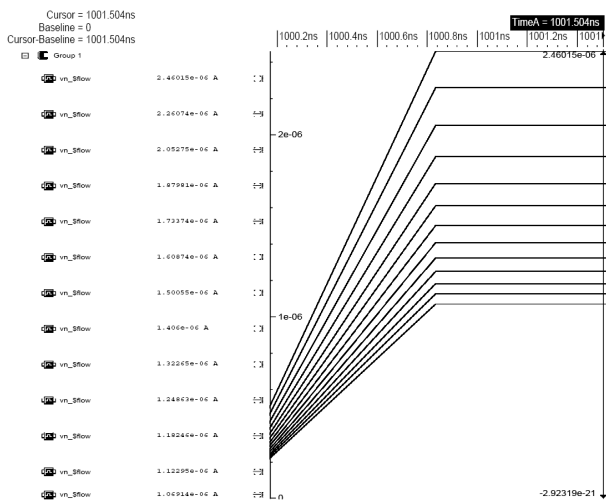


Figure 4: G (Gap) variation and capacitor current based on voltage applied

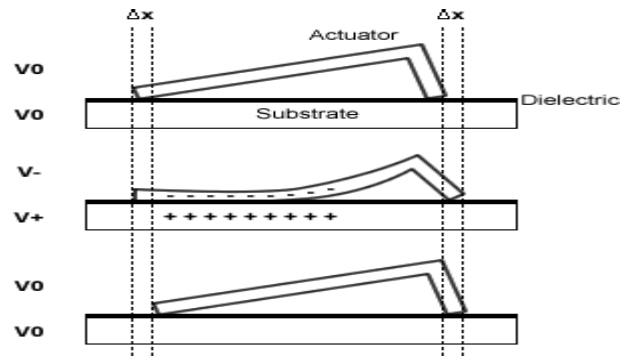


Figure 5: Illustration of electrostatic actuation [4]

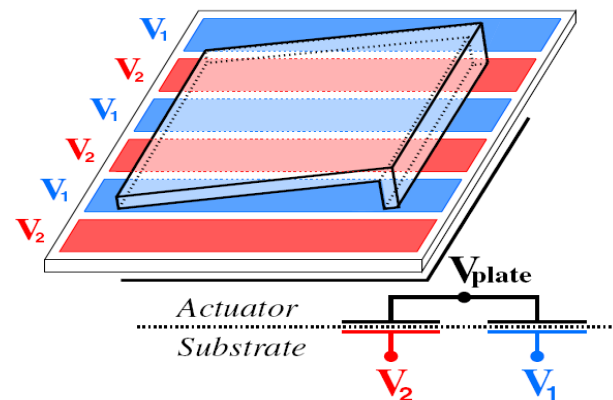


Figure 6: Illustration of power grid [3]

2.2 Drive power used to supply voltage to logic arrays

By powering onboard digital logic, this paper attempts to overcome the limitation in [2] of global control. The required logic to control a microrobot is a one-hot encoded state machine consisting of a dozen or so states. It would require around one hundred gates, clocked in the 1 Hz to 1 kHz range. At this level of simplicity and low frequency, the power requirements should be minimal. In the preferred embodiment, this logic would be programmable, which would require additional gates to support reconfiguration. The SDA's motion comes from electrostatic actuation shown in Figure 5. A voltage is applied between plate and substrate. This builds the charge between them causing plate to bend towards the substrate. The front of the plate is supported by the bushing as shown in Figure 1. The stored energy in the plate causes the edge of the bushing to move forward. When the voltage is released, the plate returns to original shape. This process repeats in order to propel SDA. Figure 6 shows the schematic of power grid or electrodes used by Donald et al. [2]. By using these

electrodes, SDA can operate more reliably due to the uniform coverage underneath. Therefore, the voltage on the plate can be simply equated by circuit analysis [3].

$$V_{plate} = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2} \quad (13)$$

We assume that we can fabricate actual transistor devices as part of SDA to incorporate digital logic. The power to these devices must be available in order to operate. Since there will be a stable $V_{platehi}$ available when V_1 or V_2 is applied, this voltage can be used to supply power to the device. However, the voltage range of SDA operation is very high so it cannot be used directly. This is a key concept which needs to be developed and further research is needed to support the CMOS-MEMS monolithic fabrication effort discussed in the introduction. In order to verify this conceptually, we have simulated this in Cadence AMS environment as shown in Figure 8. Figure 7 shows the equivalent circuit which illustrates the goal of this setup. This simulation environment allows co-simulation of Verilog-RTL / Verilog-A / Verilog structural netlist / transistors. This provides flexibility to work with mixed signal design where both digital and analog circuits need to be validated together [8].

First, we verified $V_{platehi}$ voltage as shown in Figure 9 where voltages to be the mean of V_1 and V_2 . Next, a more elaborate Verilog-A model was developed to include parallel plate modeling from section 2.1 and other parameters needed to model SDAs [5-6]. Since 40nm 1 Volt standard cell library was used for digital circuits, the voltage had to be lowered using a voltage regulator. A Verilog-A model of a voltage regulator was developed to meet this requirement. This voltage regulator accepts V_1 or V_2 as an input and uses $V_{platelo}$ as a reference for regulation. To test the functioning of the voltage regulator, we created a ring oscillator circuit in standard cell which can be simulated in Cadence AMS as transistor level circuits. A ring oscillator would be an essential circuit since it would be necessary to drive digital state machines onboard. To match the 1 Volt technology used in the ring oscillator circuit, the regulator was designed to provide a 1 Volt swing. The result of this V_{reg} can be observed in Figure 9 and 10. To verify that V_{reg} / V_{plate} can be used to supply power to transistor devices, a ring oscillator operation was demonstrated as in Figure 10. As long as there is a time when V_1 and V_2 are stable, the regulator can supply power and enable the digital logic to perform any

function needed.

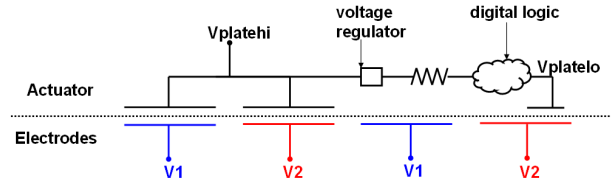


Figure 7: Equivalent circuit showing $V_{platehi}$ and $V_{platelo}$

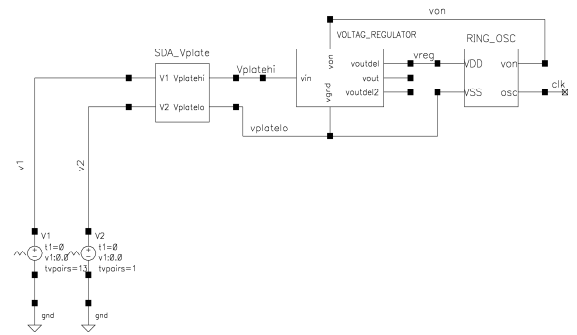


Figure 8: Full simulation setup

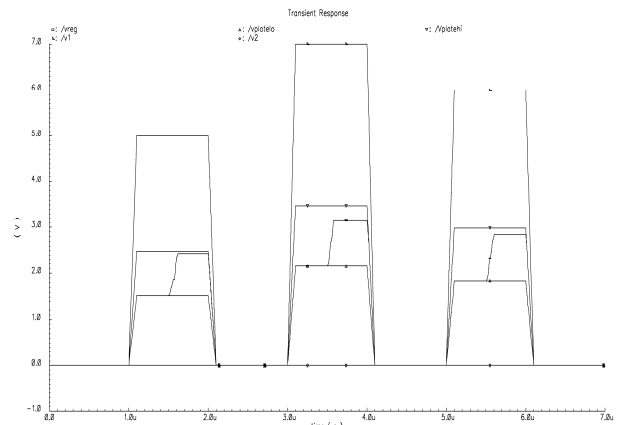


Figure 9: V_{plate} and V_{reg}

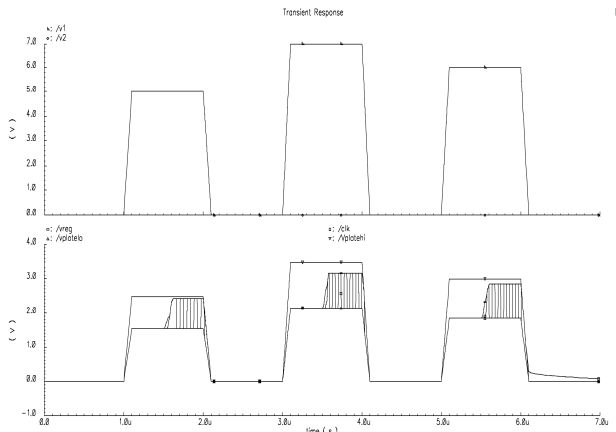


Figure 10: Ring Oscillator operation

3. Conclusions

We have proposed a power supply solution which can be the foundation for an FPRA. In order to function, the FPRA requires key features which need to be further developed. The major component is the SDA which has been well researched and demonstrated to be functional [2]. A novel approach to combining the SDA with real onboard circuits has been discussed. This approach uses the inherent voltage called V_{plate} to supply power to circuits. This way the SDA can continue to operate on the grid where it navigates and use its V_{plate} voltage to power the logic necessary to make the microrobot perform its functions.

4. References

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