Fast and Waveform Independent Characterization of Current Source Models

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ABSTRACT

A fast characterization method for current source models (CSM) is proposed. It analyses the given transistor netlist of CMOS logic cells to determine both static and dynamic CSM parameters in the same DC simulation. To account for the influence of parasitic elements in large logic cells, an additional low pass filter is inserted to the CSMs. AC analysis is employed to efficiently define its parameters. The characterization is therefore independent of user specified input waveforms. CSMs of industrial gates have been integrated into a standard SPICE simulator, showing high accuracy also for noisy input waveforms. Used in path based timing analysis of ISCAS85 circuits, average errors of 3% have been observed while simulation times could be reduced by a factor of 100.

1. INTRODUCTION

Reduced feature sizes and high integration density of contemporary digital integrated circuits result in long interconnects between logic gates. These pose new challenges to timing analysis [13]. Wire delays are introduced which can be of the same magnitude as gate delays. Furthermore, complex and nonlinear output loads are not well modeled by existing timing methodologies based on delay models dependent on input slew and output load. Moreover, the combination of strongly coupled nets and increasing operation frequency leads to severe crosstalk and might result in non-monotonic input signals [9, 15]. In these cases the gate delay can differ significantly from the pre-characterized value which employed a linear ramp model. This is illustrated in Fig. 1. Both input signals are identical except for a crosstalk attack at the end of the transition. The noise pulse in Fig. 1 causes a change of 13% on the delay and 10% on the slew. Such *noise-on-delay* effects can lead to significant signal integrity problems [13]. To guarantee accurate timing results and signal integrity, new simulation methods for digital designs are needed. They must provide a more detailed description of signals and more accurate timing models [8].

Analog circuit simulation is highly accurate but too costly when being applied to complex digital designs. This slowdown results from solving large equation systems originating from an electrical network of thousands of transistors. A remedy applied in FastSPICE simulators is to partition the circuit into smaller blocks and use transistor table models to circumvent costly evaluation of transistor equations. Current source models (CSM) are similar to these table models as they are pin compatible macro models. Consistent with

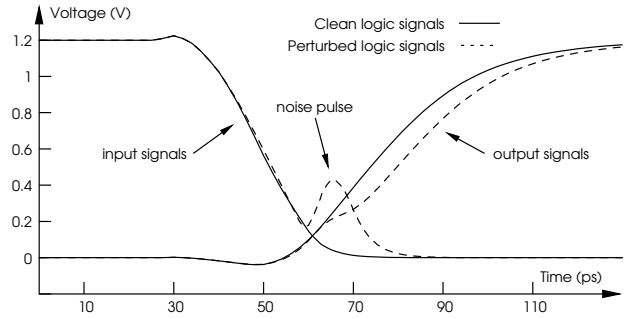


Figure 1: Influence of noise on slew and gate delay

modified nodal analysis (MNA), CSMs provide currents depending on port voltages and can be used as a substitute in SPICE-like simulators, including some tailored timing engines. In contrast to transistor table models, CSMs represent entire digital standard cells consisting of several transistors.

This paper presents a new current source modeling method that exploits structural information of the transistor netlist. Consequently, the fully automated model characterization does not rely on time consuming transient simulations, which are quite a burden for most existing approaches [2]. Instead, the main model parameters are efficiently determined through fast DC simulations. For very large cells an additional AC analysis might be needed. Hence, the characterization is independent of signal waveforms and output loads and the resulting CSMs are usable in various analysis types such as noise or timing.

Although library characterization is a one time effort, performance does matter. This is because many different models of the same logic cell are needed to account for different process corners and workload dependent aging behaviour.

The remainder of the paper is as follows. Sec. 2 gives an overview of existing CSMs. The new CSM and its simplified characterization process are explained in Sec. 3. Accuracy and simulation performance are investigated using an industrial 90nm library. The results are shown in Sec. 4. Concluding remarks are made in Sec. 5.

2. EXISTING CURRENT SOURCE MODELS

Current source models have emerged as alternatives to traditional standard cell timing models. They support arbitrary input waveforms and output loads since their model parameters are waveform and load independent. CSMs promise

close to SPICE accuracy combined with a higher simulation efficiency. Using a few basic circuit elements, the CSMs provide port currents that depend on port voltages. The voltage waveforms are calculated for a sequence of time points similar to analog transient simulation [14].
One of the first current source driver models was presented by Croix and Wong in [4]. It consists of a linear output capacitance and a nonlinear DC current source, $I(v_{in}, v_{out})$, controlled by the input and output voltage. The corresponding values are obtained from a two-dimensional lookup table (LUT). An empirical time shift has to be inserted for gates with large delays.
Extensions of this very first CSM have been published by Keller et al., who introduced a coupling capacitance to account for the Miller effect [9]. Chopra et al. further added an input capacitance for the receiver modeling [3]. Fatemi et al. extended the model in [3] by using nonlinear voltage controlled capacitances [6].
A different approach to model the dynamic behavior was presented by Li et al. [10]. For modeling the gate delay, two concatenated low pass filters are used as a pre-stage input. The filter output node is used to control the gate output capacitance and current source.
Amin et al. presented the most generic CSM [2]. It is also capable of handling multiple input switching. Every port is modeled by a controlled current source and a controlled charge, both being functions of all port voltages.
For these state-of-the-art approaches, the characterization of the dynamic components relies on time consuming transient simulations. To circumvent this, Kashyap et al. used capacitances between all ports instead of charges [7]. This allows the use of small signal analysis to determine the capacitance values by attaching biased AC voltage sources and measuring the resulting port currents. To improve accuracy, *important internal* nodes are additionally treated as *virtual* ports. They are either already known or empirically determined by transient simulation. Raja et al. circumvent this identification by only replacing the transistors with CSMs while preserving the gate internal topology [12].
While determining the static model parameters is quite simple, the challenge is in characterizing the dynamic elements, charges or capacitances, respectively. A pragmatic method is empirical waveform matching [4, 10]. A more elaborate approach applies a series of input waveforms for different bias conditions to determine voltage-dependent dynamic elements. Still, this method depends on the engineer's choice of input waveforms. A poor choice can lead to potentially inaccurate models. This holds also for the small signal method described in [7], where the amplitude and frequency of applied AC voltage signals have to be set appropriately.
In contrast to these methods, the presented approach allows the direct measurement of static and dynamic model parameters in the same DC analysis. This is enabled by analyzing the structure of a gate given by its transistor netlist.
The reduced feature sizes of integrated designs require more precise consideration of process parameter variability. Hence, also CSM elements have to be parameterized to account for parameter changes [6, 15]. This is usually done by linear sensitivities. In empirical characterization methods, it can be very expensive to derive these sensitivities. It requires the computations of finite differences since a direct measurement is not always possible. This means an additional full library characterization for every process parameter and is thus very costly. In contrast, in our proposed netlist-based method, the CSM model parameters are derived from circuit elements. Hence, their linear sensitivities can be obtained efficiently through adjoint network methods [11].

3. CSM MACROMODEL

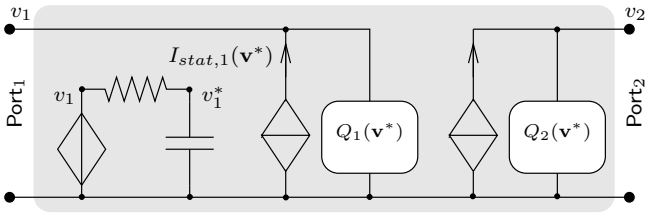


Figure 2: Proposed CSM for large cells

The proposed CSM of Fig. 2 is a pin compatible macromodel for standard cells of combinatorial logic gates. Ideally, the CSM predicts the same port current for any arbitrary sequence of port voltages as the transistor-based description. If this fulfilled sufficiently, the simpler CSM can replace the complex original subcircuit leading to faster SPICE simulations. Alternatively, it can be used in timing engines that also rely on the principles of MNA [1, 2, 12].
In the CSM, every port is modeled by a static current source, I_{stat}, and a charge element Q_{port}. They yield the total port current

$$I_{\text{port}} = f(\mathbf{v}, \dot{\mathbf{v}}), \text{ with} \qquad \dot{\mathbf{v}} = \frac{d}{dt}\mathbf{v} \tag{1}$$

$$I_{port} = I_{\text{stat}} + I_{\text{dyn}} = I_{\text{stat}}(\mathbf{v}) + \frac{d}{dt}Q_{\text{port}}(\mathbf{v}) \tag{2}$$

I_{stat} represents the DC port current for every combination of port voltages $\mathbf{v}$ whereas Q_{port} models the gate internal dynamics. It yields an additional current accounting for charging or discharging internal parasitic capacitances. Since $I(\mathbf{v})$ and $Q(\mathbf{v})$ are nonlinear functions, they are modeled as multidimensional look-up tables (LUT). We provide a CSM for every timing arc of a logic cell. Hence, with only one active input pin the table dimension can be limited to two, preserving efficient data handling.
In (2), port voltages $\mathbf{v}$ directly control the nonlinear elements. This requires that there is no differential dependency of cell internal node voltages on the port voltages. A change of port voltages has to immediately affect all internal nodes. However, in transistor level models of larger logic cells, resistors and capacitors are used to model the interconnect. These parasitic elements cause a signal delay between cell ports and transistor pins, mainly at the input. This effect has to be taken into account and is modeled by a first order low pass filter. To preserve the cell's receiver properties, the filter is attached to a duplicate of port voltage v_1. Its output node v_1^* represents the delayed signal at the transistor pins and is used to control the nonlinear I and Q in CSMs of large cells.

3.1 Characterization

During model characterization, the LUTs for $I_{\text{stat}}(\mathbf{v})$ and $Q_{\text{port}}(\mathbf{v})$ have to be obtained. In contrast to other methods, structural information of the gate is exploited to fulfill this task. In consequence, the characterization process for this CSM is extremely simple and requires only a single DC simulation for every combination of port voltages.

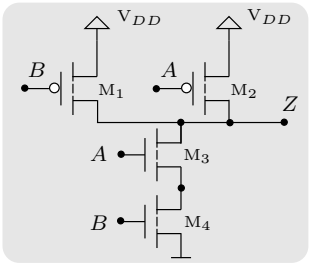


Figure 3: Idealized NAND gate

1. Identify connected transistor pins for all ports
2. Attach DC voltage sources to all ports
3. Perform nested DC sweeps of port voltages and measure transistor currents I_M and net charges Q_i
4. Add currents and charges to port quantities I_{port} and Q_{port}

Figure 4: CSM Characterization steps

The transistor netlist is analyzed to derive expressions for the static port currents. For every port, the connected transistor pins are identified. The sum of their static currents, i.e., source, drain, or gate leakage currents, equals the port current. For the example of Fig. 3, this current of output port Z is measured as

$$I_{\text{stat}} = I_{D,M_1} + I_{D,M_2} + I_{D,M_3} \tag{3}$$

Measuring the port charge Q is done in a very similar way. Again, structural information in the netlist is used to identify internal nets that are DC connected to the ports. The sum of every charge stored at these nets i equals the total port charge

$$Q_{\text{port}} = \sum_{\text{net } i} Q_i \tag{4}$$

For output Z in the example of Fig. 3, this port charge is

$$Q_{\text{port, z}} = Q_{D,M_1} + Q_{D,M_2} + Q_{D,M_3} \tag{5}$$

$Q_{D,M}$ are the charges stored at internal capacitances of transistor pins, drains in this case [5]. As these values can be obtained in a DC analysis, the measurements for static port current and port charge are combined. Hence, the characterization is simplified to the procedure given in Fig. 4. No user defined input signals are required, making this method immune against potentially inaccurate settings. Furthermore, since the characterization is not based on waveform matching, the resulting models are valid for any input waveform and can drive loads of any complexity.

3.2 Cells with extracted layout parasitics

Fig. 3 depicts an idealized case. Netlist descriptions of real cells usually include additional resistors and capacitors to model the cell internal interconnects. This parasitic network is outlined in Fig. 5, depicting the netlist of a CMOS inverter that was extracted from layout.

The new elements require a modification of the characterization. To start with, the topology of the interconnects has to be incorporated into the netlist analysis. We observed that the resistors form undirected trees connecting the ports with

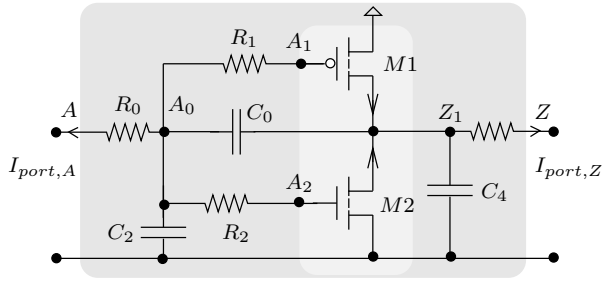


Figure 5: CMOS inverter with interconnect parasitics

the transistors. This holds for all logic cells of the industrial library that was used. For the example of Fig. 5, this tree (R_0, R_1, R_2) is replotted in Fig. 6.

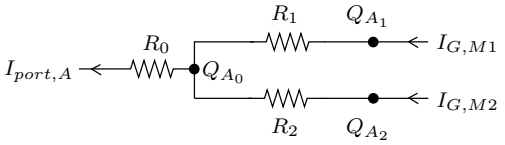


Figure 6: Resistive tree for input port A of Fig. 5

The charges stored at every tree node have to be considered in (4). For the leaf nodes, these are the charges located at the MOS structures, just as in the idealized case. Additionally, and for all other tree nodes k, charges are stored on the linear capacitors C_i, given by

$$Q_{C_i,k} = C_i \cdot (V_k - V_j) \tag{6}$$

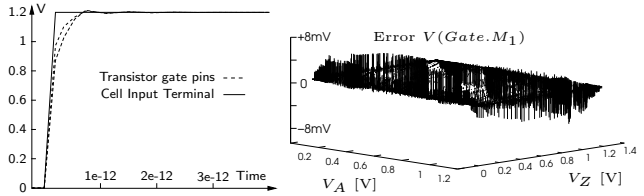
The connected node potentials V_k and V_j are known from the DC simulation and so are the capacitor values from the netlist. Hence, the values of additional charges at node k are easily measurable. For illustration, the resulting dynamic input current of Fig. 5 is

$$I_{\text{dyn}} = \frac{d}{dt}\left[(Q_{C_0,A_0} + Q_{C_2,A_0}) + (Q_{G,M_1}) + (Q_{G,M_2})\right] \tag{7}$$

For the static current no modification is needed. Due to the tree structure of the parasitic resistors, all cell internal currents are drained to the ports. However, this tree is no necessity. For arbitrary topologies, symbolic circuit analysis yields expressions for the port currents.

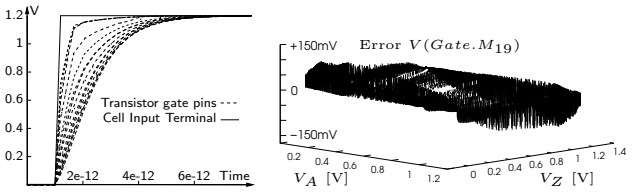
The parasitic network, nonetheless, introduces a fundamental problem. In (2), the gate currents are functions of port voltages and their first order derivatives only. Hence, all gate internal node potentials and therefore also currents must be expressible as an algebraic formula. In this case, the DC solution for node potentials during characterization and the solution during transient analysis will be identical. While this can be satisfied sufficiently well for cases with no dynamic elements, it is obviously violated for real gates. Gate internal node potentials exhibit a dynamic behavior which is expressed by a differential-algebraic dependency on port voltages.

Figures 7(a) and 8(a) visualize this problem. A step signal has been applied to the input of a small inverter (2T) and a large one (20T). The resulting voltage waveforms for all transistor gate pins have been plotted. In the case of the 2T-inverter, the resistive part of the network dominates



(a) Step Response (b) Error Plot

Figure 7: Step responses for transistor gate pins and error in gate voltage for M_1 of 2T-inverter



(a) Step Response (b) Error Plot

Figure 8: Step responses for transistor gate pins and error in gate voltage for M_{19} of 20T-inverter

and the differential dependency can be neglected. Modeling the output current as a function of the present port voltages will be a good approximation of the circuit behavior. Fig. 7(b) shows the voltage difference of a transistor gate pin in transient and DC analysis. This plot validates the algebraic assumption, since the error is less than 8mV.
In contrast, using more transistors to increase driver strength, the resulting interconnect of the 20T-inverter becomes impeding. Consequently, the plot in Fig. 8(b) shows errors of up to 150mV. The deviation in control voltages leads to wrong output currents and hence model inaccuracy. The root cause is shown in Fig. 8(a), where a noticeable signal delay between cell input and transistor gate pins is observed. Since the latter define the actual currents and charges, the differential dependency has to be incorporated into the CSM. From Fig. 8(a) it can be inferred, that first order low pass filters at the receiver ports (see Fig. 2) are reasonable means. Their delayed output nodes are used to control the nonlinear charges and current sources.

For different combinations $\mathbf{v}$:
1. Excite AC signal at port
2. Measure AC signal at all DC connected transistor pins
3. Determine corner frequencies

Build average f_{3dB}

Figure 9: Determination of filter parameters

The filter parameters are determined very efficiently through small signal analysis according to Fig. 9. An AC voltage source is attached to the input port and its frequency is swept to measure the 3dB-cutoff-frequencies at all transistor gate pins. Thereafter, the average value is calculated. This measurement is performed for different combinations of input and output voltage to account for the bias dependency of transistor pin charges. Due to the dominating linear parasitic elements, the variation of f_{3dB} was observed to be less than 10%. Hence, neglecting this dependency will cause only a minor error. Using the average value, f_{3dB}, and a fixed linear capacitor value yields the resistor value through

$$f_{3dB} = \frac{1}{2\pi RC}, \qquad R = \frac{1}{2\pi \cdot f_{3dB} \cdot C} \tag{8}$$

The capacitor value can be chosen freely but affects the timestep control. To avoid an increasing number of timesteps, the value should be in the order of expected values in the interconnect models.

3.3 Multi-stage gates

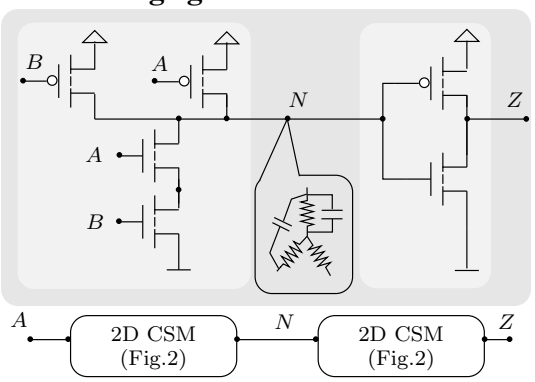


Figure 10: AND-gate modeled by two CSM stages

Special attention must be paid to multi-stage gates consisting of concatenated channel connected blocks. Here, some internal nodes suffer from a strong dynamic dependence, violating the assumption of algebraic relations to the port voltages. The authors of [7] suggested modeling these nodes as additional *virtual* gate ports in order to restore algebraic port dependency. This increases the dimension of the LUTs and requires additional elements to model the virtual ports. We use an alternative method which divides the gate into single stages. Based on the netlist, channel connected blocks are identified using a simple structure recognition algorithm. This systematic approach automatically locates cell internal nodes between CMOS blocks that have to be modeled. Hence, also for complex multi-stage gates no user interaction is needed. The autonomous structure-based characterization method is applicable to a wide range of gate types.
For illustration, Fig. 10 depicts an AND gate with a symbolized parasitic network. The algorithm identifies node N to partition the gate into a NAND gate followed by an inverter. Since there is no direct relation between primary input and output nodes, the two stages are characterized and modeled individually resulting in two concatenated CSMs. Characterization times and data amount are thus kept low. Compared to modeling virtual ports, no unnecessary redundancy is introduced. The equations for net current and charge at this internal split node are derived as described in Sec. 3.2, just as for the cell ports. Subsequently, the individual terms are assigned to the corresponding stages (AND or inverter), based on their controlling voltages.

3.4 Implementation

The proposed CSMs can be implemented into all simulators that apply MNA principles. We used an interface for compiled models to integrate the CSMs as behavioral models in a standard SPICE simulator. Hence, mature techniques for integration methods, timestep control, convergence aids,

and sparse matrix solving are already available and do not have to be reimplemented. It also allows to evaluate model accuracy independent of other error sources. Furthermore, highly accurate mixed simulation of CSM and original transistor description can be performed. Circuit elements for I and Q apply bilinear interpolation on ASCII LUT files.

4. RESULTS

Standard cells of an industrial 90nm CMOS library have been characterized and analyzed for accuracy. The gates range from one to eight input pins and are inverting as well as non-inverting. The characterization was performed completely autonomous and did not require any user interaction. Examples of characterization times for different logic gates using the structure-based approach are given in Table 1. The gates of different sizes are described by their number of inputs, transistors, and passive elements forming the parasitic network. For all cell types, very small characterization times of several seconds or a few minutes are needed. Compared to model characterization based on transient simulation (TRAN) [2], the new method is typically 60 times faster. Nonetheless, the characterization time for the buffer increases considerably, as this cell consists of 22 stages which have to be characterized. The time needed for one stage therefore remains about 80 seconds.

Cell	Inputs	FETs	Parasitics	Runtime	
				CSM	TRAN
2T Inv.	1	2	33	14s	4m 27s
12T Inv.	1	12	136	20s	13m 28s
Buffer	1	60	859	940s	1h 30m
Nand	2	32	482	56s	1h 11m
And	2	24	326	1m 12s	1h 03m
And-Or	8	68	1091	7m 51s	8h 35m

Table 1: Characterization runtimes for our structure-based CSM (CSM) and transient simulation-based CSM (TRAN) [2]

The models have been implemented in a standard circuit simulator and compared against transistor level simulation in accuracy and speed. All cells have been tested using an industrial setup with different combinations of input slew and pi-structure output load.

Tables 2 and 3 provide an overview on delay and slew error distributions for the driver model of different cell types. For all cells, good accuracy has been observed for the majority of test runs. In more than 98% of all test cases, delay and slew errors did not exceed 10%. Nonetheless, there are still cases with large maximal errors. These large errors could have two possible reasons: We observed that there are test cases for which delay or slew are very small, sometimes almost zero. This leads to a large relative delay error although the waveforms are practically identical with almost no absolute error. Despite this spurious result, there are logic cells for which the used CSM model may not suffice for the required accuracy. This holds mostly for cells with long transistor stacks. More sophisticated CSM structures are required to cope with this problem.

Figure 11 shows the relative delay and slew errors for the receiver tests. Again, very good accuracy is observed. In 99% of the test cases, errors of less than 10% are observed.

While accuracy is the necessary condition, reducing simulation time is the objective of this approach. Table 4 provides an overview of the achieved simulation time savings. In total, an average performance gain of 40x is observed. The speedup factor for individual cells ranges from 4 to 150 and is based on two effects. First, the interpolation of values from the LUTs requires significantly less time than evaluating the BSIM4 equations. This effect becomes more significant with increasing number of transistors in a cell. The second contribution to the speedup is a reduced number of time points during transient analysis. This results from the use of a single charge in the CSM as compared to many small capacitances in the transistor netlist, which allows the use of larger timesteps [14].

Referring to Section 1, one important request in digital circuit analysis is the correct handling of non-monotonic waveforms. Since noisy signals have severe impact on delay and signal integrity, the CSMs were also tested for this capability. Figure 12 shows an input signal with noise pulses and the output waveforms of two concatenated NAND cells. The results of SPICE simulation with transistor-based gate models (BSIM) and the CSM match almost perfectly, validating both receiver and driver model. In Fig. 13, the new CSM and the model according to [2] of a complex cell have been compared against BSIM. Especially at the transition tails and the noise bump higher accuracy is achieved by the proposed new model.

To demonstrate the strength in both accuracy and perfor-

Error (%)	5%-	50%-	95%-	maximal
	percentile			error
Inverters	-3.68	0.11	1.42	-11.36
Buffers	-0.71	2.76	9.97	10.61
Nands/Nors	-1.64	3.65	6.75	7.54
Ands/Ors	-8.25	1.40	6.67	-11.98
Complex	-7.47	2.09	8.73	11.96

Table 2: Delay errors of driver models

Error (%)	5%-	50%-	95%-	maximal
	percentile			error
Inverters	0.64	1.47	3.04	4.73
Buffers	0.98	2.91	7.17	7.40
Nands/Nors	-0.51	0.32	7.02	9.44
Ands/Ors	-0.81	1.93	6.40	9.61
Complex	-3.49	1.29	8.16	11.91

Table 3: Slew errors of driver models

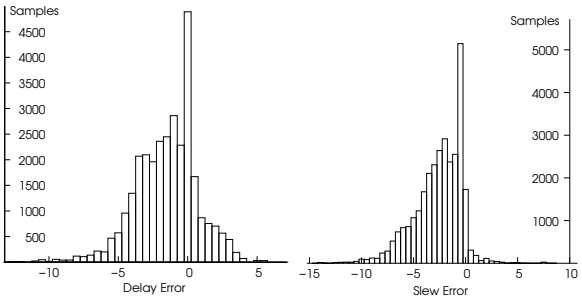


Figure 11: Delay and slew error of receiver models

2T-Inv.	12T-Inv.	Buf	Nand	And	And-Or
4x	24x	17x	81x	40x	137x

Table 4: Speedup over transistor level simulation

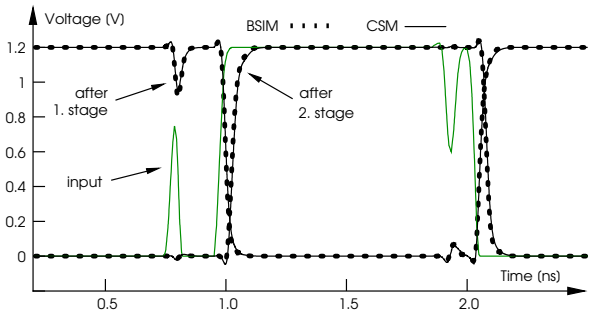


Figure 12: Noisy input signal for concatenated NANDs

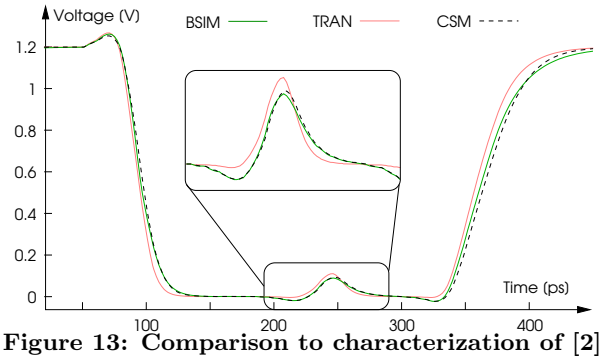


Figure 13: Comparison to characterization of [2]

mance, critical paths of different ISCAS 85 circuits have been simulated. Table 5 provides the comparison of CSM and transistor level simulation in SPICE. Since the same simulator is used in both cases, the relative delay errors of 1.8% to 4.6% stem only from the CSMs. Speedup factors of 46 to 107 have been achieved, meaning a reduction in simulation time for the critical path of circuit c6288 from 16 minutes to 9 seconds. Still higher speedup factors could be achieved by using specially tailored simulation engines, as proposed in [7, 10].

Circuit	c1908	c5315	c6288	c7552
Gates	42	49	123	42
Err. delay [%]	1.8	2.2	4.6	2.3
Err. slew [%]	1.1	5.1	2.7	6.6
Speedup	70	46	107	52

Table 5: Summary of speedup factors and errors

5. CONCLUSION

This work describes a new characterization method for current source models of logic cells. Considering the gate structure allows to determine static and dynamic model parameters by using DC analysis only. Greater model accuracy for large cells is achieved by a low pass filter, which is efficiently characterized through AC analysis. Avoiding the transient simulation of input waveforms results in a 60 times faster characterization. The model is integrated into a standard SPICE simulator, making it applicable to various analysis types, but can also be used in any simulation engine relying on MNA. Timing analysis of various ISCAS85 circuits show average errors of 3% for delay and slew while reducing the simulation times by factors of up to 100. Current work includes the automated computation of linear sensitivities with respect to process parameters to utilize the CSMs for statistical timing analysis. Because model parameters are directly related to circuit elements, efficient adjoint network methods can be used instead of expensive finite differences. For further increases in accuracy, different model refinements are being developed.

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