BER and Power Consumption Estimation Based on Hierarchical Modeling of a 2.4 GHz Power Amplifier

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ABSTRACT

This paper presents a power consumption estimation methodology for wireless devices, consisting on hierarchical modeling of specific AMS-RF IP (Intellectual Properties). It provides accurate energy consumption models for specific devices, based on simulations and/or analytical expressions extraction. Thus, within a unified simulation environment, full system's characteristics such as BER (bit-error rate), PER (packet-error rate) and DC power consumption can be evaluated in terms of block specifications (in this case, the RF power amplifier). It can be seen that the platform provides realistic accuracy with minimal electrical information, while maintaining acceptable simulation times. Also, the co-simulation advantages and drawbacks of coupling these power consumption models with network analysis are discussed.

Keywords

RF, system design, AMS IP, power amplifier, SystemC, hierarchical library, BER, power estimation.

1. INTRODUCTION

Shrinking integration feature sizes, as well as the advances of nonstandard fabrication processes, have rapidly led the microelectronics industry to a tremendous density increase in terms of circuit functionalities. As the market keeps pushing for higher performances under lower production costs, physical limits are reached and bigger modeling and conception efforts are demanded. Nowadays, commercial SoC (System-on-Chip) include several processing units, memories, transceivers, as well as heterogeneous units, which also complicate the verification task, imposing modifications in the traditional development flow.

Power consumption then rises as a major concern whereas developing such dense integrated systems, due to market need for low-cost autonomous and less-consuming devices. Applications having low-maintenance cycles and consequently longer battery lifetime, such as WSN (Wireless Sensor Networks), have been widely proposed. Increased functionality and full integration of such systems is expected as a next step, but there is still a lack of solutions for its complete simulation and verification.

The different electrical sections of a SoC device, mainly the digital, analog and RF units, present different signal processing characteristics and are often designed by different teams using isolated CAD solutions (cf. Figure 1). Although the digital development flow is relatively well structured, presenting high-level models that are quite independent of electrical block's specifications, such flows are not available for analog and RF sections. These are tied to a defined electrical architecture, preventing the use of generic high-level models if an electrically coherent accuracy must be achieved.

The proposed methodology for system-level simulation consists on using high-level analog and RF models, based on the Mentor Graphics Commlib_RF models library [1], including an internal energy consumption model. The DC power consumption formulas link the DC supply voltage values with the internal behavior of the circuit, accordingly to the characterization results, and, in the other way, impact the circuit specifications depending on the input values.

Since the new models are of greater complexity when compared to simple high-level models, this technique may be negative in terms of simulation time. Limiting the refinement of the energy consumption (efficiency), to the most important block(s) can be enough to evaluate some aspects of the complete system - like BER and power consumption - whilst adding minimal simulation overhead.

In the case of our application, the transceiver's energy efficiency was evaluated, leading to an analysis of its most energy-consuming components. The power amplifier block was then chosen for the bottom-up refinement, since its power consumption is frequently predominant over all units of the emitter. Also, as some of its characteristics can be electrically controlled, through gain regulation mechanisms, it would be interesting to verify how these functioning modes affect power consumption and system performance.

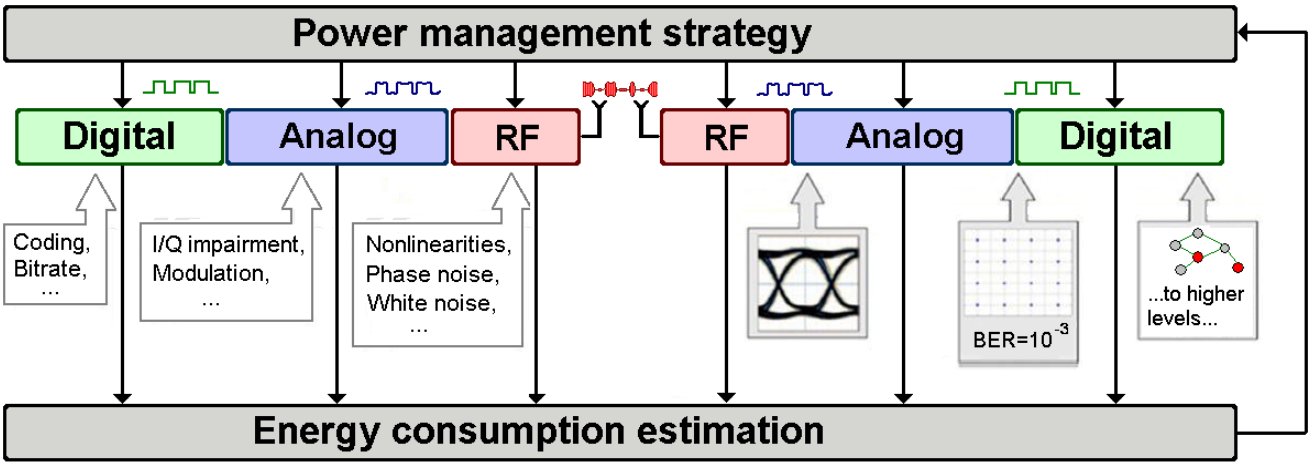

Figure 1 - Full system view, comprising digital, analog and RF sections, as well as power supply management.

In the next section, we briefly present the developed system, the model-based system specifications extraction and the retained transceiver topology. Section 3 shows the power amplifier topology choice and optimization, followed by the details about the methods for its hierarchical modeling both analytically and by simulation, as well as models comparisons. Finally, we present the conclusions and on-going works concerning the inclusion of such models in network analysis tools.

2. SYSTEM OVERVIEW

The case study presented is conforming to Bluetooth Low Energy (BT-LE) [2], a low-power wireless standard designed for ultra-low power consumption, initially known by the names of Wibree (2006), and later BT ULP (Ultra Low Power). It consists on a complementary technology to widely-known Bluetooth standard, targeting applications requiring transmissions of smaller quantities of data at very low latencies to other devices.

Concerning radio specifications, BT-LE transmissions are modulated with GMSK, in the ISM 2.402-2.48GHz band. The number of channels is reduced compared to BT, doubling channel spacing from 1MHz in classic BT devices, to 2MHz in BT-LE. Added to the simplification of the frequency hopping mechanism and the lower output power levels (in the range of -10 to +10dBm), it allows BT-LE to obtain power savings in the order of 15-20 times, when compared to classic Bluetooth [3].

2.1 System partitioning

A SystemC virtual prototype of the BT-LE protocol was created [4] in order to provide an executable specification of the upper layers of standard and for further data communication with analog and RF units (cf. Figure 2). Initially, the channel interface between the instantiated devices was coded as arrays of received data, in which the imperfections are modeled as statistically-induced faults. The SNR information can be input as a function of the device's conditions and distance between nodes.

For the AMS and RF circuits, a first model using Simulink Communications Library and AdvanceMS Model Extractor [5] was proposed, allowing a first evaluation of the system specifications, taken the effects of modulation and channel imperfections [6].

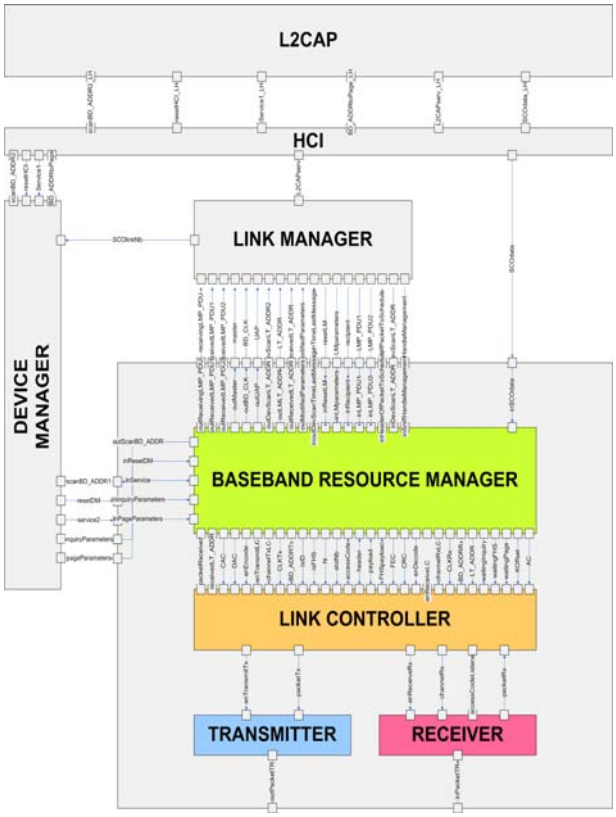

Figure 2 – SystemC model of the BT device module.

2.2 Emitter architecture

In order to comply with extracted system specifications, to reduce the global power consumption and also for matters of simplicity, we adopted a direct up-conversion emitter, as shown in Figure 3. Digital signal is passed through the Gaussian filter and then modulates the VCO frequency, which deviates up or down from the channel's central hopping frequency. The GMSK modulated signal is then amplified to the desired output level (via the gain control).

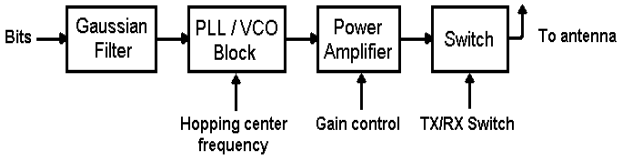

Figure 3 - High-level model of the chosen emitter topology.

Power amplifier's nominal input signal power is fixed around -10 dBm, requiring a power gain dynamic from 0 to +20 dB, in order to provide the BT-LE output power to the antenna. All blocks are considered as being 50Ω impedance matched, both at input and output.

3. POWER AMPLIFIER

The top-down power amplifier behavioral model is based on Mentor Graphics Commlib-RF models. The memory-less model takes into account the signal amplification and compression, real input and output impedances matching, the third order intermodulation and the frequency response, as depicted in Figure 4. Power consumption information can be include to obtain high-level compatibility, however it is necessary to relate block specification to energy consumption value.

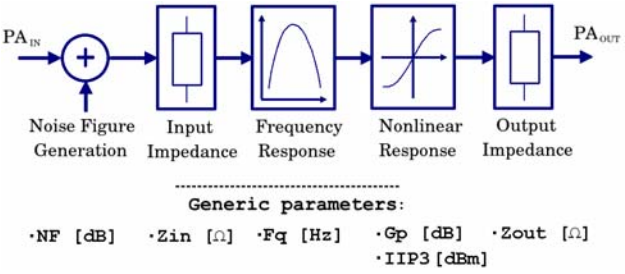

Figure 4 - Power amplifier behavioral model. The block's specifications are taken as generic parameters.

3.1 Design

A Class-E topology was then chosen for the RF power amplifier, due to its theoretical 100% energy efficiency [7], coupled to a pre-amplifier driver at the input of the switching-mode transistor (cf. Figure 5). Finally, after proper sizing of driver and power transistors [7], we can tighten specifications in order to attain design requirements with minimal power consumption.

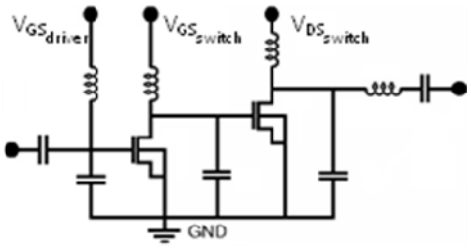

Figure 5 - Class-E power amplifier topology.

SPICE electrical model specifications can then be extracted by simulation, e.g. in terms of power gain and energy consumption (cf. Figure 6) and S-parameters (cf. Figure 7). Under nominal conditions (Vgs_{driver}=0.5V, Vgs_{switch}=0.57V and Vds_{switch}=1.0V), power gain (20.8dB), IIP3 (-4.0dBm with P_{in}=-20dBm), -1 dB compression-point (-14.3dBm of input power) and input/output impedances were characterized for a large range of components values as well as for different DC tension supplies.

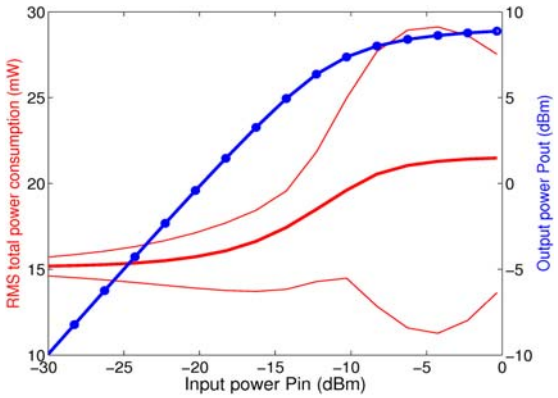

Figure 6 – Output power (dotted) and power consumption (minimal, maximal and RMS) under nominal conditions.

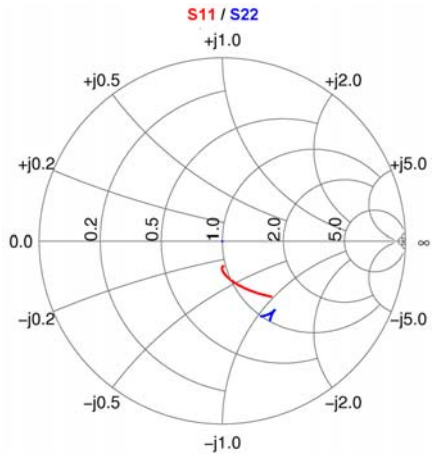

Figure 7 – S11/S22 (red/blue) extracted values within the BT-LE frequency range (2.402-2.48 GHz band).

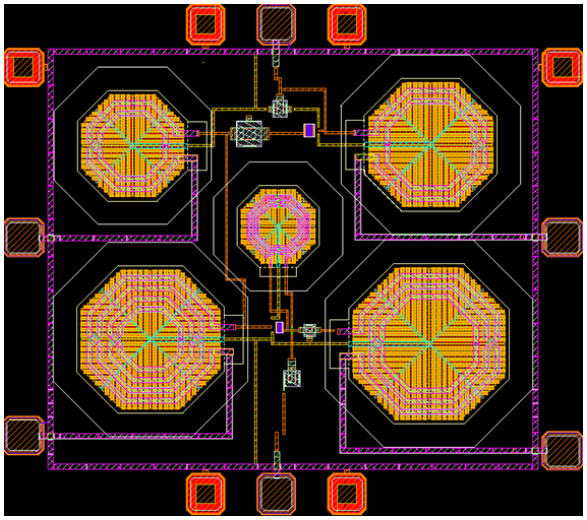

Figure 8 – Physical layout of the final circuit designed using ST 130-nm RF CMOS technology.

Post-layout simulations and physical layout refinements are under away. A first view of the proposed circuit is presented in Figure 8. Measurements results will be soon available.

3.2 Model refinement

The behavioral model of the power amplifier was then refined with the introduction of an intrinsic expression for the power consumption. The choice of an internal consumption model was made due to the fact that external DC supplies would have an impact on the block's behavior (i.e. transistor bias). DC power supplies ports were added and block's specifications generic parameters were replaced by coefficients of the fitting functions relating power supplies voltages and the PA's internal functioning, as depicted in Figure 9.

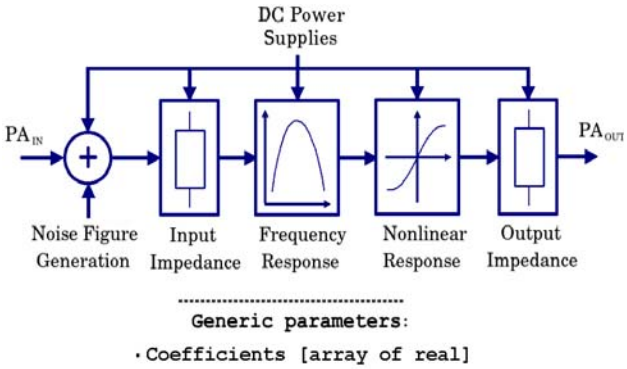

Figure 9 - Refined PA model, including power supplies pins.

Firstly, these coefficients were extracted from simulation results, with the exhaustive characterization of the circuit's SPICE model as a function of its DC supplies. Results were then analyzed and fitted to different types of functions (cf. Figure 10), providing expressions as accurate compared to simulations, as the complexity of the chosen fit function increases. Naturally, the choice of an optimal function will have a negative effect in the model's complexity, increasing the number of generic parameters and consequently its simulation overhead.

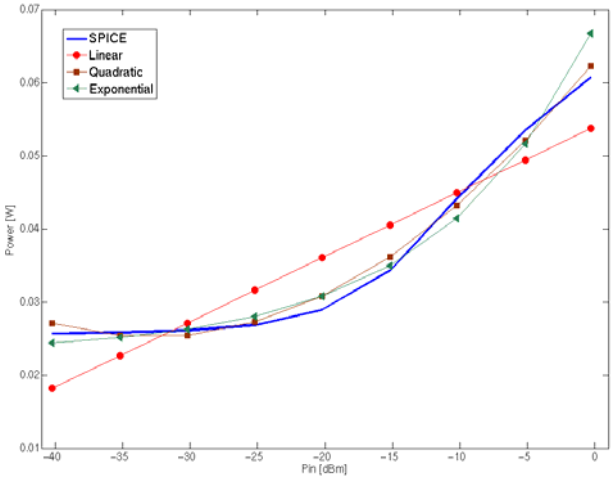

Figure 10 - Results comparison, using nominal voltage supplies.

The figure 10 shows the fitted functions for the total power consumed by the power amplifier, as a function of the input signal power:

- exponential: $0.0231 + 0.0448*e^{Pin/11.4507}$
- quadratic: $3.5e\text{-}05*Pin^2 + 0.0023*Pin + 0.063$
- linear: $8.9e\text{-}4*Pin + 0.054$

A second approach is proposed, based on an analytical extraction of the circuit's behavior. Ideal models for every component of the schematic were used and both linear and non-linear behavior expressions were calculated, taking transistors modes into account. Simulated values and circuit conditions were then included to the expressions, in order to fit analytical expressions to the simulations.

3.3 System's BER and power estimation

With the introduction of the power consumption model, it becomes possible to perform power consumption estimation for the individual block during system-level simulations, with acceptable simulation times. Also, within the proposed development environment, exported Simulink models can be simulated together with SystemC and VHDL-AMS blocks, as well as SPICE circuits.

Extrapolating initial BER (and even PER) results and neglecting the emitter noise figure (compared to noise added by the receiver and the channel), one can relate the PA's energy consumption to the bit-error-rate, as depicted in Figure 11.

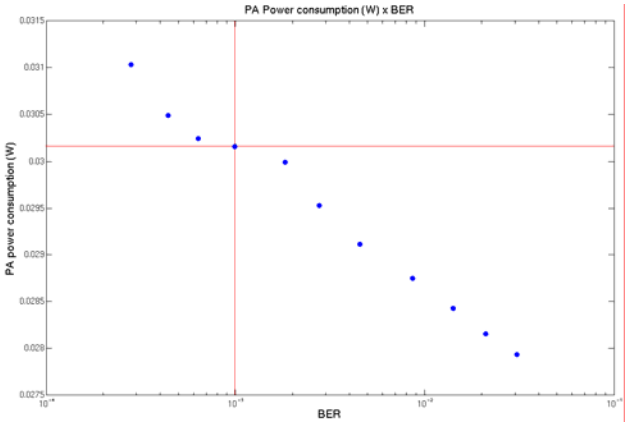

Figure 11 - BER variation extrapolated in function of power amplifier's power consumption.

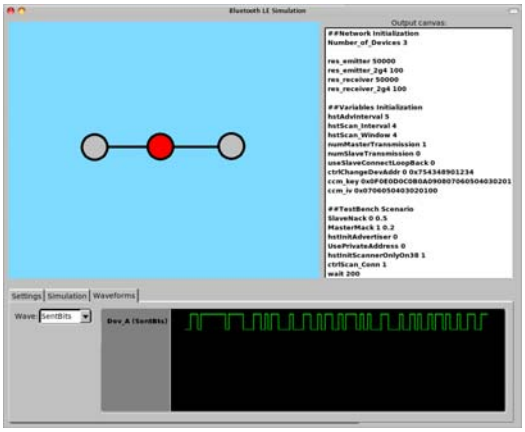

Figure 12 - Network analysis tool GUI including power consumption models.

4. CONCLUSION AND TRENDS

We propose the use of high-level power consumption models refined for most relevant blocks, while performing system-level simulations. It can be shown that simulation overhead is minimal when compared to high-level standard consumption models, yet maintaining results accuracy closer to electrical extracted information. Considering electrical power consumption of the power amplifier, related to its output power, for bit- or packet-error-rate simulations brings a much more realistic view of system's performance.

The power amplifier's gain control must be adapted to correctly adjust signal's output power, in order to effectively increase correctness on data transmission. The nonlinear relation depicted in Figure 11 proposes that robustness of the system will not be directly improved with linear increase of signal power, as can be initially supposed. However, for a better analysis of the link between two devices, a simplified energy consumption model of the reception blocks should be developed.

Finally, to estimate energy consumption in a network environment, these models were rewritten using SystemC-AMS language and included in a network analysis tool (cf. Figure 12).

The tool presents a user-friendly interface to evaluate different network topologies within environmentally-aware scenarios. It allows the full integration of the extracted electrical information, modeled as current signals, and the high-level system models and protocol. On-going projects are dealing with the inclusion of battery models for each network device, as well as different approaches for the AMS blocks' modeling, in order to deal with the current high simulation times (e.g. baseband modeling and co-simulation).

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