VHDL Based Simulation of a Sigma-Delta A/D Converter

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Abstract

The VHDL based mixed-signal event-driven (MixED) simulation method is employed to simulate a sigma-delta modulator for A/D conversion. Results are verified by experimental data and comparison to PSpice-AD simulations.

1 Introduction

The VHDL based mixed-signal event-driven (MixED) simulation method [1] has been shown to allow for effective mixed-signal simulation in a number of useful applications. The range of possible applications is smaller than that of tools such as VHDL-AMS [2,3] or PSpice-AD [4]. However, a number of useful mixed-signal circuits have already been successfully simulated, e.g. an analog inverter with operational amplifier (OA) [5], a switched capacitor circuit with OA [6] and a PLL [7].

The three major goals of this communication are

1. to study the accuracy of the MixED-method,
2. to present a simple ΣΔ-modulator as one more useful MixED application and
3. to discuss the clocked comparator as an A/D interface device.

2 Accuracy studies of the MixED method

After presenting a number of circuits that can be simulated with the MixED method, there is an increasing need to demonstrate its accuracy rather than to increase the scope of simulatable circuits. In this communication MixED simulations are compared to both simulated and measured data.

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2.1 Suitable applications

Suitable applications for the VHDL based MixED method are digital designs with some simple analog functions. The mixed-signal gate array offered by the Institute for Microelectronics Stuttgart [8] was identified as an ideal target technology for this method. As illustrated in Fig. 2.1, analog blocks were incorporated into an otherwise digital gate array, the so-called "gate forest" [9].

Customers of gate-arrays have a VHDL rather than a VHDL-AMS simulator. With the MixED module a silicon foundry is capable of offering mixed-signal circuits together with appropriate VHDL models.

The mixed-signal circuit employed for the accuracy studies of this communication is an A/D converter realized as sigma-delta modulator [9] with RC lowpass filter as integrator, as shown in Fig. 2.2.

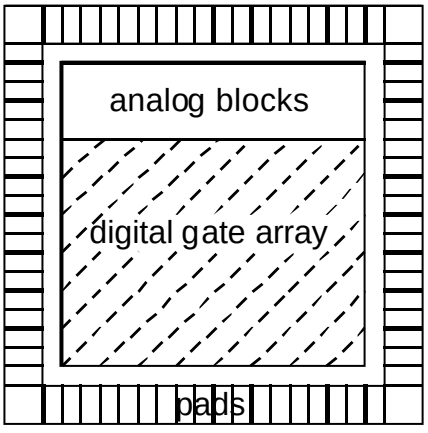

Fig. 2.1: Mixed-signal cells incorporated into an otherwise digital gate array (acc. to Gärtner et al. [9]).

2.2 MixED versus PSpice-AD simulations

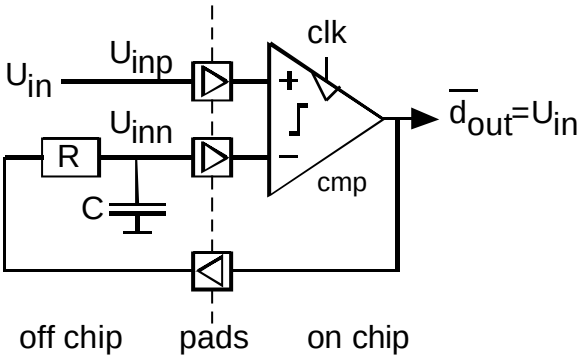

Figure 2.2: ΣΔ-modulator using RC-lowpass as integrator (acc. to [9]): The mean value of d_{out} is proportional to U_{in}.

The sigma-delta modulator illustrated in Fig. 2.2 was simulated with two different mixed-signal simulation tools: Fig. 2.3(a) and (b) show the results of simulations obtained with PSpice-AD and the MixED module using ModelSim 5.3 [10], respectively. The MixED module required 0.26 seconds CPU time on a 500MHz Pentium III processor and was approximately six times faster than PSpice-AD 8.0 [4] on the same system.

In Fig. 2.3 the externally applied analog input voltage, $U_{in}=U_{inp}$, steps from 0V to 5V with a step size of 1.25V. The digital clock signal, clk, is the second externally applied signal. The digital output signal of the modulator, d_{out}, is identical for both simulations. U_{inn} is the voltage at the inverting input of the comparator. It is the lowpass filtered mean value of d_{out} and oscillates around U_{inp}. The results for the analog signal U_{inn} obtained from PSpice and from MixED simulations are very similar, as illustrated in Figs. 2.3 (a) and (b).

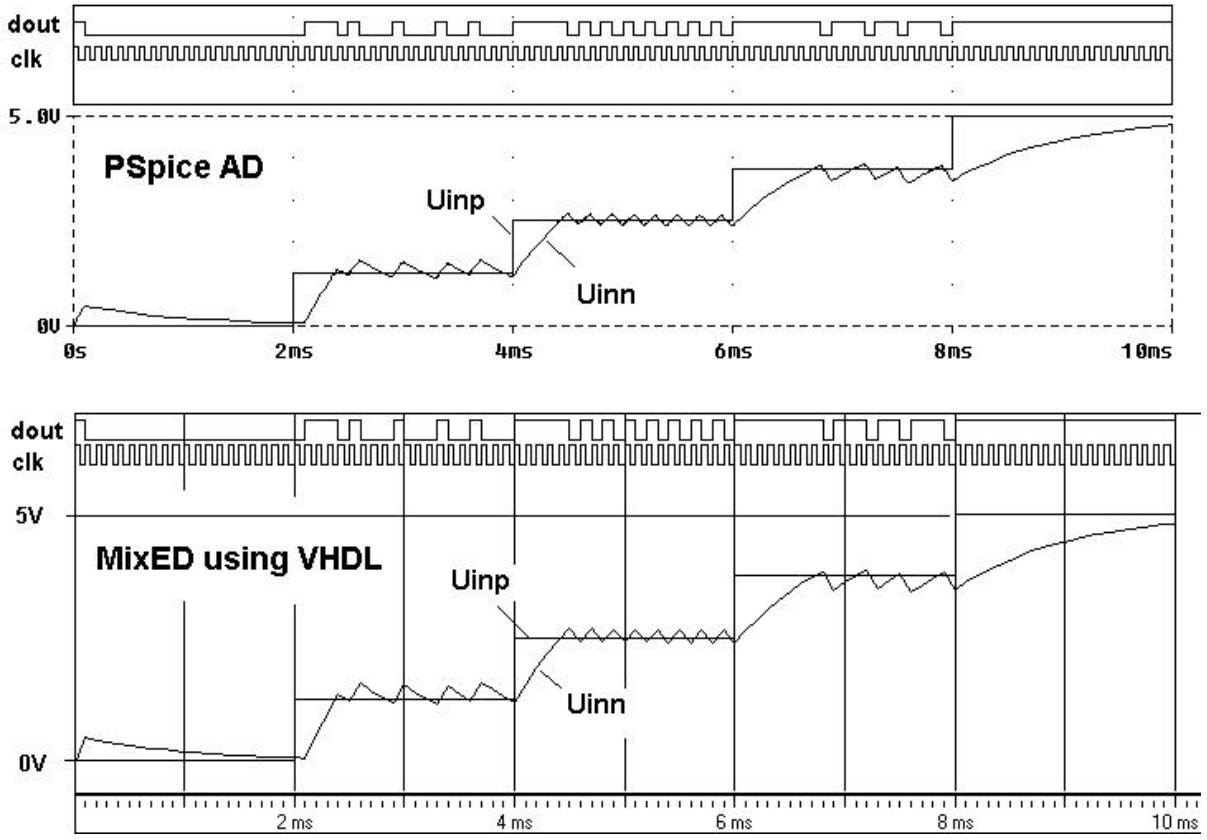

Figure 2.3: Screen shots of simulations of the ΣΔ modulator shown in Fig. 2.2 with $u_{inp}=u_{in}$ stepping from 0...5V with a step size of 1.25V: **(a)** Simulation performed with PSpice-AD version 8, and **(b)** Simulation performed with the VHDL-based MixED module ModelSim 5.3 [10]. ($R=1K\Omega$, $C=1\mu F$ and $f_{clk}=10KHz$.)

2.3 Simulated results versus measured data

2.3.1 Measurement techniques.

Measurements described in this communication are based on a report of Gärtner et al. [9]. It describes the characterization of the ΣΔ modulator shown in Fig. 2.2 with minimum hardware effort. Differences of this work compared to [9] are intended to minimize computational rather than hardware effort.

Fig. 2.4(a) illustrates the reported [9] measurement technique: The bit stream dout is subdivided into intervals of L bit. The number N of '1'-states contained in an interval is counted while the input voltage U_{in} is constant. If N out of L bits are logic '1', the average output value can be computed from

$$\bar{d}_{out} = N / L . \quad (1)$$

Using $a \cong 1$ and $b = V_{SS}$, then U_{out} should equal U_{in} when U_{out} is computed from

$$U_{out} = a \cdot (V_{DD} - V_{SS}) \cdot \bar{d}_{out} + b . \quad (2)$$

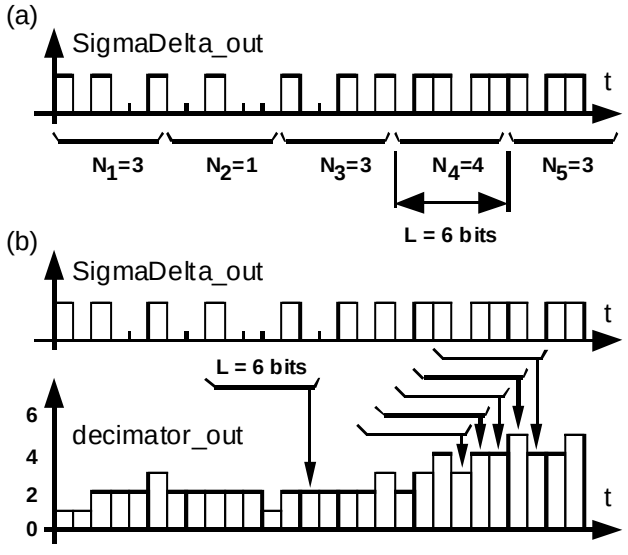

Figure 2.4: Techniques to measure the mean value of the ΣΔ-modulator's pseudo-random output bit stream d_{out}: (a) counters count bits in intervals of Length L, (b) using a decimator.

The measurement technique according to Fig. 2.4(a) minimizes the hardware to two counters: one to measure the interval length L and one to count the N logic '1'-states. However, many intervals have to be measured to acquire statistically satisfactory data.

For simulation purposes a decimator according to Fig. 2.4(b) was employed that delivers an output value for every bit according to the formula

$$decimator\_out(n) = \sum_{i=0}^{L-1} d_{out}(n-i)$$

where the argument (n) indicates an actual value. The argument (n-i) indicates a value that occurred i clock cycles before the actual one. Although the decimator requires $L=2^M$ bit memory instead of 2M bits for two counters, it is advantageous for simulation: the decimator delivers a result with every clock cycle and not only at the end of an interval. Therefore, the decimator acquires L times more data from the same bit stream.

Before statistical data can be taken, the modulator must have been running for more than L bits with constant input voltage to remove the impact of transient effects from measured results.

Simulations documented in this communication use the supply voltages V_{DD}=5V and V_{SS}=0V. The decimator length is L=500 bit so that ΔN=100 bit corresponds to ΔU_{out}=1V. Following [9] there was one measurement series performed with $L = 2^{15}$bit.

2.3.2 Simulation accuracy adjustment.

For the following simulation experiments, the accuracy of the MixED module was increased until further accuracy improvement had no more impact on the output data of the decimator. The accuracy calculated with this method was 5 times higher than that used for the simulation shown in Fig. 2.3. CPU power consumption was found to increase significantly with accuracy. The low clock frequency of 10 KHz was chosen to make unknown details of digital gate delays negligible.

2.3.3 Simulated versus experimental results.

Experimental data [9] is given as statistical data as illustrated in Fig. 2.5. Measuring a good ΣΔ modulator with constant input voltage will deliver B_0 intervals containing N logical '1'-states and B_1 intervals containing N+1 logical '1'-states. [9] reports few intervals contain N-1 or N+2 logic '1'-states as shown in Fig. 2.5(b). The two extreme cases are: (1) U_{in} corresponds exactly to N logic '1'-states as shown in Fig. 2.5(a), and (2) U_{in} corresponds to N+½ logic '1'-states as shown in Fig. 2.5(b).

Simulated data was acquired with R=1KΩ, C=1μF and f_{clk}=10KHz. There were one or two bars in the statistics as shown Fig. 2.5: the decimator with L=500bit delivered B_0 and B_1 times the values N and N+1, respectively. The only exception that occurred was for U_{in}=½(V_{DD}+V_{SS})=2.5V, where only one bar at N=250 was found in the statistics.

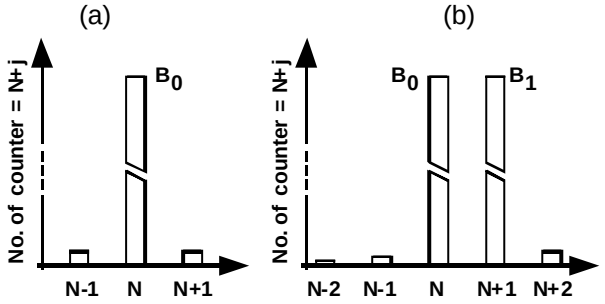

Figure 2.5: Measured data [9] characterizing the ΣΔ-A/D converter: an interval of L bits taken from the output bit stream d_{out} contains N or N+1 logic '1'-states depending on the input voltage U_{in}.

Experimental statistics [9] obtained wider shapes for longer integration intervals. The situation B_0=B_1 as illustrated in Fig. 2.5(b) delivered two bars in the statistics according to Fig. 2.5 until L=2^{13}bit=8192bit. For an interval of length L=2^{14}bit=16384bit more bars appeared in the statistics and for L=2^{15}bit=32768bit the two cases illustrated in Fig. 2.5(a) and (b) could no longer be distinguished. For L=2^{16}bit=65536bit the hardware capabilities were exceeded because more than 8 bars appeared in the statistics.

Simulated statistics obtained with a decimator length of L=2^{15}bit=32768bit did not show a wider shape than for L=500. Used simulation setup: the first 40000 bit of d_{out} (0 to 4ms) were neglected, then 40000 values of d_{out} (from 4 to 8ms) were observed. For U_{in}=2.5V the decimator's output delivered B_0=40000 times the value N=16384 corresponding to

$$\bar{d}_{out}(U_{in} = 2.5V) = 16384 / 32768 = 0.5 ,$$

$$\bar{U}_{out}(U_{in} = 2.5V) = \bar{d}_{out} \cdot 5V = 2.5V .$$

For U_{in}=3.75V the decimator's output delivered 2 bars in the statistics acc. to Fig. 2.5: B_0=29091 and B_1=10909 intervals contained N=23831 and N+1=23832 logic '1'-states, respectively, corresponding to

$$\bar{d}_{out}(U_{in} = 3.75V) = \frac{B_0 \frac{N}{L} + B_1 \frac{N+1}{L}}{B_0 + B_1} = 0.72727 ,$$

$$\bar{U}_{out}(U_{in} = 3.75V) = \bar{d}_{out} \cdot 5V = 3.636V .$$

An increase of the standard deviation as reported in [9] could not be observed for simulated problems. This may be due to a number of idealized assumptions made for the behavioral models.

The simulated characteristics of the A/D converter is shown in Fig. 2.6, where ΔUin=10mV.

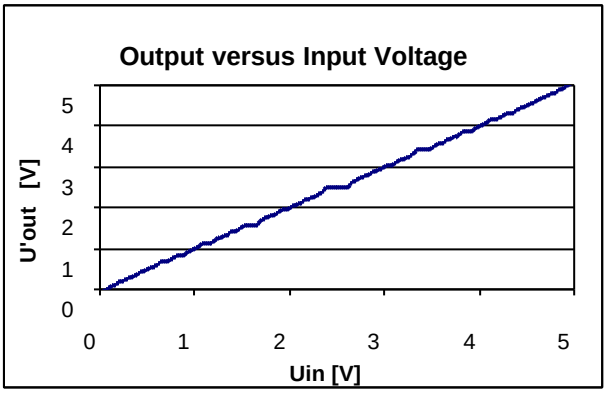

Figure 2.6: A/D conversion characteristics.

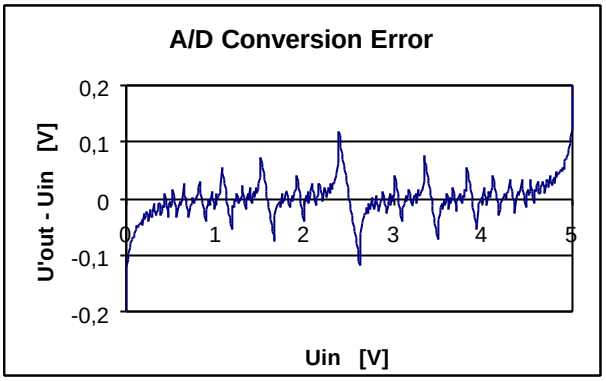

Figure 2.7: Error U_{out}-U_{in} of the A/D conversion characteristics, a=1.1 in eq. (2) and ΔUin=10mV.

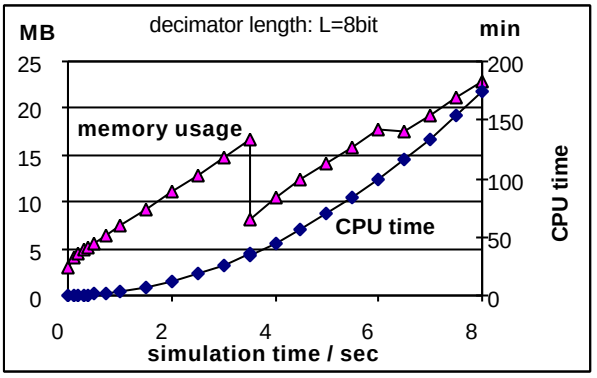

Figure 2.8: CPU power and memory consumption for ΣΔ modulator with 8 bit decimator, f_{clk}=20KHz.

The measured inaccuracy of the ADC in the range U_{in}=1...4V is acc. to [9] less than 1.4%.

The simulated error computed from

$$U'_{out} = a \cdot (U_{out} - 2{,}5V) + 2.5V \quad \text{with} \quad U_{out} = 5V \cdot \bar{d}_{out} \qquad (3)$$

is symmetric around U_{in}=2.5V. It rises to 2.4% for U_{in}=0.1 - 4.9V when U'_{out} is computed from eq. (3) with a=1.1. In the circuit considered a>1 is required to compensate for the finite closed loop DC amplification which is due to the non-ideal RC-integrator. The step size ΔU_{in} is 10mV in Figs. 2.6 and 2.7.The absolute error in Fig. 2.7 with maxima around U_{in}=2.5V is caused by the horizontal plateaus in Fig. 2.6 due to the dead zone problem [11].

2.3.4 CPU runtime and memory usage.

All statistical data in this chapter was taken from simulations on a 733 MHz Intel Pentium III processor operated under Windows-NT 4.0.

Figs. 2.8 and 2.9 illustrate consumed CPU time and memory usage of the simulator for a decimator length of L=8 bit and L=32768 bit, respectively. The data was taken from the Windows-NT task manager. The CPU runtime differences between Fig. 2.8 and Fig. 2.9 correspond to the numerical effort of shifting 32760 bit and counting their '1'-states.

In Fig. 2.8 at 3.5 s simulation time the consumed CPU time and memory usage jump from 2113 s and 16,568KB down to 2089 s and 8144KB. After accidentally restarting computer and simulator the same problem on the same system ran 1.1% faster and used 51% less memory. Furthermore, the simulation speed strongly depends on the simulation time: the simulation speed decreased from 250 to 4 (simulated clock cycles) / (second CPU time) during the simulation shown in Fig. 2.7.

To compare the numerical effort for the ΣΔ-modulator to other digital tasks Figs. 2.8 and 2.9 compare similar simulations with different decimator lengths: for L=23768bit the total consumed CPU time at 8s sim. time was 33% larger than for L=8bit.

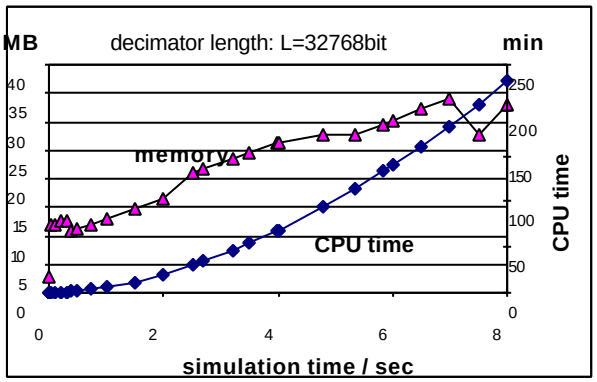

Figure 2.9: Consumed CPU time and memory for ΣΔ mod. with 32768 bit decimator at f_{clk}=20KHz.

3 The clocked comparator

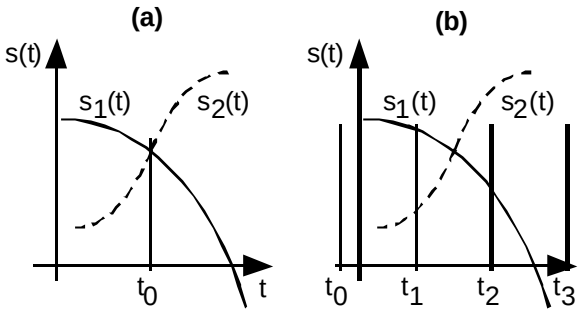

Figure 3.1: Measured versus simulated data for the ΣΔ-modulator.

The clocked comparator is an A/D interface device which allows for effective mixed-signal simulation. A non-clocked comparator has to figure out the cross-over time point, marked as t_0 in Fig. 3.1(a). This requires a careful approach to this point and may cause backtracking. The clocked comparator compares two signals at given time points t_n and avoids the numerical approaching procedure.

The clocked comparator is a new device in the MixED module. Conventional mixed-signal simulators compute a solution for all analog nodes at any point of the analog time axis. The MixED module preserves the event-driven nature of VHDL and allows analog nodes to set time points independently of each other. Therefore, some additional code had to be added to the MixED module which synchronizes the setting of time points for devices with several inputs.

4 Conclusions

The VHDL based MixED module is shown to be capable of simulating a simple sigma-delta modulator with RC-integrator allowing for A/D conversion. This building block is suitable for integration in otherwise digital technologies. Results obtained with the MixED module were compared to both simulated and measured data. Both comparisons validated the MixED method. A clocked comparator model was included in the module.

5 Acknowledgments

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6 References

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