Modeling and simulation of a Sigma-Delta digital to analog converter using VHDL-AMS

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Abstract— **Sigma-Delta digital to analog converters are less vulnerable to circuit imperfections than their A/D counterparts because they have their noise-shaping loop all in the digital domain. Still the analog part of the system (basically a low-pass filter) can degrade the overall performance, especially in the case of multi-bit converters. This paper presents a way of identifying and simulating the major noise and harmonics contributions of the system using VHDL-AMS. The resulting system-level model can be used to explore different architectures in the digital domain and to determine the specifications of the different building blocks.**

Keywords—**D/A conversion, Sigma-Delta, VHDL-AMS**

I. Introduction

In past years Sigma-Delta modulators have been a very popular means for A/D and D/A conversion, mainly because of the low impact of circuit imperfections on the behavior of the converter, due to the noise shaping. [1]. This makes this type of converter scheme more tolerable to changes in technology parameters and mismatch. Research in this area has mainly concentrated on architectural exploration and the impact of circuit imperfections. Because the noise-shaping loop is entirely in the digital domain for a Sigma-Delta D/A converter (Fig. 1), but mainly in the analog domain for the A/D converter, a greater part of the research was devoted to the latter. However, the impact of circuit imperfections in the analog part of the D/A converter cannot be ignored especially in the case of a multi-bit converter. In this paper the different circuit imperfections are identified and the impact of these imperfections is modeled and simulated in VHDL-AMS [2]. In the case that the circuit imperfections are small enough, the ideal signal to noise ratio can be calculated using the assumption that the quantization noise is white and uniform. The signal to noise ratio for an n-bit quantizer can then be calculated [3] using:

$$SNR = \frac{3\pi}{2} A^2 (nl)^2 (2k+1) \left(\frac{OSR}{\pi}\right)^{2k+1} \qquad (1)$$

Where k is the order of the filter, A is the amplitude of the input-sinusoid and OSR is the oversampling ratio and nl is the number of output levels of the quantizer.

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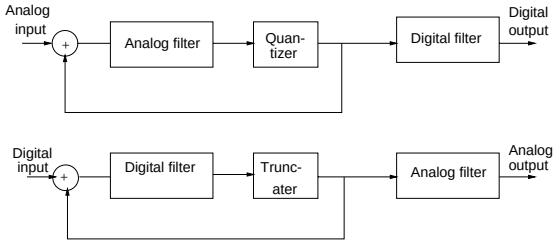

Fig. 1. A/D and D/A Sigma-Delta converters.

II. Modeling of the different components

The Sigma-Delta D/A converter can be split up into different components, this is shown in Fig. 2. For each of the different components a behavioral model is constructed using VHDL-AMS.

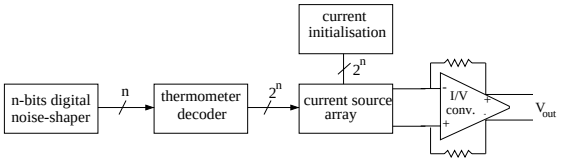

Fig. 2. Block scheme of the Sigma-Delta D/A converter.

A. The digital noise-shaper

This component is the heart of the Sigma-Delta modulator. It is a feedback loop consisting of a truncator and a noise-shaping filter Fig. 3. The truncator just strips the least significant bits of the k-bit input word, thus performing a coarse quantization of the signal. The number of levels resulting from a coarse quantization of n-bits can be calculated as:

$$nl = \#levels = 2^{n-1} + 1 \qquad (2)$$

The error resulting from the quantization is filtered and added to the input. The filter is constructed such that the error will be shaped [4] following:

$$\begin{aligned} Y(z) &= X(z) + (1 - H(z))\, E(z) \\ Y(z) &= X(z) + \left(1 - z^{-1}\right)^k E(z) \end{aligned} \qquad (3)$$

In the model the digital words are replaced by their integer equivalents to facilitate the modeling of the filter and the adders. The truncator now performs an integer division and the adder is the normal addition. When modeling systems with feedback loops, care must be taken not to introduce extra delays in the loop. The simplest way to prevent this is to put the complete noise shaper in one single `process` block. The order of the filter can then be selected by means of a `case...when` statement. Alternatively, the adders and truncator can be put in separate asynchronous processes. These are not sensitive to the clock, but to the output of the preceding block [5]. On the event of a changing input, the process becomes active and will use the new input value to calculate the new output. For higher-order

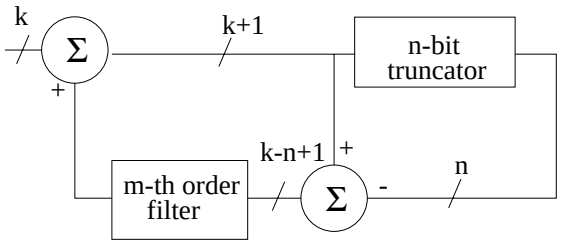

Fig. 3. n-bit digital noise-shaper.

filters overload can occur, which can be prevented by the use of a limiter [6]. Modeling of such a limiter can be done using an `if...then` statement.

B. Thermometer decoder

The decoder is the block which converts the bit stream from the noise shaper into a thermometer code. This can be done in the standard way, but also dynamic element matching (DEM) techniques can be used. Here on top of the normal thermometer decoder, two different DEM techniques are implemented : clocked level averaging (or barrel-shift) and data-weighted averaging (DWA) [7]. The main difference between those DEM techniques is the way the different current cells are selected. The first current cell cs_1 which is selected at time step k can be calculated using:

$$\begin{aligned} \text{normal} &: cs_1(k) = 1 \\ \text{barrel-shift} &: cs_1(k) = k \mod nl \\ \text{DWA} &: cs_1(k) = \sum_{i=1}^{k} cs_1(i) \mod nl \end{aligned} \tag{4}$$

From (4) it can be seen that the DEM techniques are based on modulo-nl counters. In VHDL-AMS a counter comes down to storing an index in memory, which can easily be done using a `variable`. Since the noise-shaper output is an integer, the indices are too, which means normal addition and modulo statements can be used to model the counter. The output of the decoder is a `bit-vector` of length nl.

C. Current source D/A converter

The D/A converter in a multi-bit Sigma-Delta, needs to be fast, but has relatively few output bits. This makes it suitable to be realized using a current source array. The resolution must be as high as the desired resolution of the complete Sigma-Delta modulator. This means that the constraints on mismatch of the different current sources are high with respect to the number of output bits. By using DEM techniques, clever layout and scrambling of the order of current sources, this can be achieved. In general it will cost more area and power to do so. Because neither the current sources nor the switches can be considered to be ideal, the impedance seen from the output node n_1 changes when the number of selected current sources (i.e. the activated cells) changes. A system like this can be modeled using the scheme depicted in Fig. 4. The current I_{cs2}, R_{cs2}, R_{on2} and C_{cs2} are the lumped current and impedances of the part of the array which is switched on at that moment. The current I_{cs1}, R_{cs2}, R_{on2} and C_{cs2} are the lumped current and impedances of the part of the circuit that was already on. If DEM techniques are being used care must be taken, as even for the same input code, current sources are being switched on and off. This setup diminishes the number of quantities used, which causes the simulation to run faster. However, this setup requires the impedances and the currents to be changed instantaneously. Although this is possible by the use of `signals`, it is unpredictable how the simulator reacts to such an abrupt change. Normally this can be resolved by the use of `break` statements. Unfortunately in the simulator used by us, this was not implemented (yet). This means that the only proper way to model such a system is by an array of (nearly) identical current cells. This can be done by using the `generate` statement. This approach is of

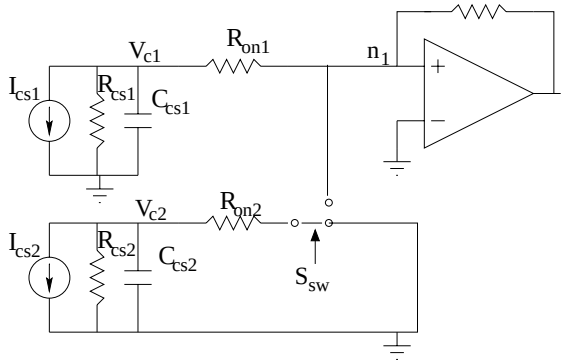

Fig. 4. Lumped model of D/A converter current sources.

course much more straightforward, but is also slower, because the number of quantities used is larger. The model for one such current cell is depicted in Fig. 5

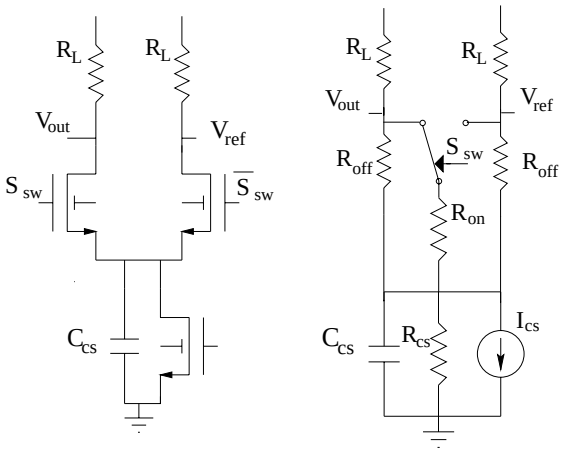

Fig. 5. Model for a current cell.

D. The current to voltage converter

If the output of the current-source array would feed into a normal resistor, its voltage would be sweeped from the highest output to the lowest output, which would increase the settling time. To prevent this from happening, a virtual ground is created using an opamp The opamp model used is depicted in Fig. 6. The model makes it possible

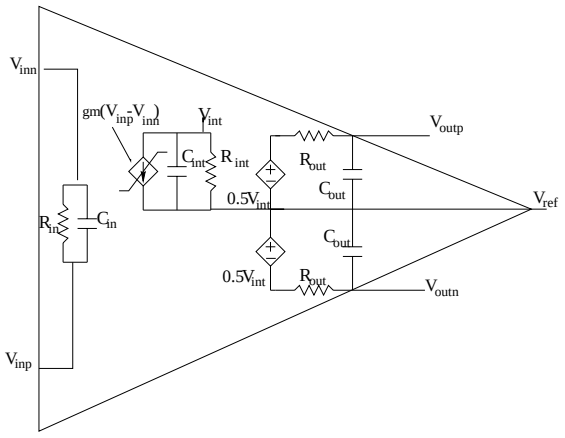

Fig. 6. Model for the opamp.

to specify finite in- and output impedances, finite gain and gain-bandwidth product and slewrate. The latter is accomplished by limiting the voltage controlled current source output current to I_{max}. The basic equations used to transform the given specifications into the internal equations used by the model are given by:

$$GBW = \frac{gm}{2\pi C_{int}}, \qquad SR = \frac{I_{max}}{C}$$
$$A = gm\,R_{int}, \qquad \tau = \frac{1}{2\pi RC} \tag{5}$$

III. The impact of different circuit non-idealities

In this section the modeling of the different circuit non-idealites will be described and the impact on the system's signal to noise ratio will be examined. It is always assumed that the maximum output voltage of the buffer is 1 Volt peak to peak.

A. Mismatch of the current cells

The currents in the different current cells are suffering from mismatch, both due to systematic and random errors. The systematic errors can be modeled using a linear or quadratic gradient on the complete current array. In this manner the cell in the middle will have zero systematic error and the ones at the beginning and end of the array will have maximum error. The systematic errors can be minimized by the use of scrambling and by placing the different current cells in a quad (or a quad-quad) formation, which makes errors due to a linear gradient add up to zero (the quadratic error remains however). The errors resulting from random mismatch are modeled by the use of a random number generator with normal distribution. This is the **current-initialisation** block in Fig.2. Since information of the actual output is not fed back to the noise-shaping loop, the random errors of the DAC cannot be compensated for. If high accuracy is needed, these random errors can diminish the overall signal to noise ratio. The impact of the random errors can be calculated using the fact that the deviation in output current for an input word K can be denoted as:

$$\Delta I_{out} = \Delta I_{cell}\sqrt{K} \tag{6}$$

Normalizing the members of this equation respectively to the maximum output current and the current of one cell, yields:

$$\sigma\left(\frac{\Delta I_{out}}{I_{max_{out}}}\right) = \frac{1}{2\sqrt{nl}}\sigma\left(\frac{\Delta I_{cell}}{I_{cell}}\right)\sqrt{K} \tag{7}$$

Random mismatch can be reduced greatly by careful layout (by using more area per current cell) and by using DEM techniques.

B. Settling time of the current array output

Since the settling time of the system is an important specification, the settling behavior will now be investigated. When the opamp is connected to the output of the

current source array, the resulting transfer function can be calculated. To simplify the equations, the opamp is assumed to have zero output impedance and $R_{cs} \gg R_{on}, R_f$. Furthermore a capacitance C_h is introduced to deal with the influence of other cells in the array that are switched on. This capacitance runs from the opamp input to ground (the R_{on} of the other switches is neglected here). The output voltage then becomes:

$$\frac{V_{out}}{I} = H_b(s) = \frac{A_f}{s^2 + 2s\omega_n\zeta + {\omega_n}^2} \tag{8}$$

where:

$$\begin{aligned} A_f &= \frac{R_f A_0}{den} \\ \omega_n^2 &= \frac{A_0 + 1}{den} \\ 2\omega_n\zeta &= \frac{\tau + 2C_{in}R_f + A_0 C_{sc} R_{on} + C_h R_f}{den} \\ den &= R_f\left(C_{sc}R_{on}\left(2C_{in} + C_h\right) + \tau\left(2C_{in} + C_{sc} + C_h\right)\right) \end{aligned} \tag{9}$$

In equation (9) it becomes clear that the damping factor ζ is dependent on all the different time constants in the system. This damping factor has a large impact on the system's behavior, especially for relatively high clock frequencies. If the damping factor is too low, this means that the impulse response is oscillating. and since at every new clock pulse one of the current sources is switched on or off, this oscillatory impulse response modulates the input signal. This oscillation means an error on the expected output level, resulting in an attenuation of the signal to noise ratio. On the other hand, if the damping factor is too high, the output signal will never reach its end-value (incomplete settling), which gives a distortion to the signal. The distortion which occurs for each output value is dependent on the relative distance of the output value from the output levels possible. For output values just on or right between two output levels, the errors will ad up to zero. Otherwise the resulting error is dependent on the settling time of the system, which can be calculated from (9). The maximum error can be obtained calculating the mean difference between the desired step response (which is $1/nl$ Volt) and the actual step response:

$$e_{max} = \frac{1}{2nl}\int_0^{\frac{1}{fs}} h_b(t) * u(t) - \frac{1}{nl}dt \tag{10}$$

Where $h(t) * u(t)$ is the response of the opamp output for an input-current step. Since the minimum error is zero and a uniform distribution may be assumed, the resulting noise power becomes:

$$e_{rms}^2 = \frac{1}{e_{max}}\int_0^{e_{max}} e^2 de = \frac{e_{max}^2}{3} \tag{11}$$

C. Slew rate of the opamp

Not only the opamp's settling behavior, but also the slew rate has an important impact on the system's total signal to noise ratio. Again the error is dependent on the distance between the actual (desired) output value and the possible output levels. If it is assumed that the absolute values of the positive and negative slew rate are equal and that always the two levels are used that are closest to the desired value, the resulting maximum possible error can be calculated as:

$$e_{max} = \frac{f_s}{2(nl-1)SR}\frac{1}{nl-1} \tag{12}$$

Equation (12) can be explained when it is noted that the slewing takes place between two adjacent levels (which are $1/nl$ Volt apart) and that the error is relative to the clock period. The resulting relative error has to be divided by $nl - 1$ to calculate the absolute error. Again the resulting noise power may be calculated using (11)

IV. Simulation results

A number of simulations has been performed using the VHDL-AMS models described in section II. The influence of slew rate, current mismatch and finite gain-bandwidth of the opamp are examined.

A. Impact of slew-rate

To investigate the influence of finite slew rate of the opamp, a 5-bit (17 level) second order Sigma-Delta converter is simulated. The current cells have no mismatch and the oversampling ratio and input amplitude are chosen such that according to (1) the SNR should be 58 dB. The results of the simulation are shown in figure 7 Using (11) the theoretical curve is plotted. Differences between the simulated and the theoretical value can be explained in the fact that the equation (11) is an oversimplification of the real behavior. For slew rates higher than $10V/\mu s$, the system follows its theoretical signal to noise ratio until it begins to suffer from other circuit imperfections such as the described oscillating behavior.

B. The impact of the current cells mismatch

The impact of the mismatch of the current cells can be made visible using the same system as described in the previous section. The opamp slew rate is set to a value of $20V/\mu s$, just to make sure that it is only the current mismatch which has high impact on the system's behavior.

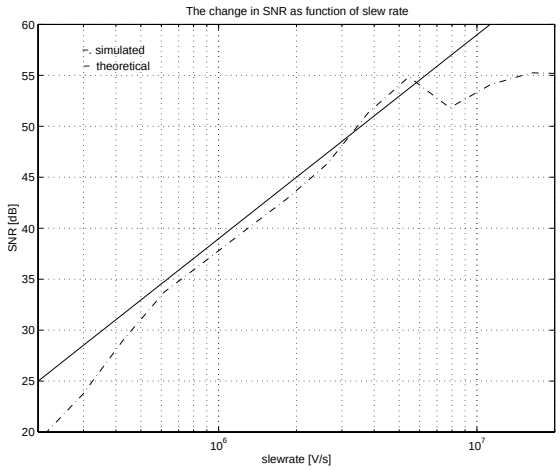

Fig. 7. SNR as a function of slew rate of the opamp.

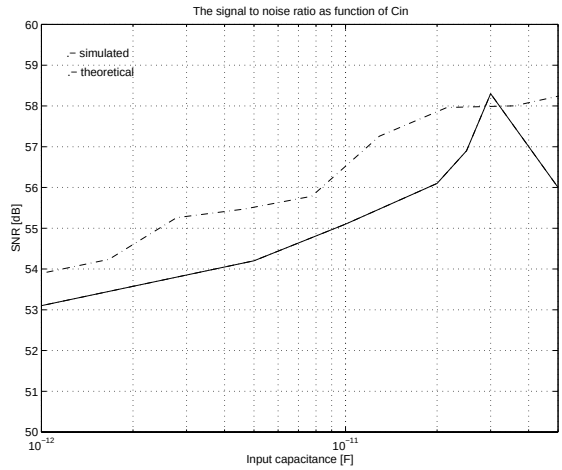

Fig. 9. SNR as a function of the opamp's input capacitance

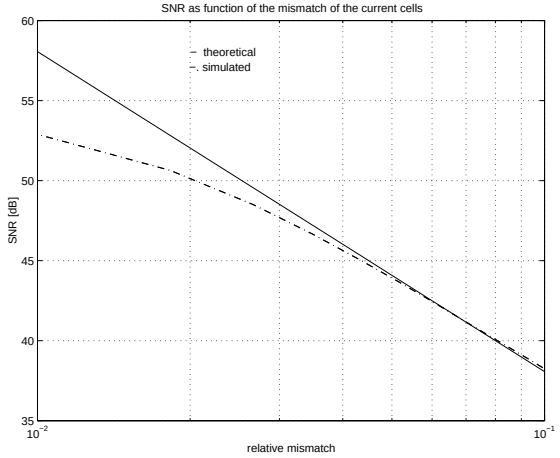

Fig. 8. SNR as a function of mismatch of the current cells

The theoretical curve in Fig. 8 is plotted using (7). For low mismatch levels, other sources of error as well as the theoretical limit (1) are more dominant than the current cell mismatch. For larger amounts of mismatch simulation results correspond very well with the calculated ones.

C. The impact of the input capacitance of the opamp

Because of the complex nature of (9) it is cumbersome to sweep all of the different elements and look at the resulting change in SNR. Therefore it was chosen to only look at the input capacitance of the opamp, since this is one of the elements which has a high impact. The resulting change in SNR is depicted in Fig. 9 The theoretical curve is calculated using (10). In Fig. 9 it is shown that about 4 dB can be won by adding extra capacitance to the input nodes of the opamp. However, this result is only valid in this particular case, because changes in other opamp parameters or in the clock period, will shift the optimum value of C_{in}. Furthermore, this effect cannot be analyzed analytically, because of the impendance changing with on or off switching of the current cells. This means the only way to get insight in this behavior is by the use of models such as described in this work.

V. Conclusions

In this work a VHDL-AMS model of complete Sigma-Delta D/A converter was developed. This model can be used to perform high-level analysis of the impact of system non-idealities, such as opamp slewing and current source mismatch. The results of the analysis can be used to find an optimum set of building block specification yielding optimum system performance

Acknowledgments

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