BMAS 2000

High-level design case of a switched-capacitor low-pass filter using Verilog-A

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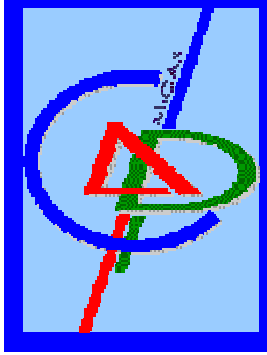

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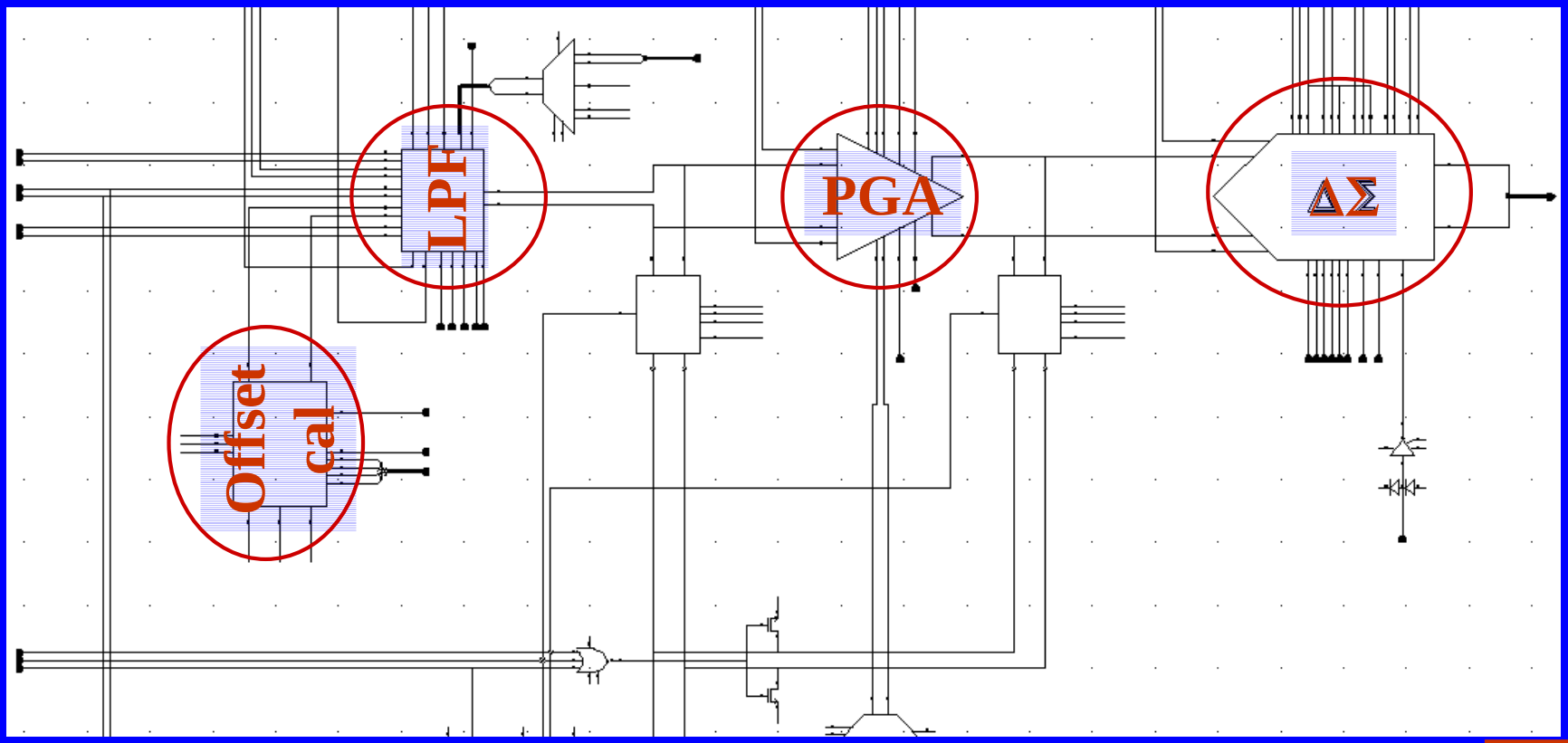
Introduction

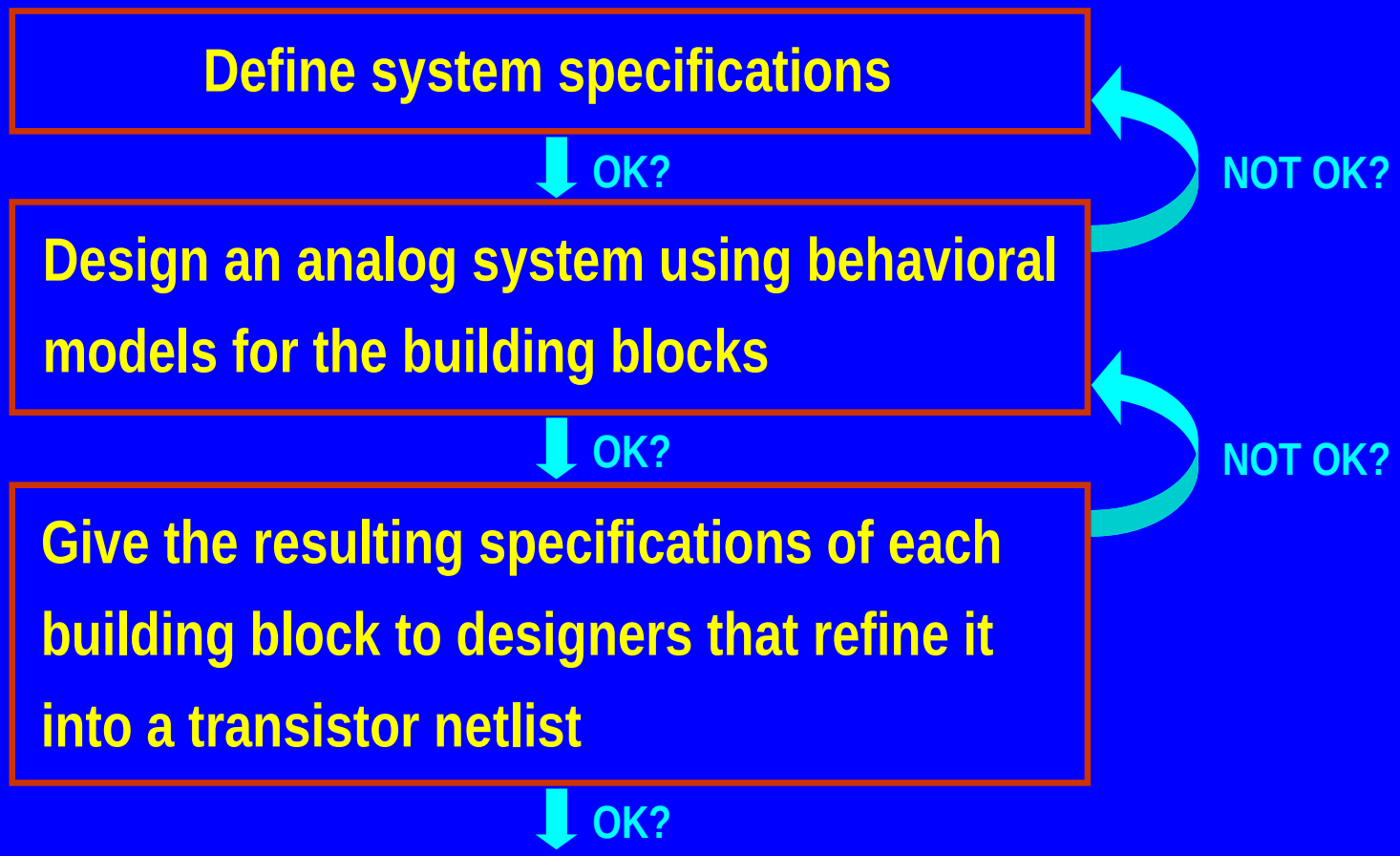
Behavioral models as a tool for:

- Verification: ideal functionality, connectivity
- High-level design



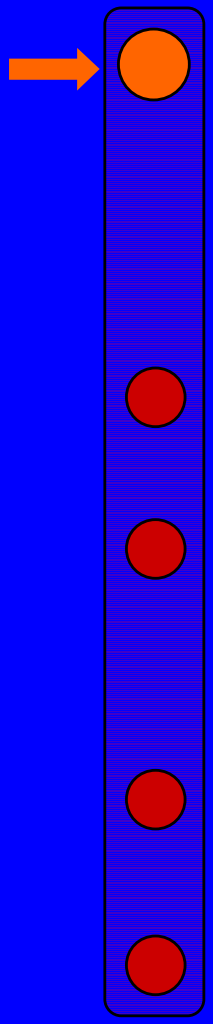
Introduction

High-level analog design?



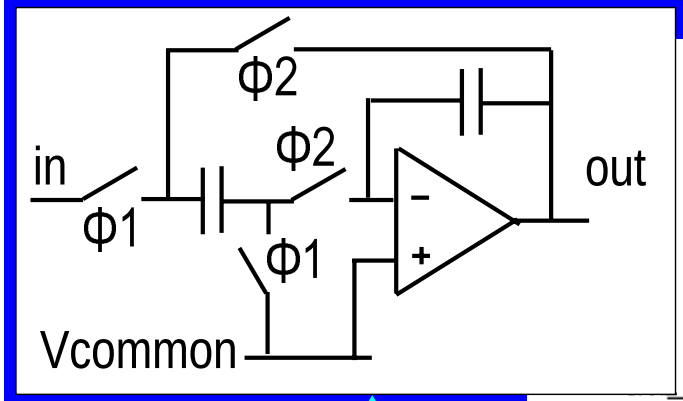
This means: accurate, feasible, non-ideal models

Overview



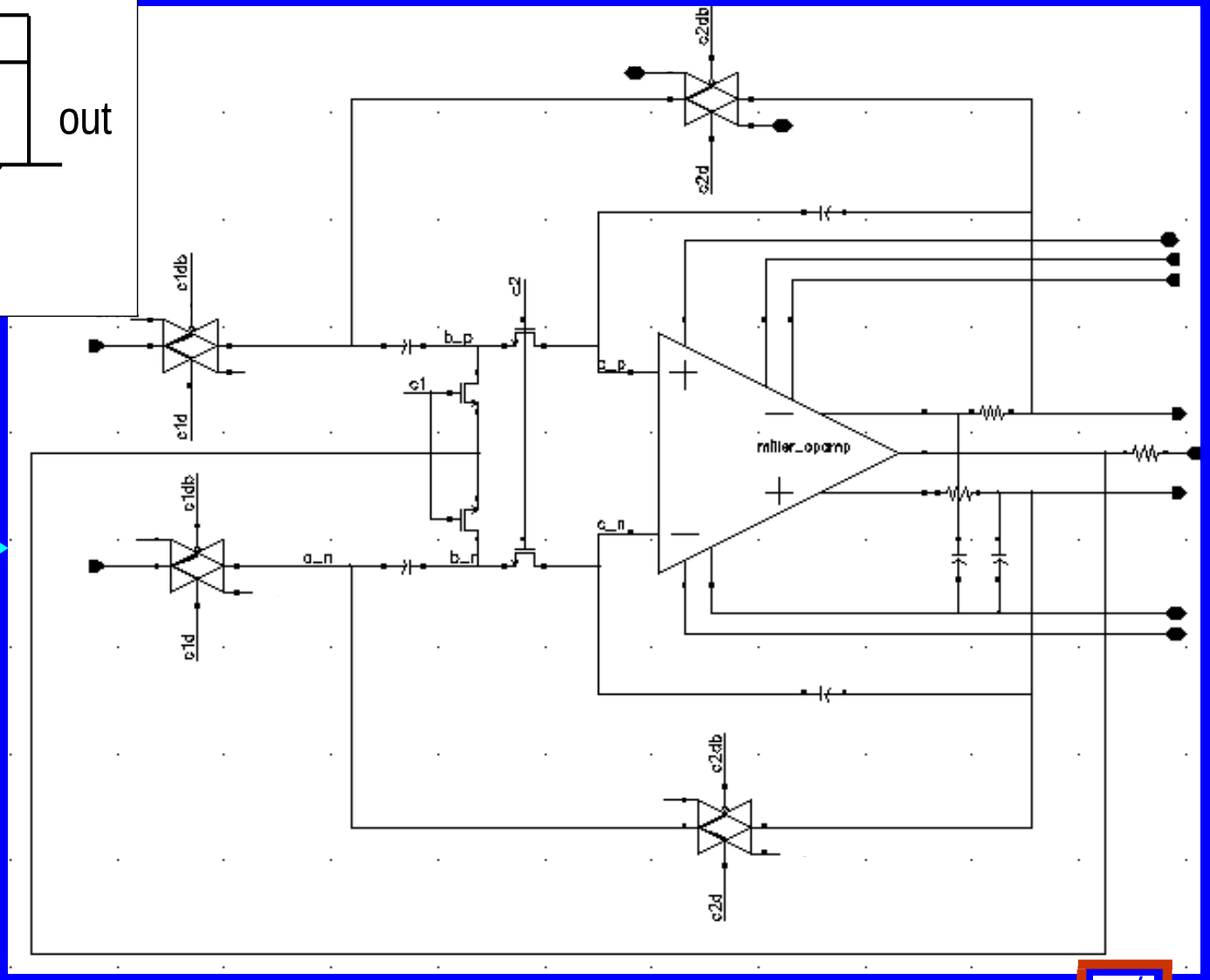
- **Switched-capacitor low-pass filter**
  - Topology / Schematic
  - Specifications / goals
- **Behavioral Miller OPAMP model**
- **Behavioral switch (or passgate) model**
- **Simulation results with Verilog-A**
- **Summary and conclusions**

Switched-capacitor low-pass filter: circuit



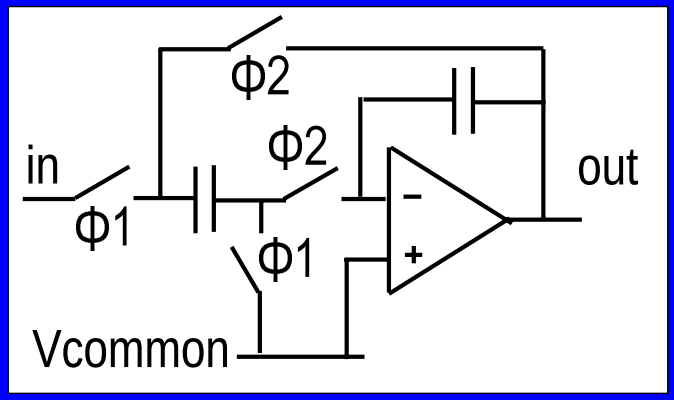
topology

and “schematic”



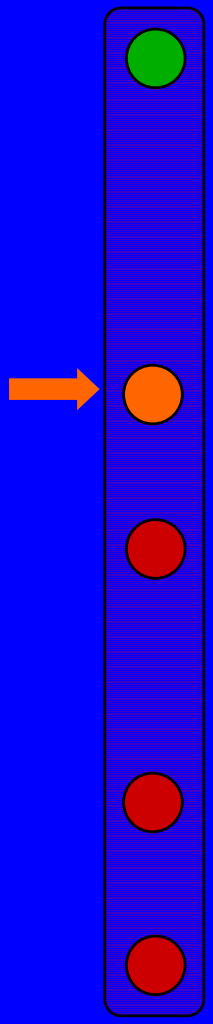
1 Miller Opamp
4 passgates
4 nmos switches
4 capacitors
+ external load

Switched-capacitor low-pass filter: specifications



Input signal condition	Differential, 2.8 Vpp max
order of the filter	1st-order SCF
Output signal condition	Differential, 2.8Vpp max.
In-band ripple	< 0.2dB, pole = 2.5 MHz
THD	-53 dB
Tone due to clock	< -30 dBc
…	…

Overview



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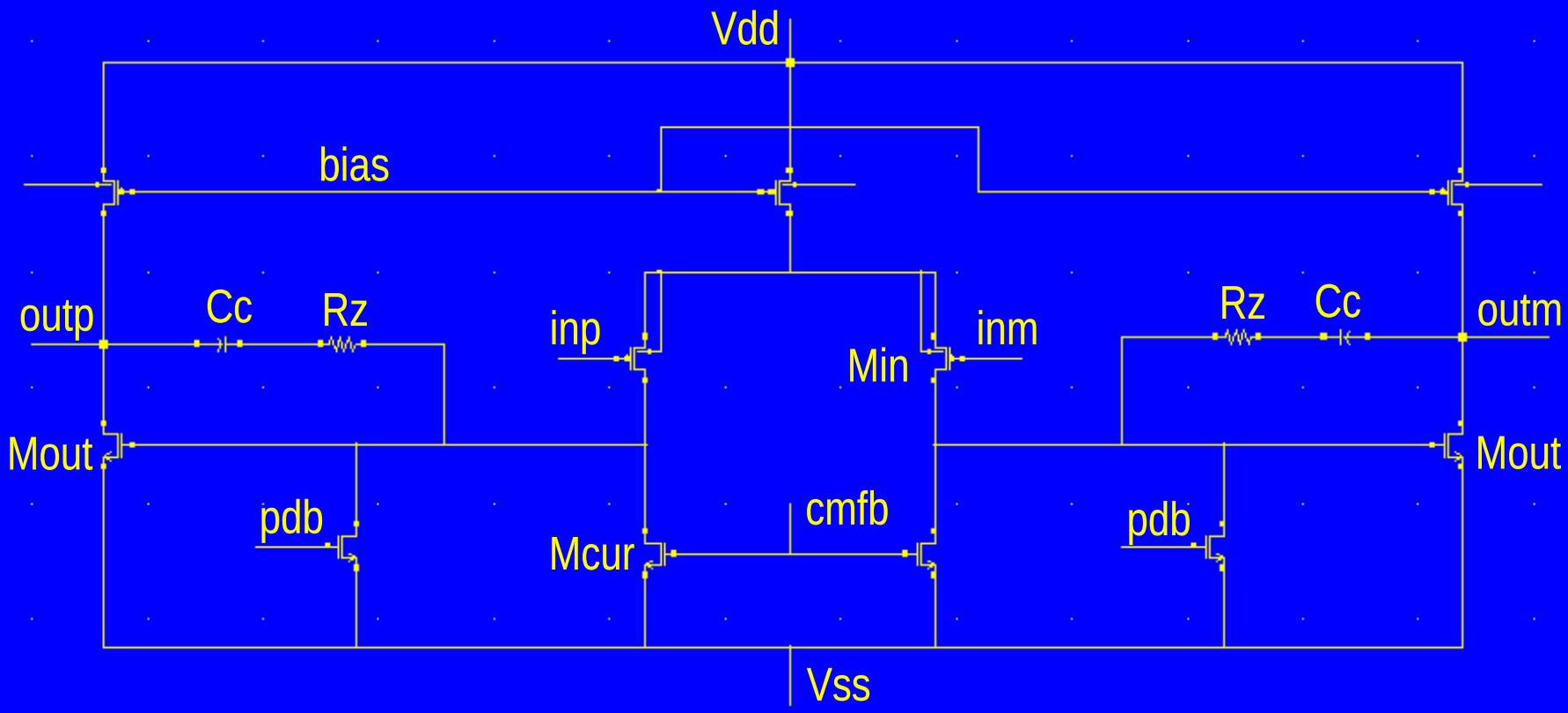
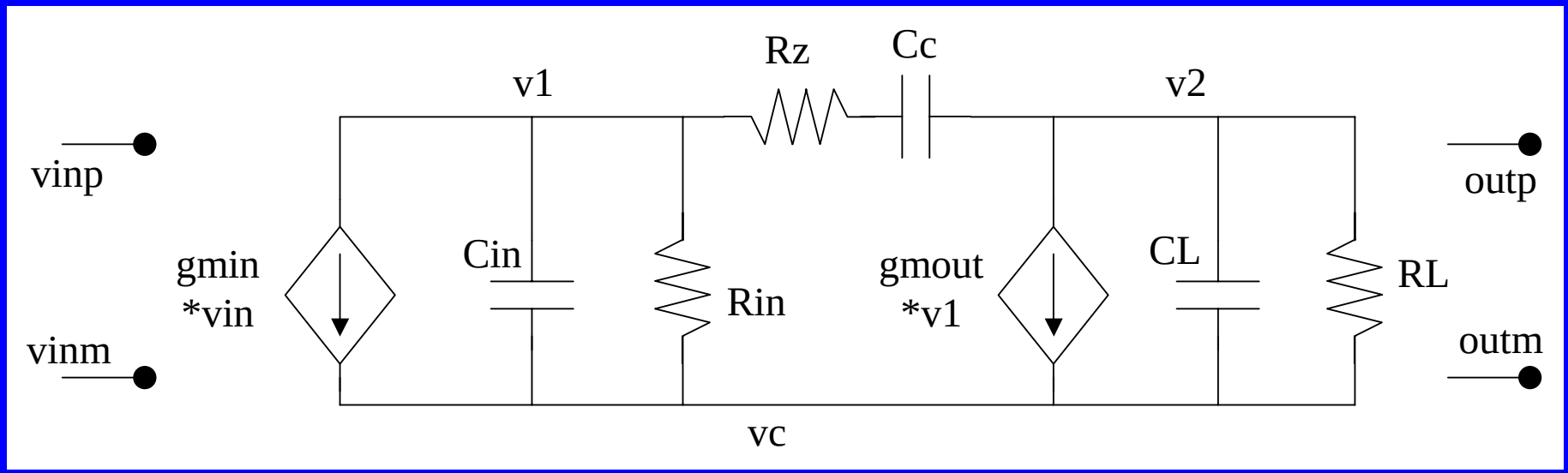
Miller OPAMP



- Gain
- GainBandWidth
- input referred offset
- SlewRate
- PhaseMargin
- CapacitiveLoad
- ResistiveLoad
- total integrated output white noise

+ technology, +topology: non-ideal, feasible model

Miller: model



- Values are calculated from high-level parameters using ideal hand formulas and following a design plan (first-order behavior)
- @(initial_step)
  calculate RL, Rin, Iin, Ioutm, gmin, gmout, gmcur, Cc, Rz
  from high-level parameters

Next: add specific behavior == non idealities

Miller: AC and Noise model

- **in AC simulation:**
  - An Operating Point is calculated. A linear behavior is expected from in this OP
  - No clipping or slewing effects have to be taken into account.

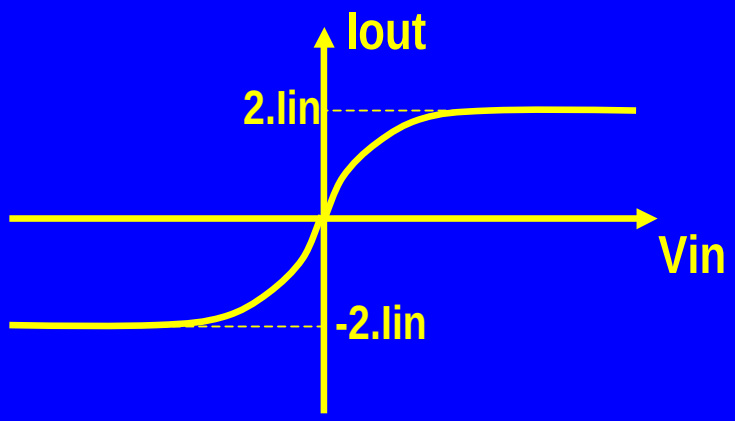
- **A noise analysis uses the same behavior**
  - 3 possible user modes:
    - No noise
    - Only white noise sources
    - White and Pink noise sources: corner frequency to be provided by user
  - Important for interaction with other blocks/components

$$\text{int. white noise@output} \approx \sqrt{\text{GBW} \cdot \text{gain} \cdot \frac{\pi}{2} \cdot \overline{\text{dv}_{\text{N,i}}^2}}$$

Miller: transient model

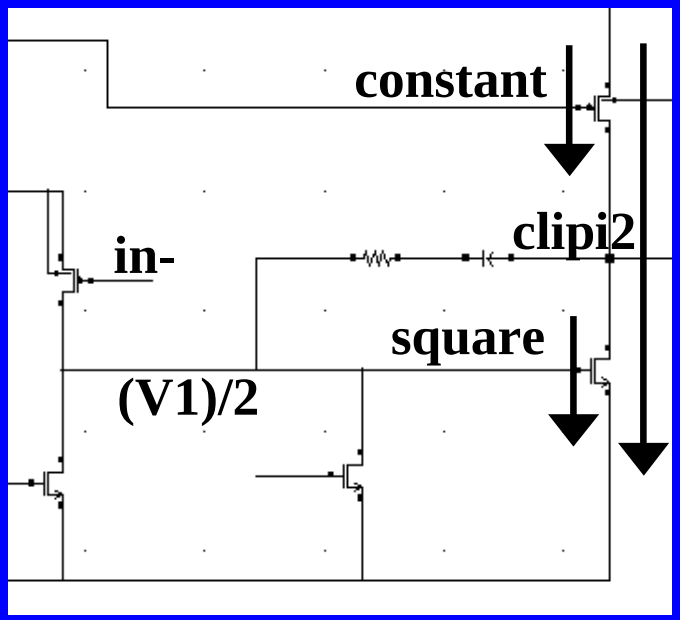
- slewing by limiting the current = change gm

1



$$i_{out} = \frac{2 \cdot v_{in} \cdot I_{IN}}{(V_{GS} - V_T)_{in}} \cdot \sqrt{1 - \frac{v_{in}^2}{4 \cdot (V_{GS} - V_T)_{in}^2}}$$

2



$$\text{if } \frac{v_1}{2} < -(V_{GS} - V_T)_{OUT}$$

$$clipi2 = I_{OUT}$$

else

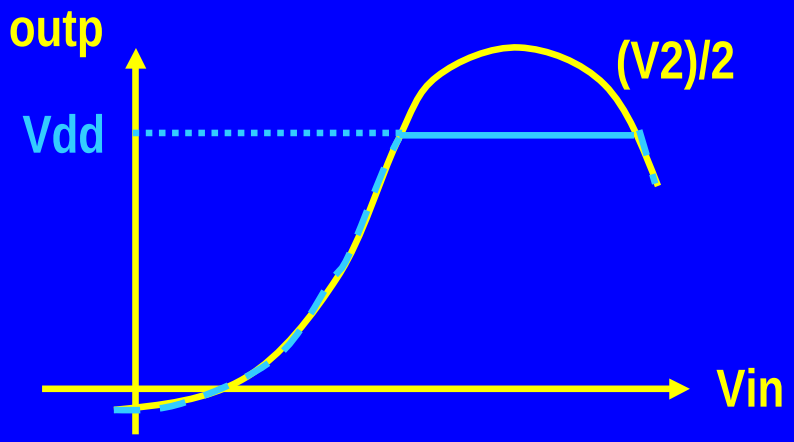
$$clipi2 = I_{OUT} - \frac{v_1^2 \cdot I_{OUT}}{4 \cdot (V_{GS} - V_T)_{OUT}^2} + \frac{I_{OUT} \cdot v_1}{(V_{GS} - V_T)_{OUT}^2}$$

Miller: transient model

- Clipping: the outputs and the internal nodes

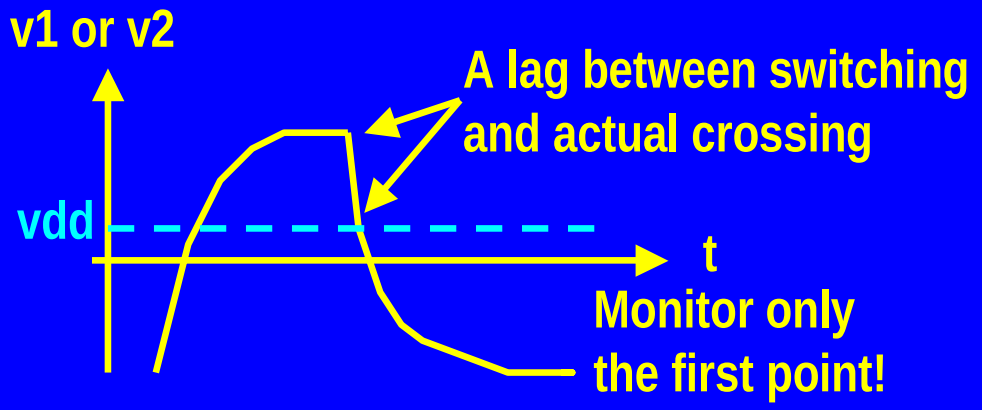
1 - Each output has to be clipped separately because this depends on the common-mode output value.

- Abrupt / smoothened clipping

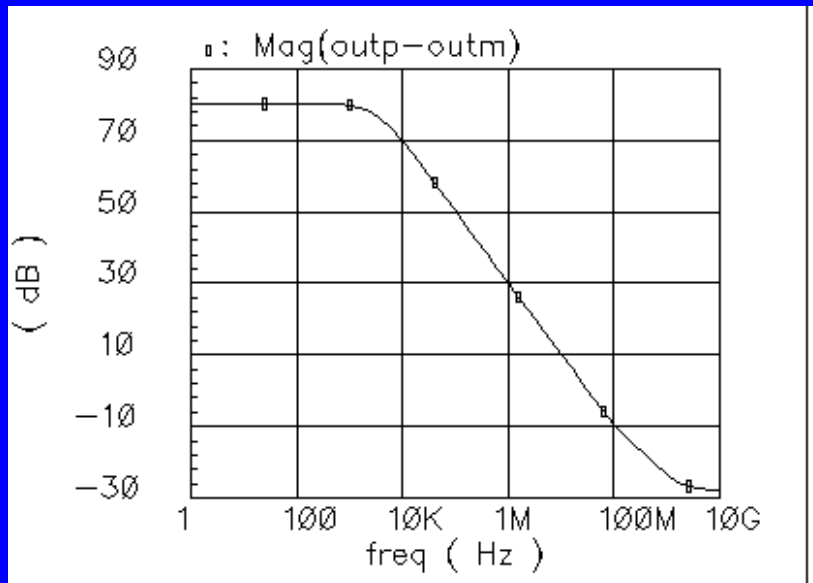


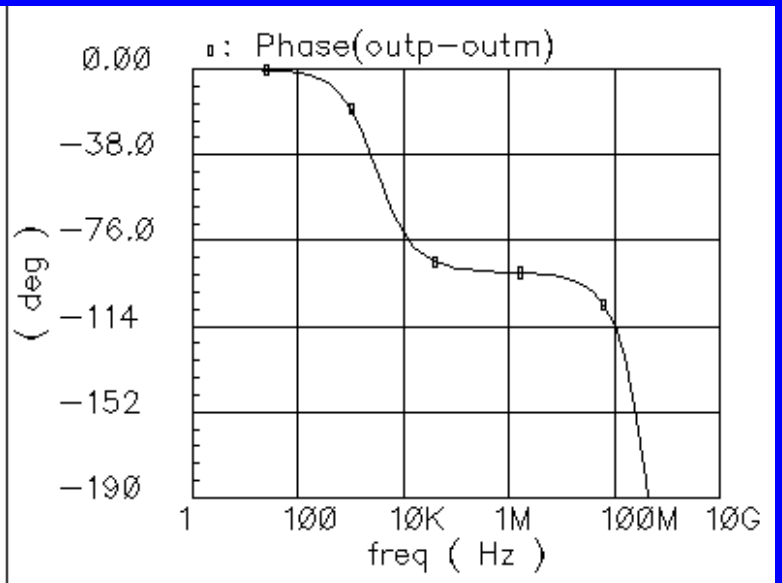
2 - Switching behavior? (large input signals)

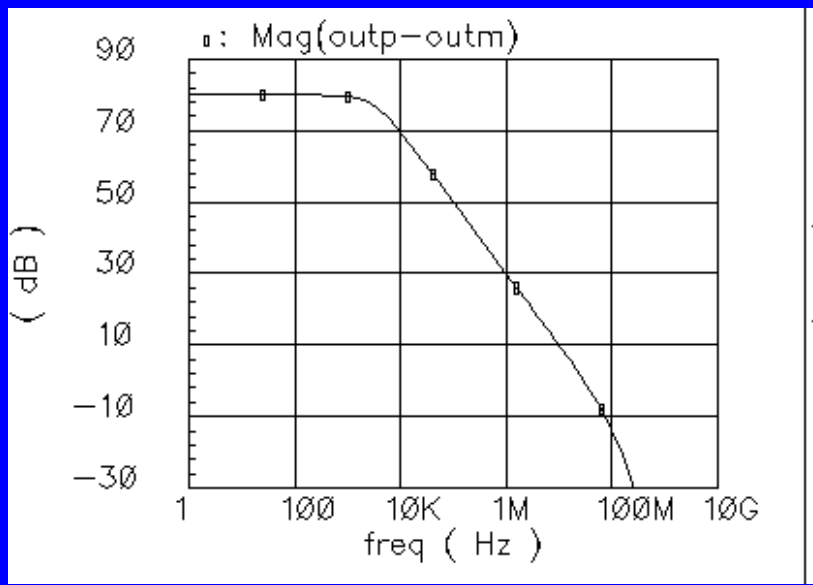
- Preclip the internal signals and still allow correct asymmetrical output clipping
- Use feedback to solve timing problem: measure node 2, adjust node 1.

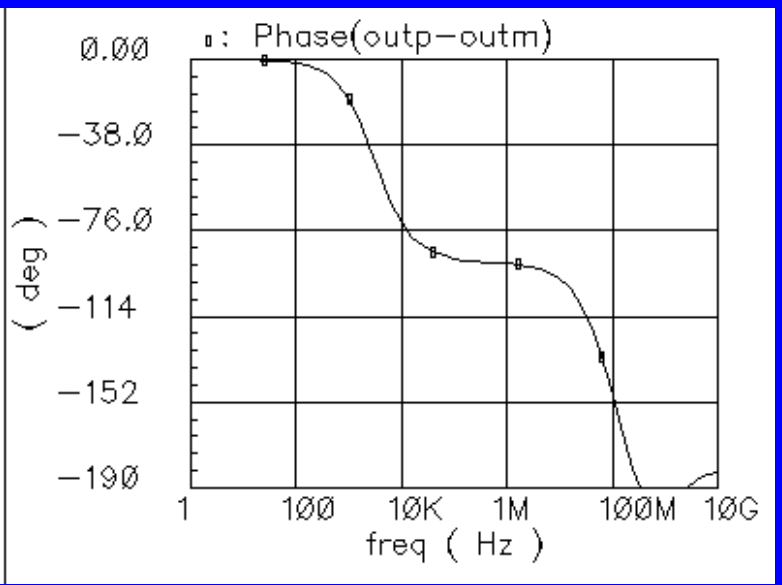


Miller simulations: AC

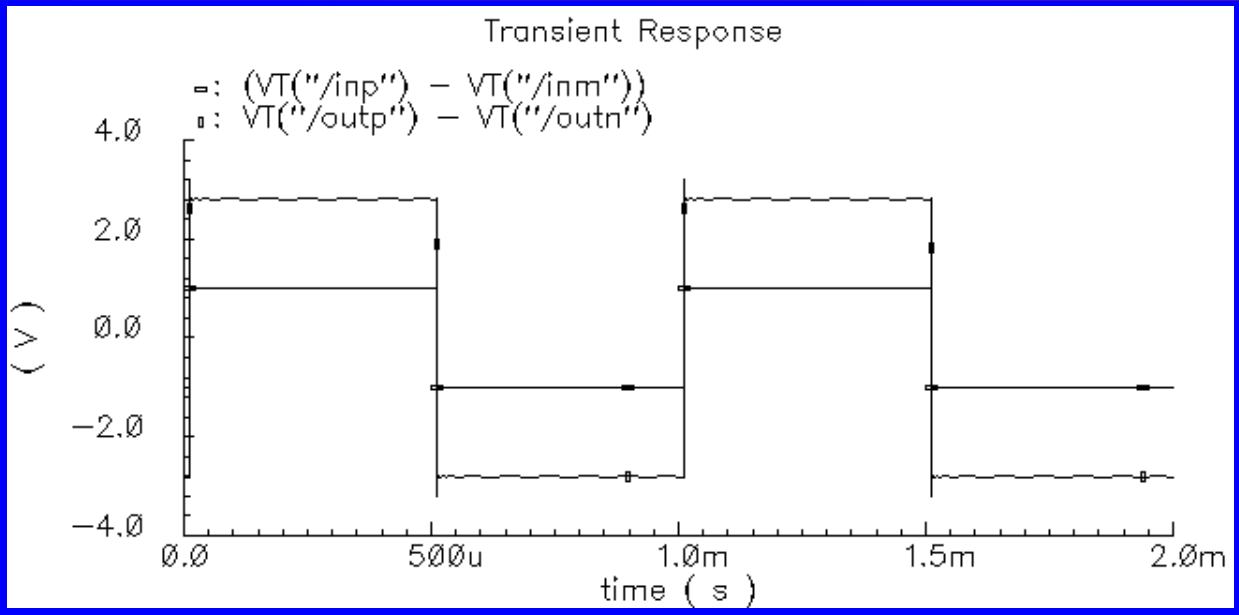


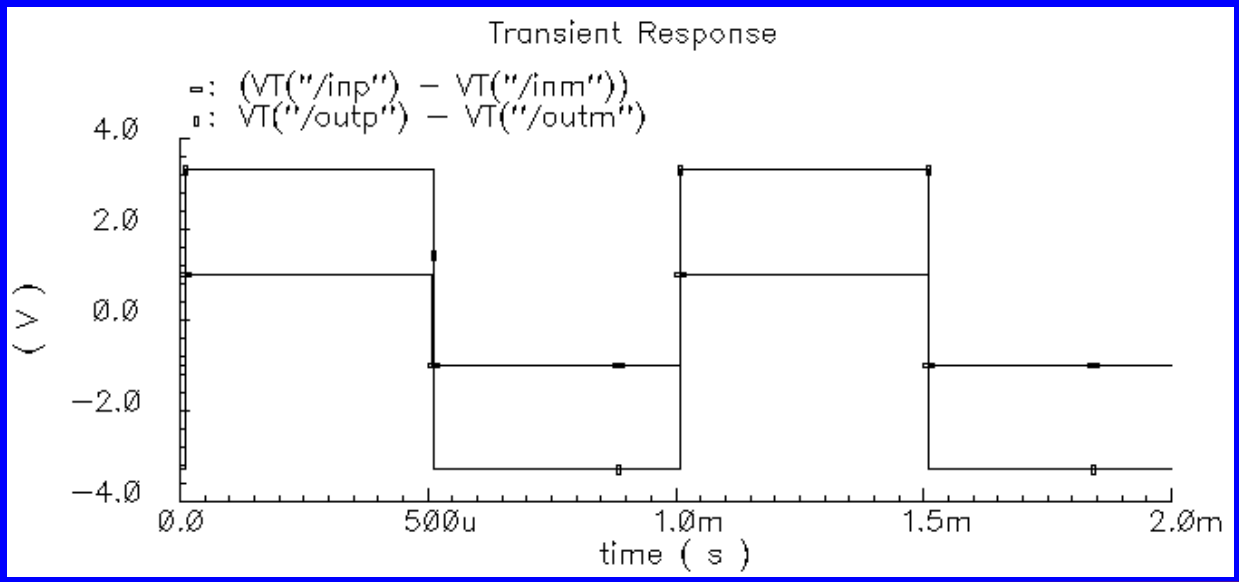




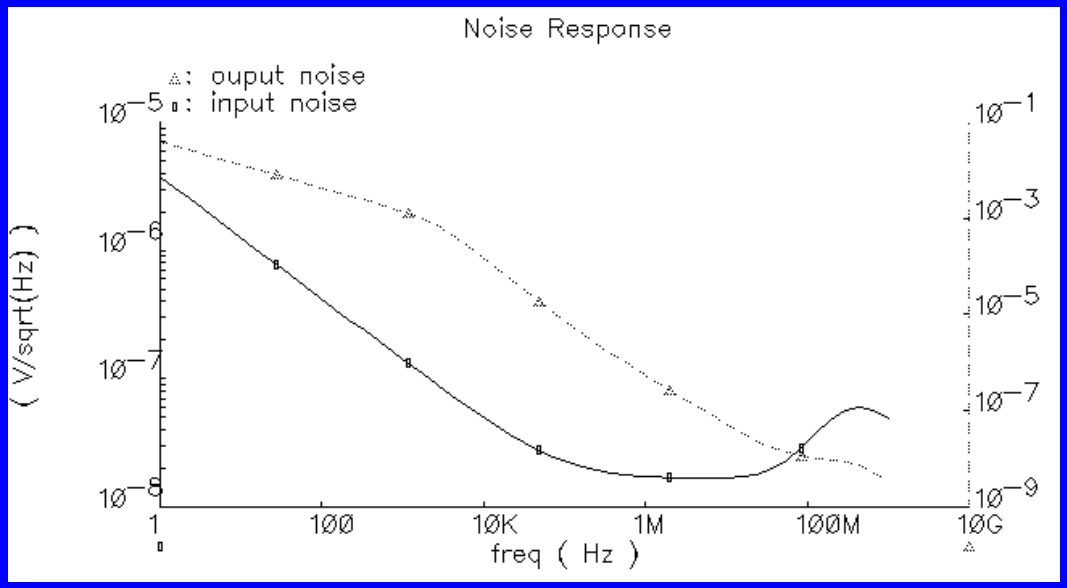


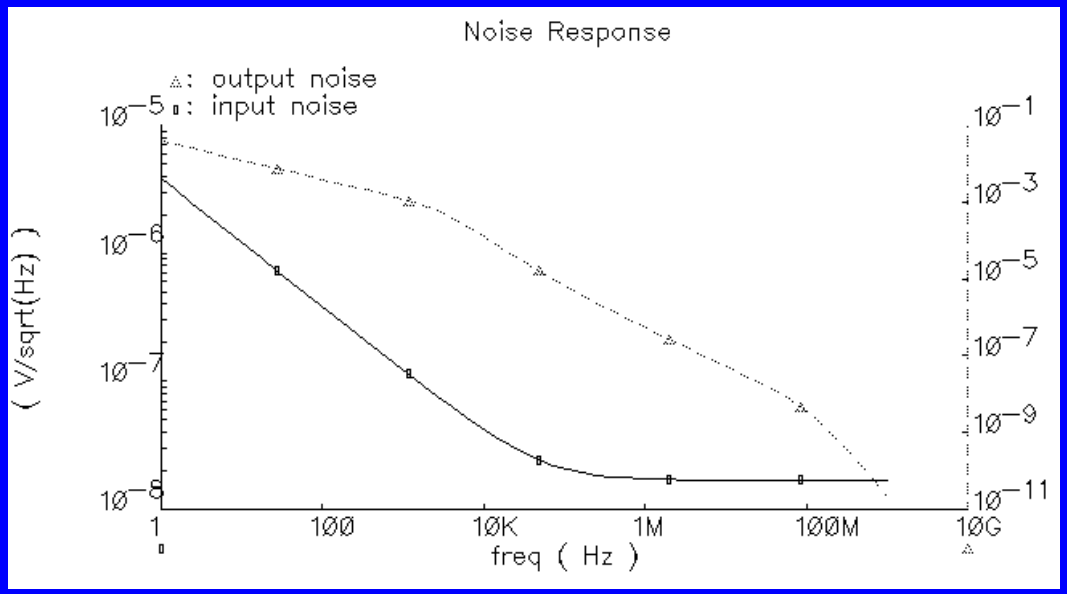
Miller simulations: tran





Miller simulations: noise





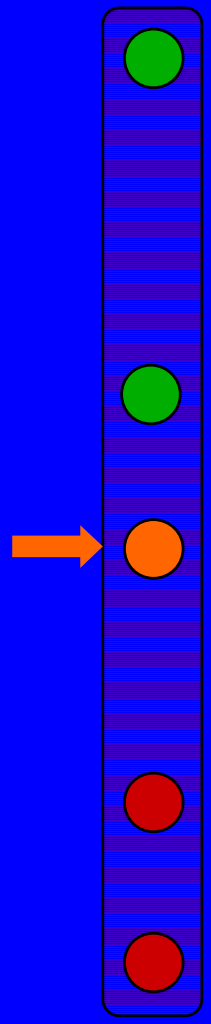
Simulation time comparison

Simulation time	schematic	behavioral**	remarks
tran. Large signal	6.03s	1.07s	same delay
tran. Clipping	2.4s	0.2s	0 --> 3.3V vs. 0.07 --> 2.73V
tran. No clipping	1.55s	0.2s	HD3=38dB (sch.) HD3=50dB *(beh.)
ac (1V amp)	0.29s	0.09s	
noise	1s	0.1s	1/f noise estimate!

*: not perfect but not an ideal model either

**: significant speed gain (not even considering the actual design) BUT!...

Overview



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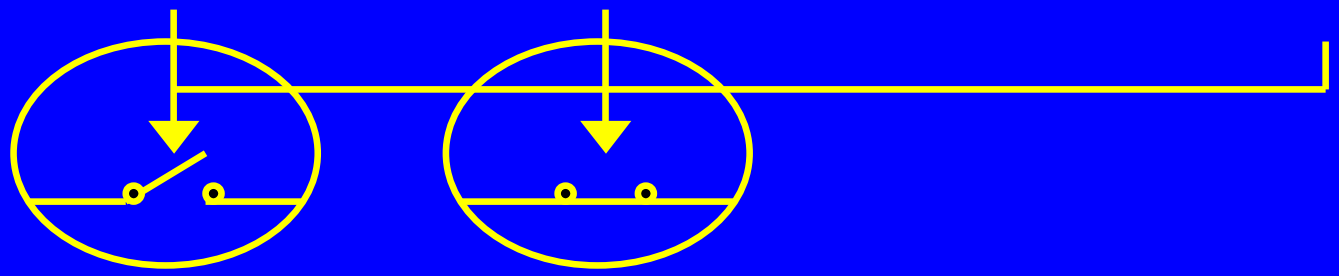
The switch

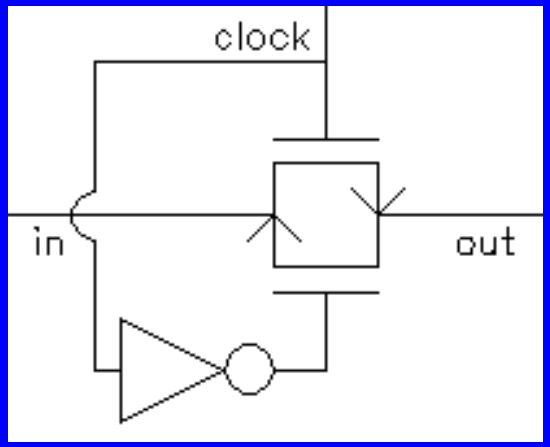
- **A switch is used in many analog and digital electronics**
  - sampling switch: memory cell, analog data acquisition, switched capacitor circuits
  - routing switch: control (AGC, logic, …)
- **The principle of operation of a switch is easy:**
  open or closed depending on a control signal

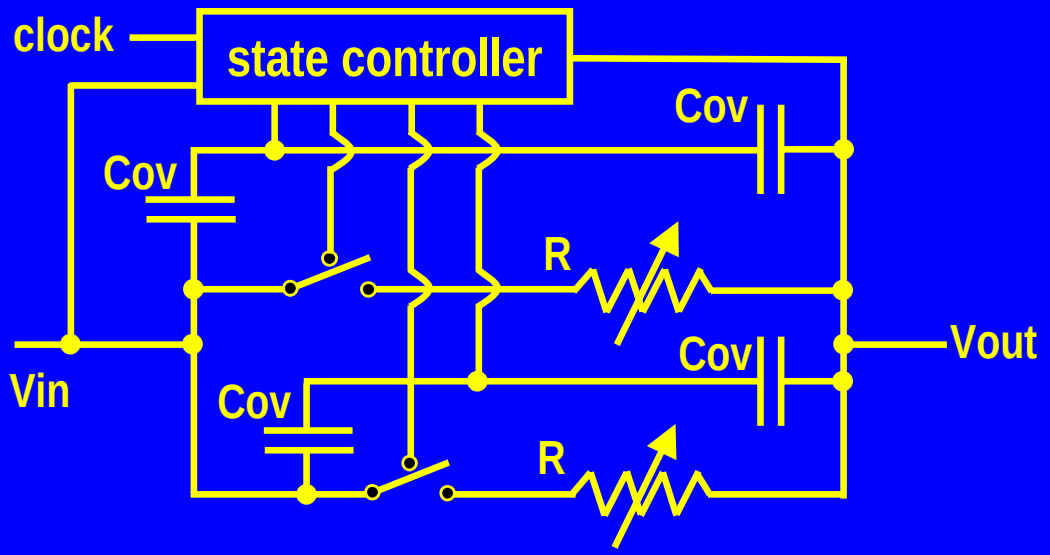


- **The Verilog-A model of an ideal switch is readily available from a multitude of sources**
- **Switch == transistor (passgate = nMOST and pMOST in //)**

Switch: model

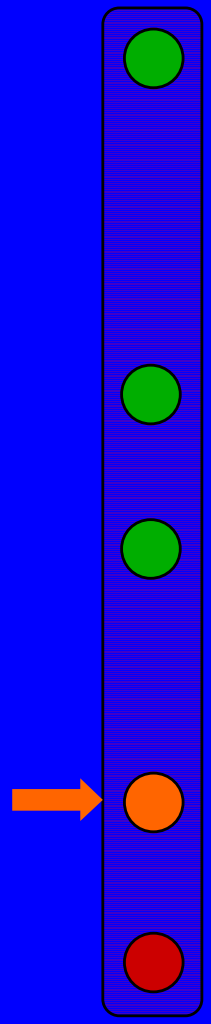
- feedthrough: overlap capacitance
- signal-dependent switching: no fixed threshold!
  - Example: sourceN=min(V(in,avss),V(out,avss))
- switch conductance: depending on the state of each transistor 0.0, $G_{SW,N}$, $G_{SW,P}$ or $G_{SW,N}+G_{SW,P}$





R = f(Vin, Vout, Vcontrol, techn.)

Overview



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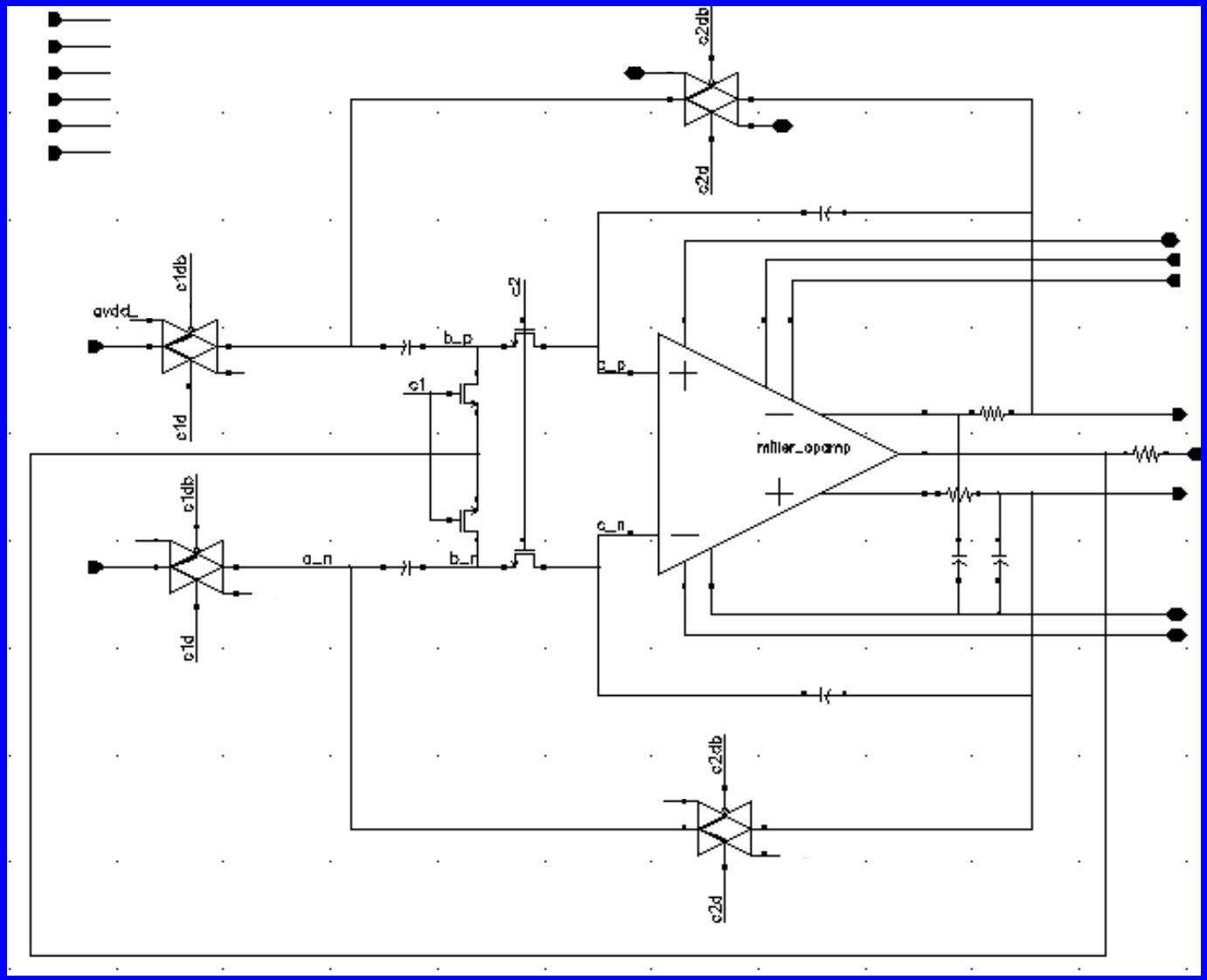
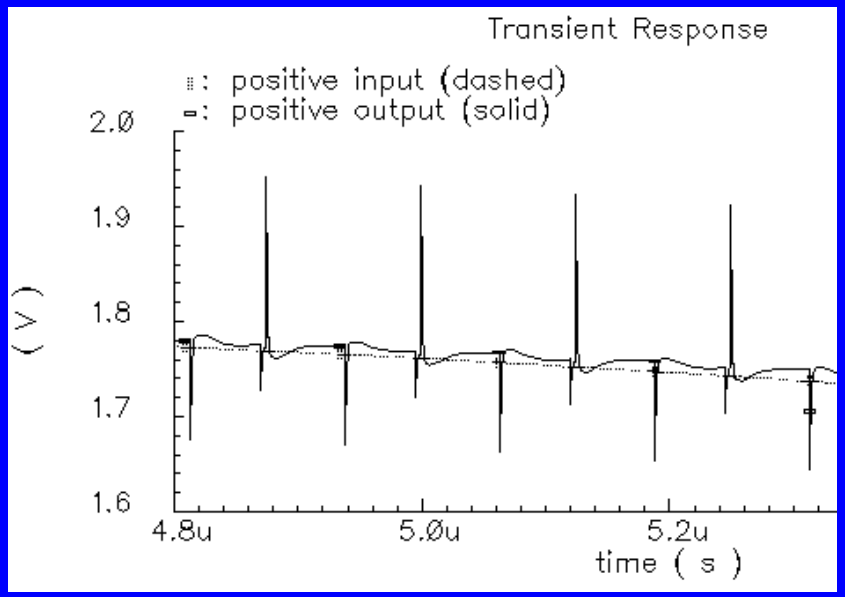
Switched capacitor LPF

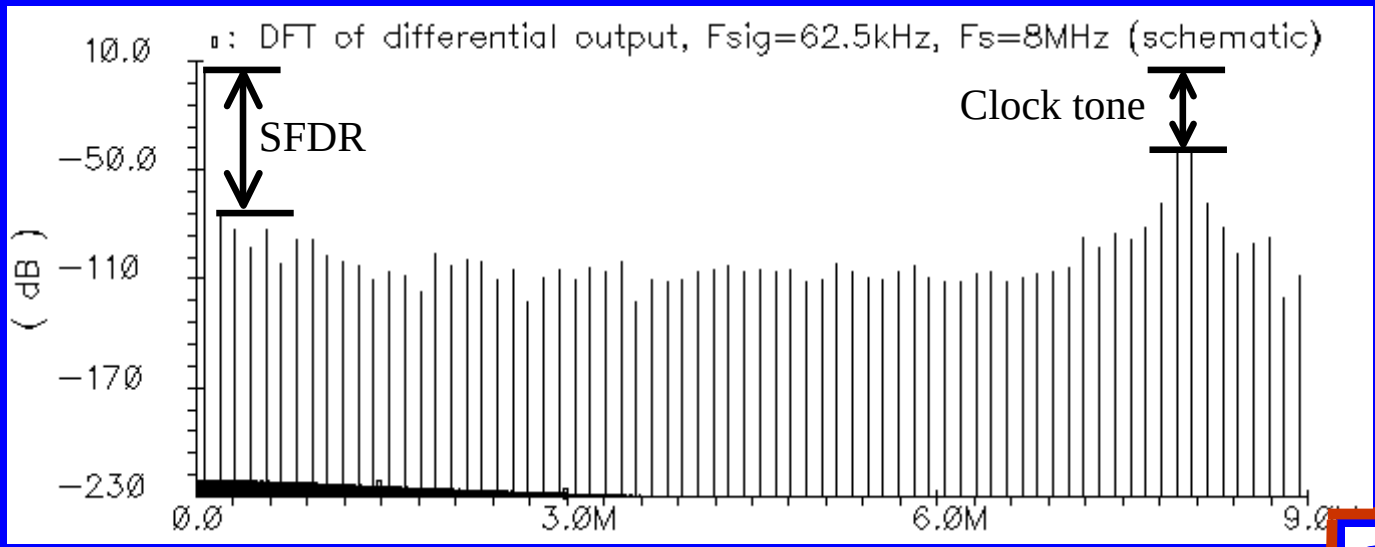


SCF simulations

- **Transient simulation result (full schematic)**
  - spikes on clock transitions
  - settling



- **DFT of the transient waveform (full schematic)**
  - SFDR
  - clock tone



SCF: interaction @ the boundaries

1: Spectre puts the model components in a matrix

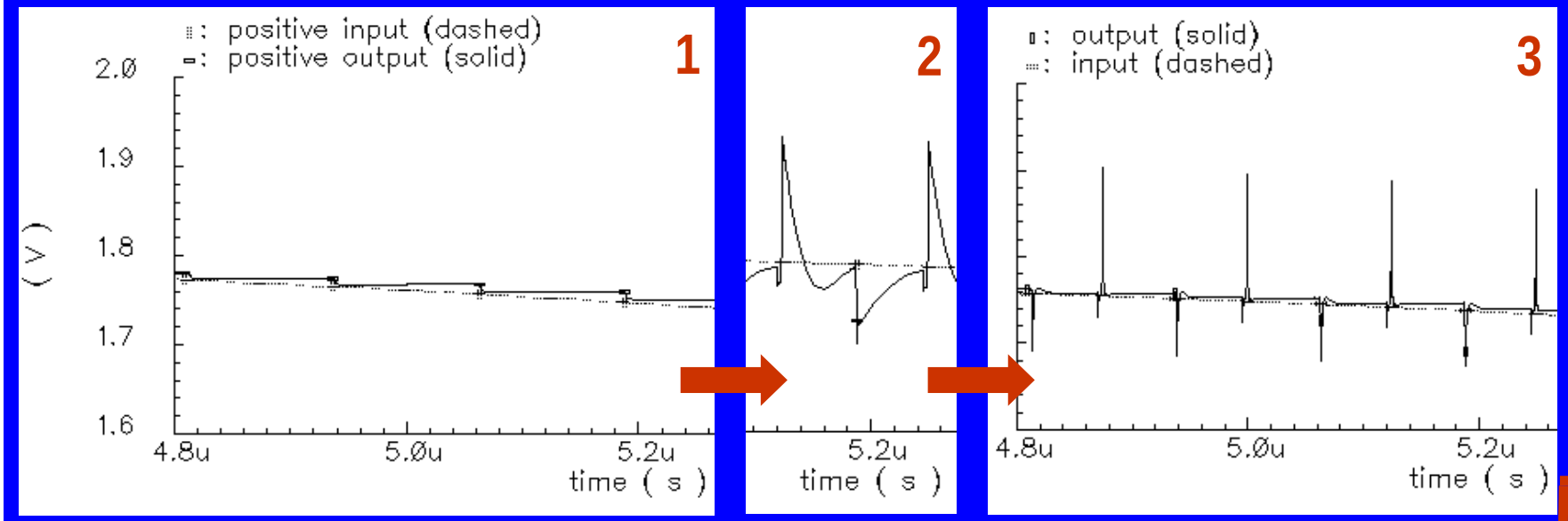
- No difference between model components and schematic components

2: Copy output VCVS (for clipping) to a VCCS and a resistor

- output voltage can vary now by added charges/current

3: Feed the disturbance back to internal node

- Model for common-mode feedback



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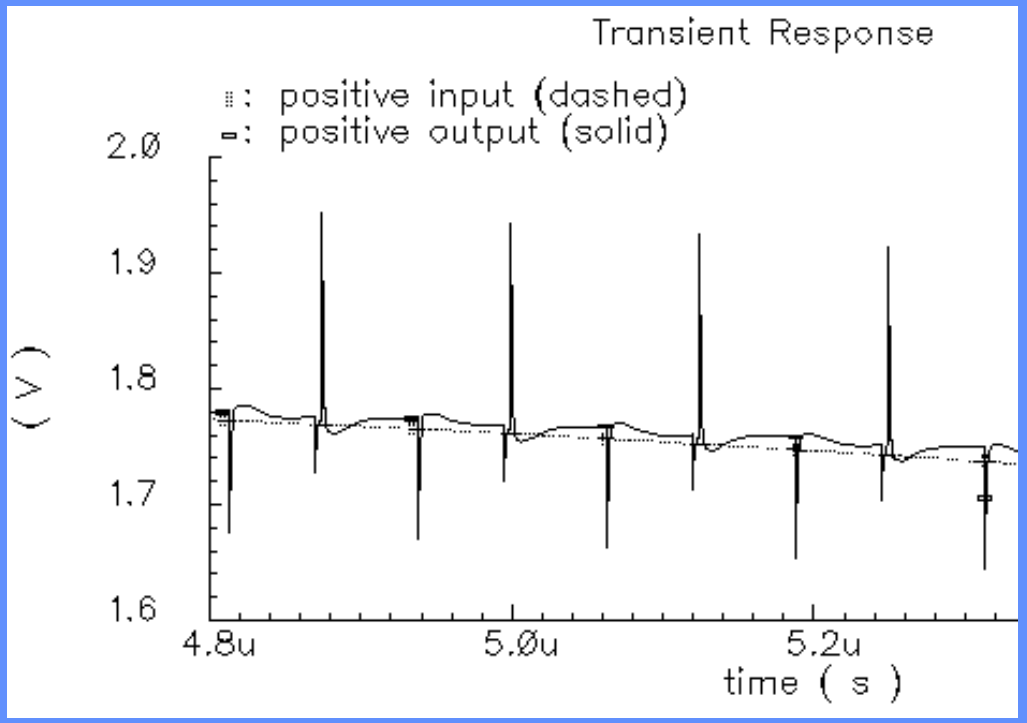
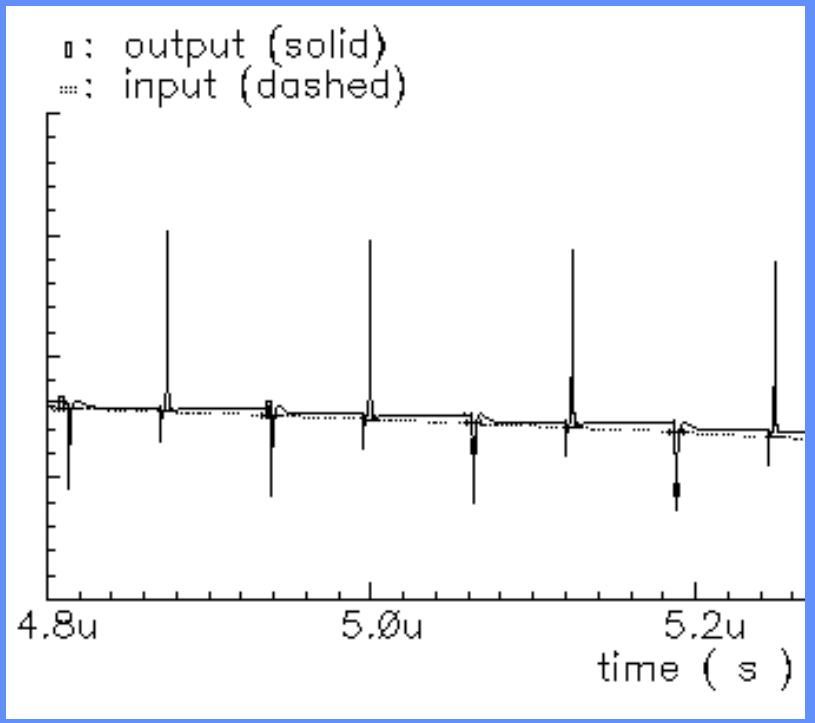
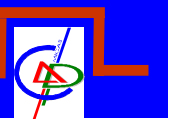




SCF simulations

Simulation results	SFDR [dB]	clocktone [dB]	relative simulation time
full schematic	75.9	42.0	100%
beh. opamp	80.0	41.2	84%
beh. Opamp&passg	72.3	42.1	164%
beh. Passgates	80.5	41.4	154%
full behavioral	71.7	41.2	169%

- Remember: design time, NOT simulation time!



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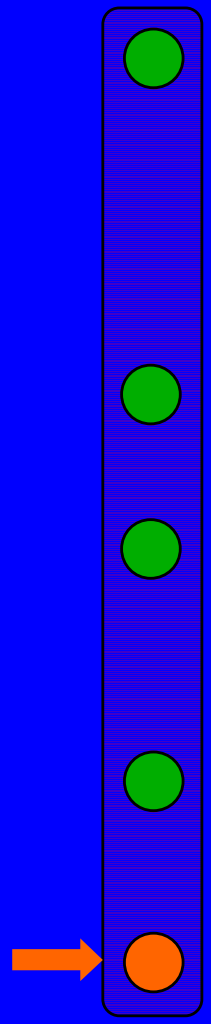

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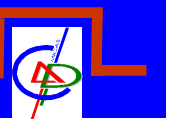
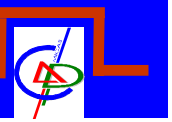
Summary: Verilog-A pittfals

- no local loops
- feedback slows down the simulation (if at all possible)
- copy with vcvs <--> see all the impedances
  → meet in the middle: vccs
- no discontinuities without transition or discontinuity statements BUT slows down
- if rigid branch of voltage sources in interconnection of behavioral models --> add 1 mΩ resistors
- for a switch sometimes direction does matter because of DC solution
- V(in,out) <+ 0.0; not equal to V(out) <+ V(in);



Conclusions

- behavioral models that are more than ideal
- limited set of high-level parameters: fast system design
- details can (often) be glued to the model at designer's taste
- results within 10% for first-order switched capacitor low-pass filter
- no gain in CPU time, but in design time
- no models without design understanding




Questions
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