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On Accommodating Particular Analog System Models With VHDL

Gabriel Stefan Popescu
Technical University of Iasi, Romania
E-mail: gpopescu@ieee.org

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Simulation Requirements

Speed - Accuracy Tradeoff

- Requirments
- To take into account performance limiting factors
  - To accurately represent the timing behavior of the modeled hardware
  - The analog behavior of the circuit - even for digital circuits.
- To reduce the costs of the simulation
  - To reduce the simulation time
  - To reduce the memory overhead
- To manage the simulation of huge simulated systems

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Interconnection Macromodels

Interconnections: A Limiting Factor of the Actual Circuit Performances

- Long line approximations:
  - Precise only for particular topologies.
- Precise models - use complex numeric processing:
  - Convolution,
  - Numerical inversion of the Laplace transform, etc.
- Reduced order approximations - less precise but less numerical intensive:
  - Padé like approximations (AWE, CFH),
  - Krylov subspace approximations (PVL).

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Simulation of High Speed VLSI Circuits

The Simulation Approach

- Classical simulators (SPICE):
  - Low level of model abstraction ÷ high precision.
  - The latency is not exploited ÷ high simulation cost.
- Discrete event simulators (VHDL):
  - High level of model abstraction ÷ low precision.
  - The latency is exploited ÷ low simulation cost.

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Simulation of High Speed VLSI Circuits

The Simulation Approach - An Insight Point of View

- Classical simulators (SPICE):
  - Solves numerically a set of nonlinear differential equations:
    - Establishes a discrete equivalent set of equations;
    - Solves at discrete moments of time a set of nonlinear equations:
      - Solves sets of linear equations - computes the terms of a string which eventually converges.
  - The concurrence of the circuit is established by solving a system of equations.
- Discrete event simulators (VHDL):
  - Solves numerically a set of linear decoupled equations - liniarization by abstraction:
    - Establishes a discrete-quantized set of equations;
    - Solves with respect of time the transitions between to states defined as amplitude vectors
  - The concurrence of the circuit is established using concurrent statements.

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On Some Event-Driven Aspects of VHDL

Predefined Discrete Event Features of VHDL

- The VHDL grammar proposes two syntactic constructs:
  - Inertial delay (digital devices such as gates, flip-flops, etc.):
    - A new input value must persist a minimum amount of time to initiate a change in the state of the component.
  - Transport delay (interconnections):
    - Any change of the input signal, regardless of its duration, initiates a change of the state of the device.
- The transport delay interconnection model assumes some serious limitation:
  - The interconnection has only one tap connected to a driver.
  - The signal is only delayed on the interconnection:
  - Old transactions that are to occur at, or after the time at which the earliest new transaction is projected are deleted from the event queue:
    - The energy of any signal can be vanished without any impact on the system behavior.

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The Proposed Approach

Features of the Model

- The targeted interaction between the macromodel and VHDL:
  - Avoid modifications in the VHDL standard,
  - Avoid limitations imposed to the modeled system.
- The interconnection macromodel is implemented as an *entity* that must satisfy two essential conditions:
  - The macromodel must be able to be activated by the input signals:
    - Initial activation - a consequence of the activity of one or more drivers connected at the interconnection taps.
  - The macromodel must have a mechanism to auto activate until it reaches a temporary steady state corresponding to the input and output signal's state:
    - Events are necessary to update the state of the interconnection during the propagation of the signals.

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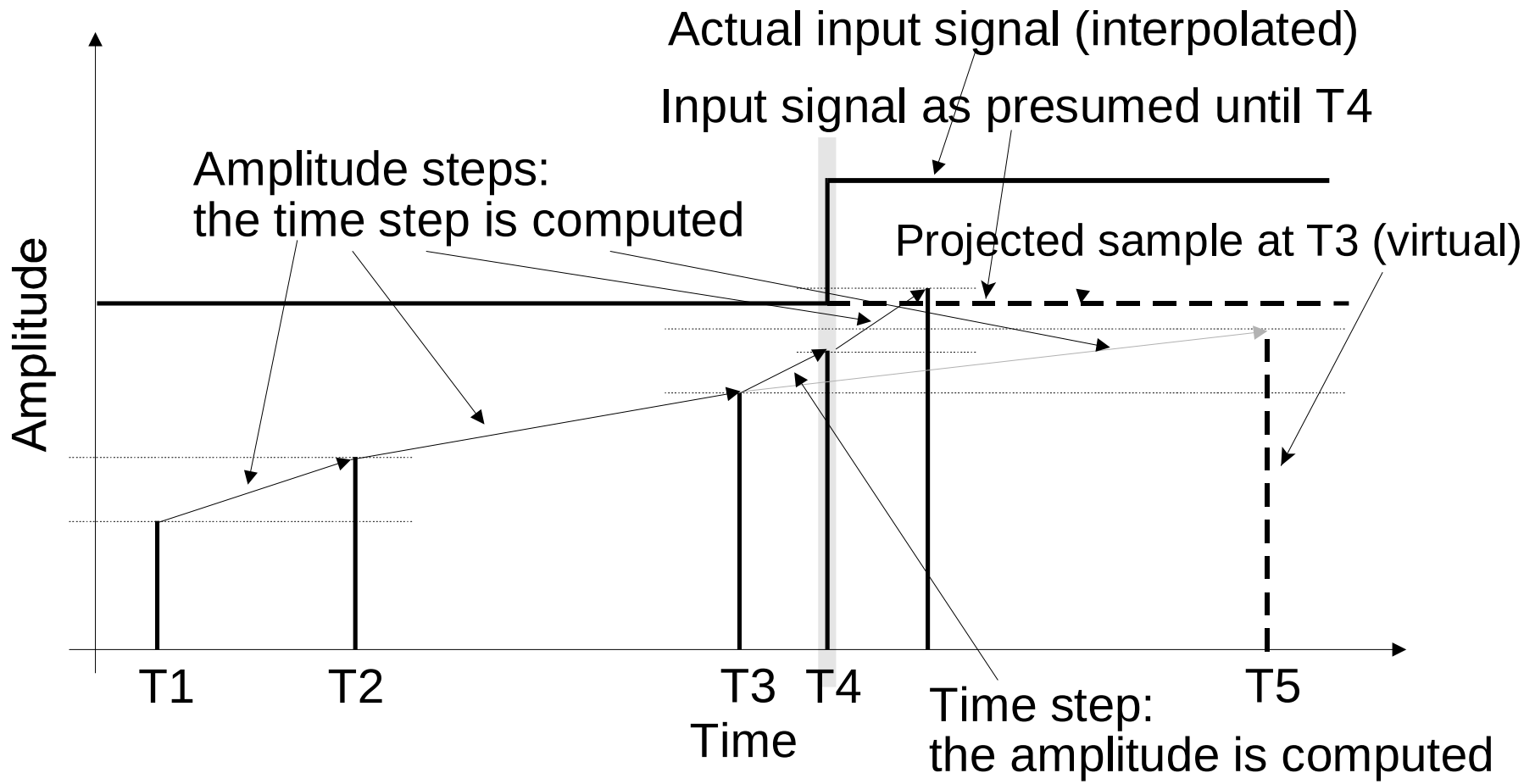
The Proposed Approach

The model development

- The definition of the events and their transactions for the analog system:
  - Discrete amplitude;
  - Discrete time.
- Intermediate layer - translation to the VHDL's events and their transactions:
  - The evolution of the system with constant imput values;
  - The synchronization due to the modifications of the input values.
- Implementation for VHDL

Example of event - transaction

P At the moment T4 an event occures on the input signal ÷ synchronisation.



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The analog system representation

- The hybrid representation for the N-port which represents the modeled system the in the frequency domain:

$$Y(s) = H(s)X(s)$$

$$Y_k(s) \;/\; \begin{cases} I_k(s) & when \quad X_k(s) \;/\; V_k(s) \\ V_k(s) & when \quad X_k(s) \;/\; I_k(s) \end{cases} \qquad k \;'\; 1, \ddot{y}, n$$

$$H_{pq} = K^{pq} + \sum_{i=1}^{m_1} \frac{k_i^{pq}}{(s + p_i)^{j_i^1}} + \sum_{i=m_1+1}^{m_1+m_2} \left(\frac{k_i^{pq}}{(s + p_i)^{j_i^2}} + \frac{k^{(}{}_i^{pq}}{(s + p^{(}{}_i)^{j_i^2}} \right)$$

- To accomplish equation decoupling - enabling milti rating integration:

$$Y_p = \sum_{q=1}^{n} Y_{pq}(s) = \sum_{q=1}^{n} \sum_{i=1}^{1+m_1+m_2} Y_{pq\,i}(s)$$

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Real Poles

- For the term:

$$Y_{pq\,i}(s) = \frac{k_i^{pq}}{s + p_i} X_q(s)$$

- The time domain equation is:

$$\begin{cases} \dfrac{d}{dt} y_{pq\,i} = \&p_i\, y_{pq\,i} + k_i^{pq}\, x_q \\ y(t_0) = y_0 \end{cases}$$

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Amplitude step:

< Evolution

$$t_{n+1} - t_n = \left[y_{pq\,i\,n+1} - \sum_{j=0}^{l} a_j y_{pq\,i\,n-j} \right] \left[\sum_{j=-1}^{l} b_j - p_i y_{pq\,i\,n-j} + k_i^{pq} x_{n-j} \right]^{-1}$$

Time step:

< Synchronisation

$$y_{pq\,i\,n+1} = \left[\sum_{j=0}^{l} a_j y_{pq\,i\,n-j} + (t_{n+1} - t_n) \sum_{j=0}^{l} b_j - p_i y_{pq\,i\,n-j} + k_i^{pq} x_{n-j} + (t_{n+1} - t_n) b_{-1} k_i^{pq} x_{n+1} \right]$$
$$(1 + (t_{n+1} - t_n) b_{-1} p_i)^{-1}$$

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Complex Poles

- For the term:

$$Y_{pq\,i}(s) = \left(\frac{k_i^{pq}}{s + p_i} + \frac{k(_i^{pq}}{s + p(_i} \right) X_q(s)$$

- Time step:
  - < Synchronisation

$$\begin{cases} \frac{d}{dt} y_{pq\,i\,1R} = \&p_{i\,R} y_{pq\,i\,1R} + p_{i\,I} y_{pq\,i\,1I} + k_{i\,R}^{pq} x_q \\ \frac{d}{dt} y_{pq\,i\,1I} = \&p_{i\,I} y_{pq\,i\,1R} - p_{i\,R} y_{pq\,i\,1I} + k_{i\,I}^{pq} x_q \\ y_{pq\,i\,1R}(t_0) = y_{pq\,i\,1R\,0} \\ y_{pq\,i\,1I}(t_0) = y_{pq\,i\,1I\,0} \\ y_{pq\,i} = 2\, y_{pq\,i\,1R} \end{cases}$$

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Amplitude discretization

- Too many steps reduce the simulation efficiency,
- Too few affect the accuracy of the simulation results.
- Assumptions.
  - Uniform discretization
  - The local steady state is given by the value zero of the derivative of the output when the input value is constant
  - M is the number of amplitude steps per input amplitude unit
- A real pole:

$$\Delta y_{pq\,i} = \left\lfloor \frac{k_i^{pq}}{M\,p_i} \right\rfloor$$

- A pair of complex poles:

$$\Delta y_{pq\,i\,1R} = \left\lfloor \frac{k_{i\,R}\,p_{i\,R} + k_{i\,I}\,p_{i\,I}}{M\,(p_{i\,R}^2 + p_{i\,I}^2)} \right\rfloor ; \quad \Delta y_{pq\,i\,1I} = \left\lfloor \frac{k_{i\,R}\,p_{i\,R} - k_{i\,I}\,p_{i\,I}}{M\,(p_{i\,R}^2 + p_{i\,I}^2)} \right\rfloor$$

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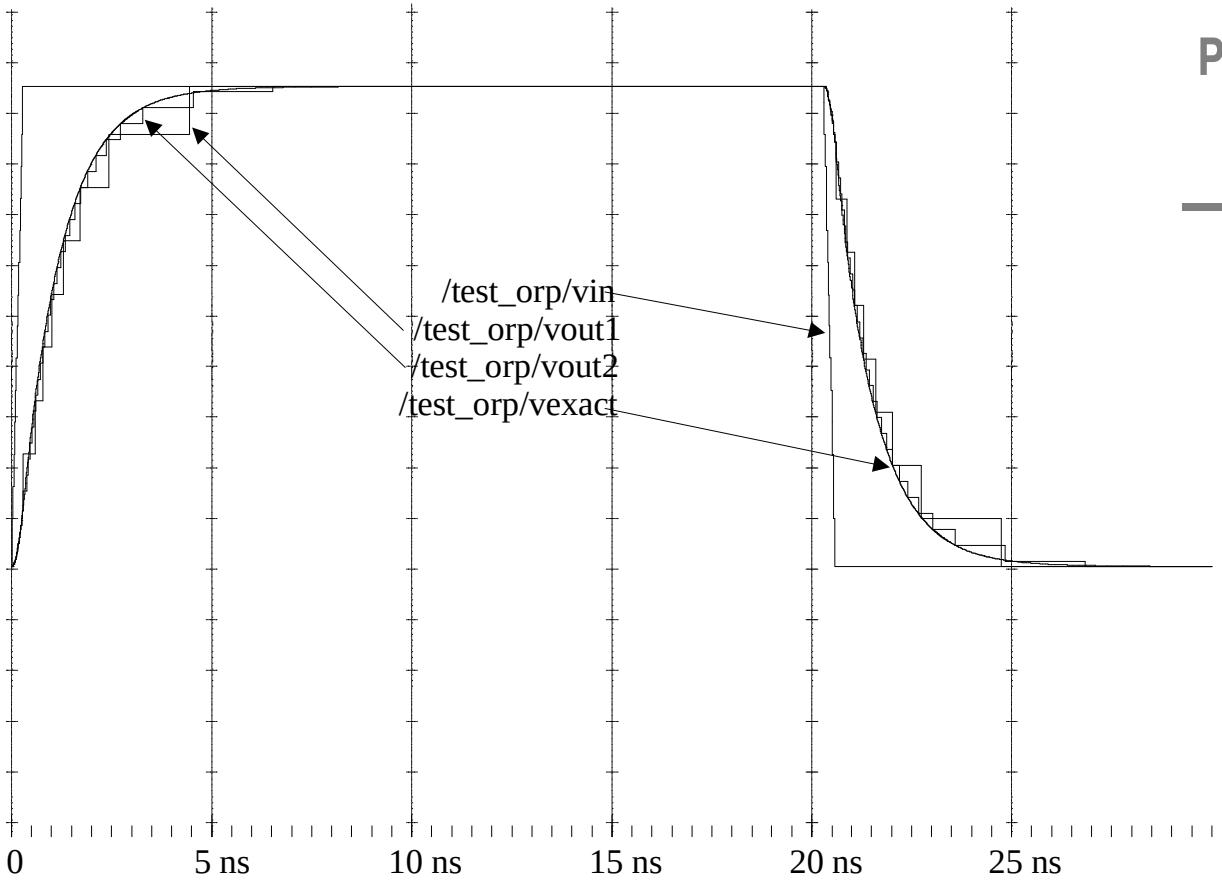
Experimental results



- Input siganl - vin
- Output signal vout
  - vout1 : M = 3
  - vout2 : M = 10

- One real pole

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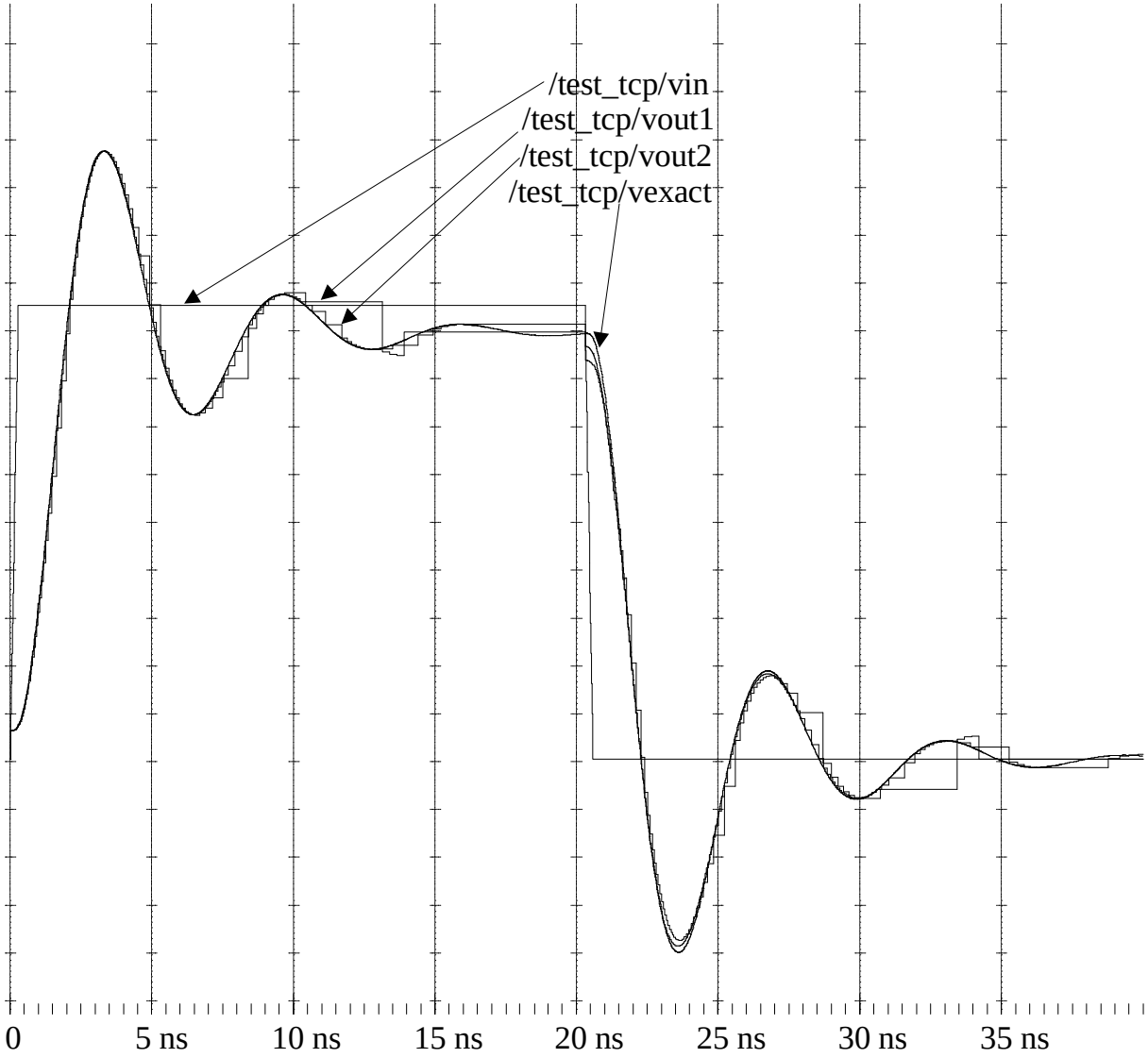

- Input siganl - vin
- Output signal vout
  - vout1 : M = 3
  - vout2 : M = 10

- Complex poles

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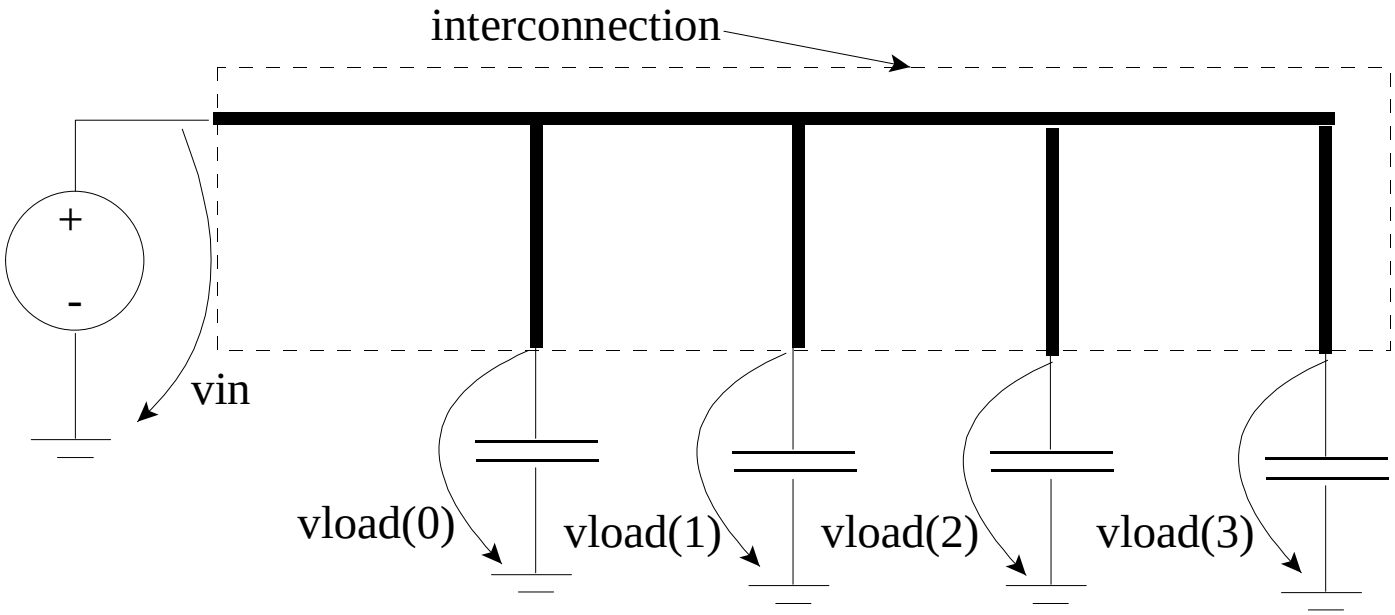

P The topology of a test interconnection.

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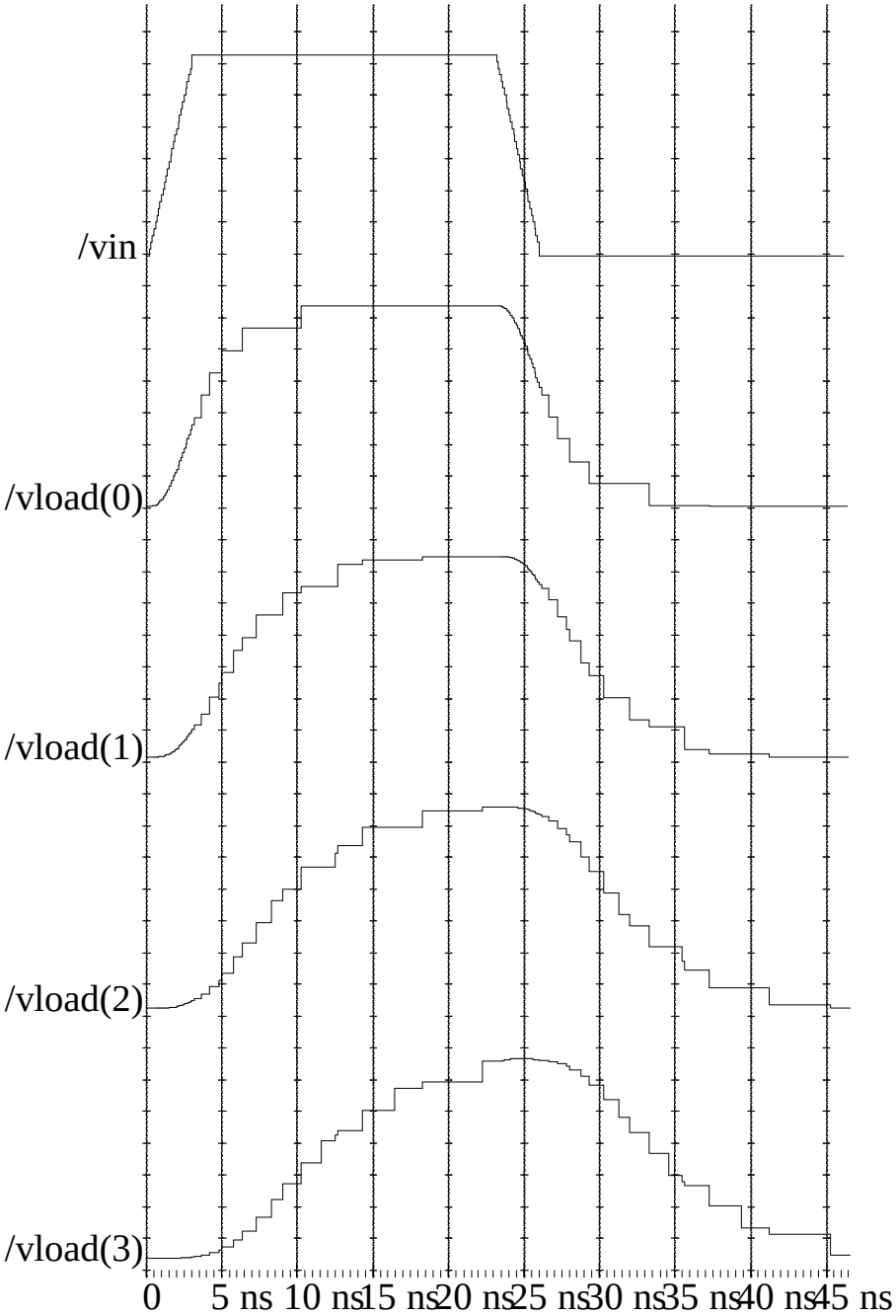

- Simulation results for a interconnection modeled using real poles

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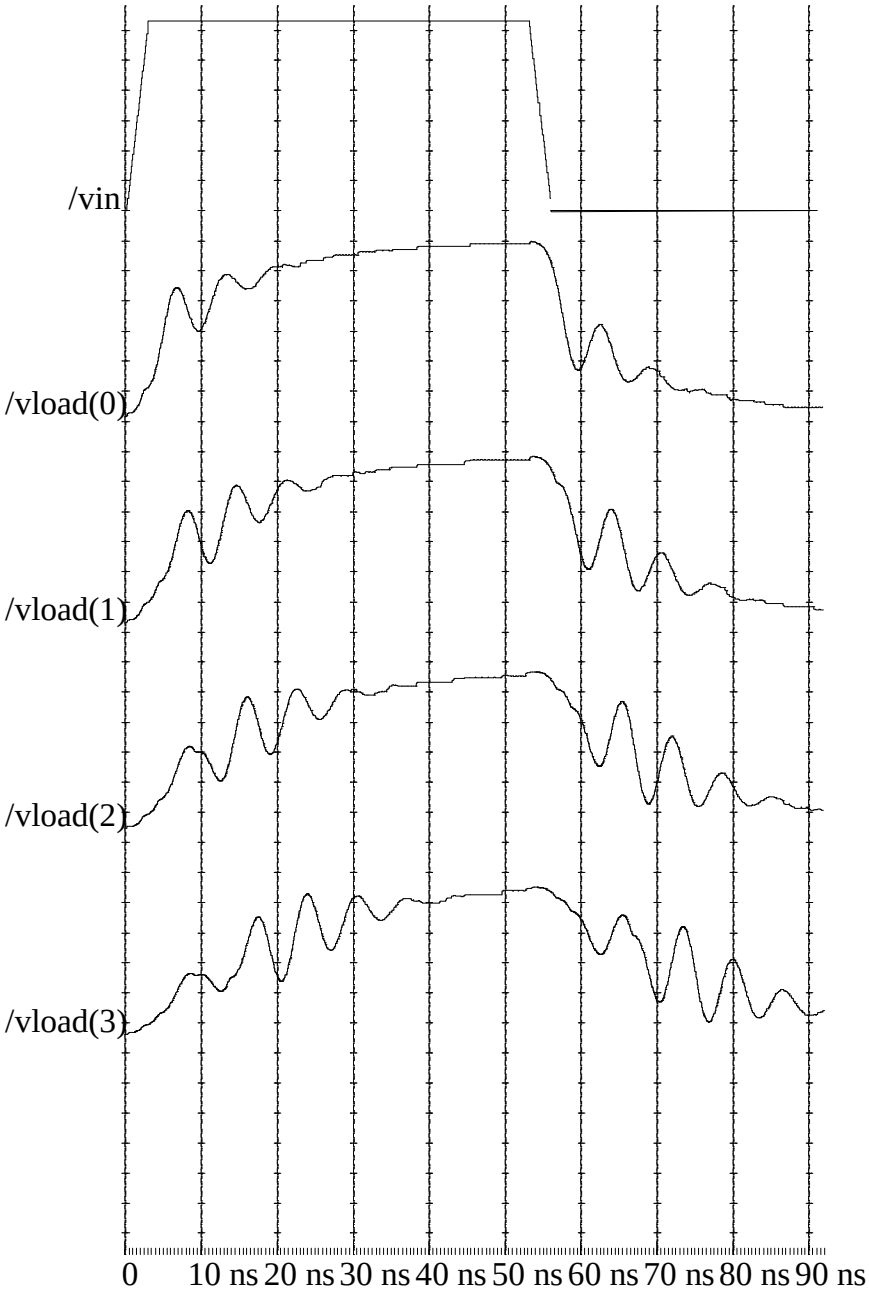

- Simulation results for a interconnection modeled using both real and complex poles

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Conclusions

- The paper discusses the development of a VHDL analog system modeling approach with applications in interconnections' modeling.
- The method is based on a multi rate integration approach derived from an implicit integration algorithm exhibiting:
  - Latency exploitation;
  - Superior stability properties of implicit integration methods.
- The modeling process uses available VHDL constructions.
- An extra layer of the model adapt the set of events and their transaction imposed by the analog stage to the discrete event approach used by the discrete event simulator. In this layer tow kind of iterations are used:
  - Amplitude step - evolution
  - Time step - synchronization.
- The obtained modeling solution is able to represent analog behavior including crosstalk and non monotonic transitions.
- It is usable only into a particular simulation scenario mainly when the analog stage of the circuit is represented by nonideal interconnections.