A VHDL-AMS Library of RF Blocks Models

N. MILET-LEWIS, G. MONNERIE, A. FAKHFAKH, D. GEOFFROY, Y. HERVE [*], H. LEVI, J-J. CHARLOT [**]
IXL laboratory - Bordeaux 1 University, 351 cours de la Libération, 33405 Talence Cedex, France
tel : (33) 5 56 84 27 66, fax : (33) 5 56 37 15 45
e.mail : milet@ixl.u-bordeaux.fr
[*] ENSPS – ERM/PHASE, Pôle API, bd S. Brait, 67400 Illkirch, France
[**] ENST, 46 rue Barrault, 75634 Paris Cedex 13, France

Abstract

This paper presents a behavioral model library of analogue and mixed circuits used in the radio-frequency domain. The models are described in VHDL-AMS and are carefully documented and validated, in order to be easily used by designers or model developers. These models allows to explore systems architecture easily and rapidly.

Keywords

Behavioral Modeling, VHDL-AMS, Radio-Frequency Systems, Model Library, Mixed-Signal.

1. Introduction

With growing circuit integration, tomorrow's challenge of Microelectronics is the SOC (System On Chip). Such complex, mixed-signal and mixed-technology circuits impose to reconsider traditional design methods. Hierarchical design (Top-Down, Bottom-Up) and design re-use represent some solutions. Behavioral modeling is one key, to explore high-level architecture possibilities. Standard description languages for analogue and mixed circuits, like VHDL-AMS [1], and compatible mixed simulators offer now the required tools to develop this new design methodology.

The first issue is to develop behavioral models libraries that will be available in the design flow. This paper presents a VHDL-AMS library of analogue and mixed circuits used to simulate radio-frequency (RF) systems. All models have been elaborated and simulated with ADVanceMS software [2]. Our priorities wasn't only the models performances but also the models documentation and validation, which are the minimum requirements for a correct using.

2. Library description

2.1. Library contents

At the present time, our models are organized in three libraries : passives components, sources, RF components. The content of RF library is detailed in Table 1.

All fundamental blocks for frequency synthesis are present ; various structures from classical Phase-Locked-Loop (PLL) to fractional frequency synthesizer can be simulated. As phase noise is a critical parameter in such applications, we propose a modeling approach of jitter in oscillators [3]. Theoretical relations between phase noise in the frequency domain and jitter estimation are exploited, then jitter is introduced in oscillator models with a random generator. This characteristic appears in the synchronous oscillator model [4]. The second column of Table 1 indicates the model description level which is either purely behavioral or structural. In the structural description, behavioral models are instantiated and connected together.

2.2. Digital or analog approach

As RF oscillators are often based on square waves, two description modes are possible for the input and/or output signals of each PLL blocks. In VHDL-AMS, it corresponds to a bit digital signal or an analog electrical terminal. During simulation, digital signals call the digital event-driven kernel while analog terminals call the analog continuous-time kernel. The advantage of event-driven simulation is the reduction of CPU time, but the settling time of any transition can only be modeled with analog electrical terminal. For these reasons, each blocks of our RF

library has two interface descriptions : one entire analog and one digital/mixed using bit signals anywhere it is possible (Table 1). In fact, in a PLL architecture, only the loop filter requires analog input and output ; others blocks can have a purely digital or a mixed interface.

Model name	Description level	Interface description
Phase-Frequency Detector (PFD)	Behavioral	Analog or Digital
Charge Pump (CP)	Behavioral	Analog or Mixed
Loop Filter (LF)	Behavioral	Analog
Voltage-Controlled Oscillator (VCO)	Behavioral	Analog or Mixed
Frequency Divider N (FD_N)	Behavioral	Analog or Digital
Frequency Divider N or N+I (FD_N_N+I)	Behavioral	Analog or Digital
ACCumulator (ACC)	Behavioral	Analog or Digital
Phase-Locked-Loop (PLL)	Structural (PFD + CP + LP + VCO + FD_N)	Analog or Mixed
Fractional Phase-Locked-Loop (FPLL)	Structural (PFD + CP + LP + VCO + ACC + FD_N_N+I)	Analog or Mixed
Synchronous Oscillator (SO)	Behavioral	Analog

Table 1 : RF library content

2.3. Model example

Figure 1 and 2 illustrate, on an simple frequency divider model, what are the differences between an analog and a digital interface description. Each difference appears in bold characters.

```
edge : PROCESS
BEGIN
wait until Vin'above(Vthreshold);
counter <= counter + 1.0;c
if (counter<divisor*(1.0 - cyclic_ratio)) then between <= Vlow;
                                          else between <= Vhigh;
end if;

if (divisor<counter+2.0) then counter <= 0.0;
end if;

END PROCESS edge;

Vout == between'ramp(trise,tfall);
```

Figure 1 : Frequency divider model with analog interface

```
edge : PROCESS(input)
BEGIN
counter <= counter + 1.0;

if (counter<divisor*(1.0-cyclic_ratio))      then output <= '0';
                                             else output <= '1';
end if;

if (2.0*(divisor-1.0)<counter)
then counter <= 0.0;
end if;

END PROCESS edge;
```

Figure 2 : Frequency divider model with digital interface

2.4. Models documentation and validation

A special effort has been made in the purpose that all models could be understood and simulated by future users. First, each VHDL-AMS source file is precisely documented by the author. Then this model file is attached to a simulation file which describes a typical test-bench for the circuit. As a complement, the curves resulting from this typical simulation are given in a graphic file. Hence, one can have a precise idea of the circuit functionality, without performing model compilation and simulation.

For the model validation, the author compares first the model behavior with transistor-level simulations or test results. Then, the whole package {model file, test-bench file, simulation curves} is studied by another user, which criticizes the documentation and submit the model to various types of simulations. If needed, the author generates one or several improved versions of the model. At this step only, the model and its attached files are considered to be available.

3. Some simulation results

As an example, a frequency synthesizer has been simulated which corresponds to the UMTS2000 specifications : a frequency band from 1,92 GHz to 1,98 GHz with 12 channels to synthesize. This frequency synthesizer is composed of a fractional PLL (FPLL) which drives a synchronous oscillator (SO). The SO multiplies the PLL output frequency by 6. The PLL structure is depicted on Figure 3 ; each block comes from the VHDL-AMS library.

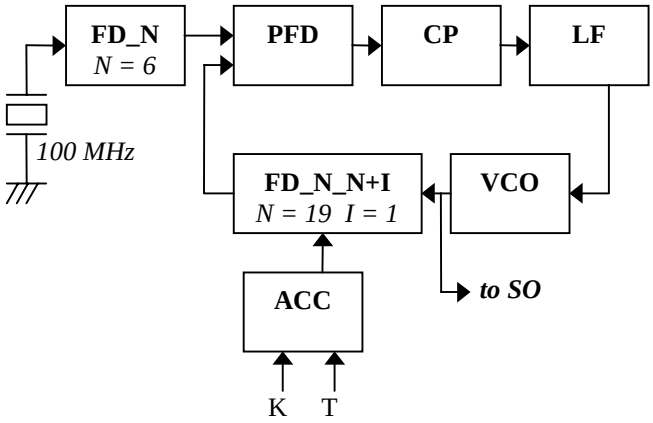

Figure 3 : Fractional PLL structure

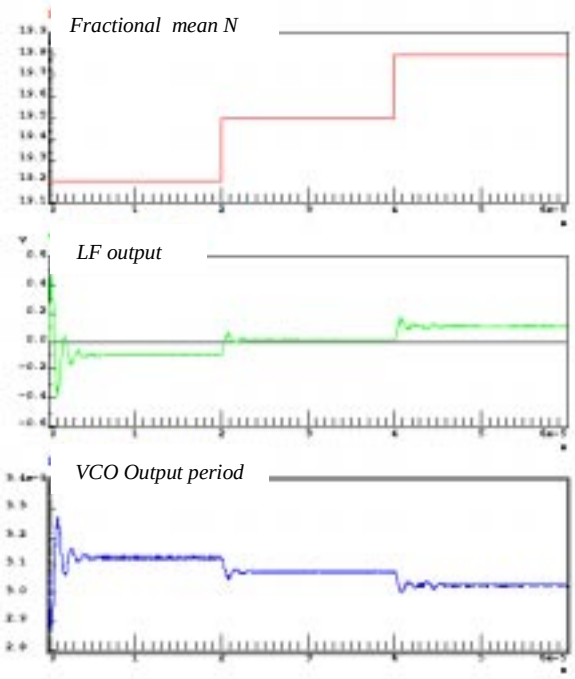

Figure 4 : PLL simulation results

Figure 4 shows some simulation results. The K parameter permits to select the PLL output frequency ; this parameter is varied as a stimulus. The first curve shows the variation of the mean ratio of fractional division, which linearly depends on K. The second curve represents the filter output reaction and the last curve the output period of the PLL. This simulation was performed over 60 µs which corresponds about to 120000 output periods.

Analog or mixed descriptions give very similar results, as the modeling method does not differ more than the port description and process synchronization. The CPU time is 13 min for the analog description and only 12 s for the digital/mixed description. Simulations were performed on a E220R sun server.

4. Conclusion

The circuits and systems designers encounter even more needs in behavioral modeling. Available model libraries are today often incomplete or insufficiently documented. That is why we propose an open VHDL-AMS library which is today composed of passives components, sources and RF components. Each model is carefully documented and validated by the author and other users. Some model performances have been shown, especially in the domain of frequency synthesizer simulation. Different architectures may be explored easily and rapidly as a typical simulation has a mean duration of ten seconds.

This library is really open for several reasons. We will always enlarge and improve it, in the RF application domain but also in other domains of microelectronics including multi-technological aspects. Further more, all models will be soon entirely public, available on BEAMS web site [5].

References

[1] : IEEE Standard VHDL Analog and Mixed-Signal Extensions, IEEE Std 1076.1 – 1999.

[2] : ADVance MS reference manual, Mentor Graphics, 2000.

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[4] : A. Fakhfakh, N. Milet-Lewis, J-B. Beguret, H. Lévi, *VHDL-AMS Model of a Synchronous Oscillator including Phase Noise*, FDL'2001, September 2001, Lyon - France.

[5] : BEAMS, Behavioural modelling of Analogue and Mixed Systems, a non-lucrative association for the promotion of behavioural modelling and simulation with HDL languages (mainly VHDL-AMS), http : //www.beams.asso.fr