Remove Model Implementation Bottleneck

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Model is One of The Keys for Simulation Accuracy

• SPICE consists of numerical algorithms to solve nonlinear differential equations that characterize analog circuits that are represented by interconnections and device models
  – Approximately 50 transistor device models supported today
  – Some hundreds of various passive components models are implemented natively or through Verilog-A
  – Major source of quality issues with ANY simulator (second to Parser)
  – Typically implement 3 models every year plus various updates
    – BSIM versions, Philips MOS9, VBIC, SOI …
Model Implementation

• Simulator vendors do not develop device models in general
  – Easier to support
  – Different expertise for model development
  – Lack of technology excess

• Models are (re)implemented in SPICE by hand
  – Derivate expressions need to be calculated manually
  – Difficult to capture errors and bugs
    – Parameter clamping; calculation efficiency
  – 3-6 man-months of implementation effort
  – Often public domain code is not in commercial quality
Simulator Vendors Are the Bottleneck for New Model Trial

• Model developers can not add model feature freely
  – Each revision takes 3-6 months to the hands of designers
• Different vendors have different tricks/standard for model implementation
  – Standardized model often does not behave the same
• Many proprietary model implementation interfaces
  – Sharp learning curve, required extensive simulator knowledge to make the implementation work correctly
Model compiler to Remove This Bottleneck

• Verilog-A language is powerful enough to allow device models to be described and proto-typed completely
  – Speed is the major limitation

• A model compiler will remove the speed limitation
  – Automatically calculates derivatives
  – Bug free by construction
  – Model developers can have a common interface