VHDL-AMS implementation

ENTITY material IS
  GENERIC (Ta: REAL);
  PORT (TERMINAL t1,t2: THERMAL);
END;

ARCHITECTURE behav OF material IS
  QUANTITY t_1 ACROSS h_1 THROUGH t1 TO thermal_ground;
  QUANTITY t_2 ACROSS h_2 THROUGH t2 TO thermal_ground;
  CONSTANT k     : REAL := 1.412;
  CONSTANT dy    : REAL := Height/(M-1.0);
  QUANTITY PkA1, PkA2: REAL;
  QUANTITY T11, T12, ... T104, T105:REAL;
BEGIN
  BREAK T11 => Ta;
  .......
END;