Abstract:
In this work we describe the digital kernel implementation of the simulator S.A.M.S.A., a tool for the simulation of VHDL-AMS systems in Matlab\textsuperscript{TM}. The digital kernel was validated by simulating different systems. In particular we will show the simulation of a low-power multistage decimator for a $\Delta$-Σ wideband Analog to Digital Converter (ADC). This example was correctly simulated given the same results as other VHDL commercial tools.

Example: low power multistage decimator

The proposed example is the VHDL implementation of a low-power multistage decimator for a wideband $\Delta$-Σ analog to digital converter (ADC). More exactly, the output of a 2-bit 2nd order $\Delta$-Σ Modulator (DSM) with optimized Noise Transfer Function (NTF) is supposed to be sampled at $F_s=320\text{MHz}$ having an oversampling ratio $OSR=F_s/2\times B=18.82$ where $B=8.5\text{MHz}$ is the baseband frequency of the signal of interest (like could be for example an OFDM signal in the standard IEEE802.11). The simulated decimator down-samples the output of the converter to 20Ms/s applying a decimation factor of $M=16$ and meeting requirements like almost same SNR at the output of the decimator as in input (SNR=80[dB] or 10 equivalent bits), low power consumption (less than 10mW) and latency delay less than 1μs.