

Modeling Thermal Induced Inter-Symbol Interference of Feedback Digital to Analog Converters in Delta-Sigma Modulators

Rahul Shringarpure¹, Todd Kaplan¹, George Valley², Peter Petre¹, John Visser¹

1. HRL LLC, Malibu, CA 90265

2. The Aerospace Corporation, El Segundo, CA 90245

Abstract

We propose a method to model inter-symbol interference due to temperature mismatch in the transistors of a 1-bit digital to analog converter (DAC) which is used to feedback the quantizer output in a 2nd order continuous time delta-sigma (CT $\Delta\Sigma$) modulator. The degradation in the signal to noise ratio (SNR) with thermal induced inter-symbol interference is reported. The phenomenon is modeled with Verilog-A, and simulated using the Cadence Spectre circuit simulator. The model provides device designers with insight into device behavior which affect circuit and system performance.

Introduction

Although the theoretical understanding of mixed-signal circuits has improved greatly in the last ten years, the real challenge on how to propagate the detailed physics captured at the process/atomic level to a higher level of abstraction still remains a challenge [1]. Thermal induced inter-symbol interference is a phenomenon in which two complementary input signals with a certain rise and fall time enter a differential pair of transistors with unequal temperatures, leading to a shift in the switching voltage. The voltage shift results in an inter-symbol interference which can seriously degrade the SNR in a DAC, when used in delta-sigma modulator circuits.

Several approaches to model temperature dependence of DC and RF characteristics of HBTs have been proposed [2-4] and implemented inside SPICE based circuit simulators. However effects such as thermal induced inter-symbol interference, which depend on the pattern or history of the input, are difficult to model with equivalent circuit components. Behavioral modeling tools such as Verilog-A and VHDL-A allow one to embed non-idealities in circuit components using mathematical equations. The proposed model uses a Verilog-A sub-circuit around a Gummel-Poon BJT. The 2nd order delta-sigma modulator circuit with the Verilog-A based model is simulated using Cadence's Spectre simulator.

Thermal Induced Inter-Symbol Interference

Thermal induced inter-symbol Interference is caused by the following phenomenon: two differential signals are entering a transistor pair causing the output to switch back and forth as in fig. 1. If the signal into transistor Q_1 switches to high and the signal into Q_2 switches to low, then Q_1 conducts current and Q_2 does not. This causes transistor Q_1 to heat up, and transistor Q_2 to cool down. The next time the signal switches, Q_1 is hotter than Q_2 . When a transistor heats up, it needs less of an input voltage to turn on than if it was cool. This means that

the input signal to Q_1 must go lower to turn Q_1 OFF, and, by contrast, the signal to Q_2 must go higher to turn Q_2 ON based on the input signals. Because of this, the new switching time is Δt later than it would be if the transistors had equal temperature.

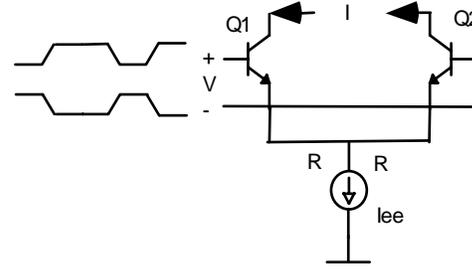


Fig. 1: Current Controlled DAC.

Δt is assumed to be inversely proportional to the slope of the input signal (i.e. $1/m$) as shown in fig. 2. If the slope is perfectly vertical, then $\Delta t = 0$, regardless of the temperature difference. If the slope is gradual then Δt would become more sensitive to the transistor temperature differences. We now derive the equation to show the dependence of Δt on the temperature difference.

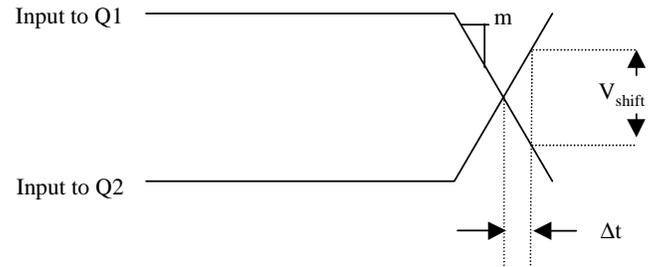


Fig. 2: Differential DAC Input

If T_H is the equilibrium temperature when the transistor in a differential pair is ON and T_L is the equilibrium temperature when the transistor is OFF, then $T(n)$, the temperature of a transistor Q at the n^{th} clock pulse is given by

$$T(n) = T(n-1) + [T_H - T(n-1)](1 - e^{-P/\tau}) \quad (1)$$

For an ON transistor and

$$T(n) = T(n-1) + [T_L - T(n-1)](1 - e^{-P/\tau}) \quad (2)$$

For an OFF transistor, where P is the clock period and τ is the thermal time constant.

Using $T_0 = (T_H + T_L)/2$, $\Delta T = (T_H - T_L)/2$. We can write simplified equations for the differential pair from fig. 1

For the ON transistor Q_1

$$T_1(n) = e^{-P/\tau} T_1(n-1) + T_0(1 - e^{-P/\tau}) + \Delta T(1 - e^{-P/\tau}) |v(n-1)| \quad (3)$$

and, for **OFF** transistor Q_2

$$T_2(n) = e^{-P/\tau} T_2(n-1) + T_0(1 - e^{-P/\tau}) - \Delta T(1 - e^{-P/\tau}) |v(n-1)| \quad (4)$$

where $v(n)$ is ± 1 .

Using the base-emitter turn-on voltage versus temperature characteristics from [2], we have come up with a relation as follows:

$$c = \frac{\partial V_{be}}{\partial T} = \frac{V_{be}(n) - V_{be}(0)}{T(n) - T_0} \quad (5)$$

Here, c is the rate of change of base-emitter voltage with device temperature ($mV/^\circ C$) and is $1.11mV/^\circ C$ for the transistor models used.

At the point where the DAC switches, $I_1 = I_2 = I_{ee}/2$,

$$V_{shift}(n) = V_{be1}(n) - V_{be2}(n) = c(T_1(n) - T_2(n)) \quad (6)$$

where $T_1(n)$ and $T_2(n)$ are the device temperature of transistors Q_1 and Q_2 .

Finally, from Eq.6 and fig. 2 we find

$$\Delta t(n) = \frac{V_{shift}(n)}{2m} \quad (7)$$

To model thermal induced inter-symbol interference, one needs to change the Physical attributes of the transistor (Example: saturation current) at every clock cycle. Dynamically changing a physical model in a SPICE based simulator is currently not possible; instead, we model this effect with a perturbation voltage at the base of the transistor. We assume a simplified transistor model with

$$V_{be0} = V_{T0} \ln\left(\frac{I_0}{I_s}\right) \quad (8)$$

where, V_{be0} is the base-emitter voltage and V_{T0} is the thermal voltage at T_0 . Therefore from Eq.6,

$$\Delta V = V_{beT}(t) - V_{be0} = c(T(t) - T_0) \quad (9)$$

where, ΔV is the perturbation voltage added to the base of the DAC transistors.

Eq. 9 is modeled using Verilog-A and was simulated in Cadence Spectre simulator. The Verilog-A code is listed in the Appendix.

Application

To test the above model, we have chosen a 2nd order continuous time sigma delta modulator [5].

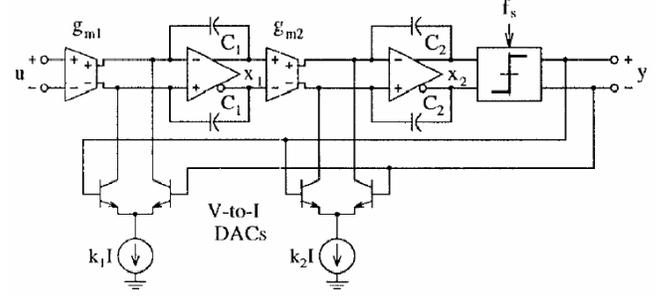


Fig 4: 2nd Order Continuous Time $\Delta\Sigma$ modulator

To isolate the effect of thermal induced inter-symbol interference, we modify the DAC portion of the above circuit and use idealized models for the Gm-Cell and Integrator. The Verilog-A model is wrapped around a bipolar transistor in the DAC and senses the input voltage to the transistor. Fig. 6 shows the CT $\Delta\Sigma$ modulator with Verilog-A model inside Cadence Affirma Analog Artist environment.

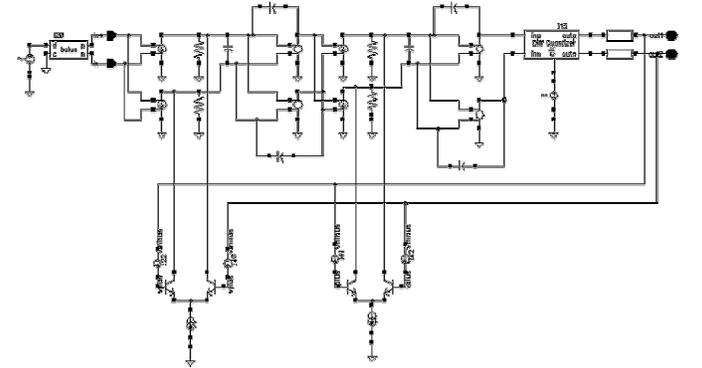


Fig 5: 2nd Order Continuous Time $\Delta\Sigma$ modulator with the thermal induced ISI Verilog-A model

Table 1: Parameters for 2nd Order CT $\Delta\Sigma$ modulator

G_{m1}	500uA/V	G_{m2}	500uA/V
$C1$	2pF	$C2$	2pF
K_1	2.13mA	K_2	1.34mA
(sampling freq) f_s	1 GHz	(input freq) f_{in}	5MHz

The differential quantizer used is modeled in Verilog-A. Using the “*transition*” function in Verilog-A, rise and fall time of the quantizer output is specified. The slew of the quantizer output is critical because it affects the slope (i.e. m) in the DAC input signal and is related to shift in the switching time (i.e. Δt) The Verilog-A code for the quantizer is listed in the Appendix

Results

According to [2], an SHBT device has a thermal resistance of 12.3C/mW. However, transistors in a DAC are differential, and closely spaced. This means that when one transistor in the DAC heats up, a transistor in close proximity cools down. The substrate is much thicker (about 100 microns) than the distance between the two transistors (about 5 microns) which means that the thermal resistance for our purposes is actually much less than the above number. This observation leads us to use a thermal time constant which is much less than the one published. The model parameters are as follows:

Table 2: Thermal Induced ISI Model parameters

Thermal Time constant	2 ns
Quantizer Output Rise/Fall Time	50ps/50ps
dVbe,on/dT (c)	1.11 mV/°C
Time-Step (P)	50ps
Average Temperature (T ₀)	310°K
Min-Max equilibrium Temp	300°K-320°K

To measure the SNR degradation we sweep variables: ΔT and rate of change of base-emitter voltage with temperature. The simulator nominal temperature (i.e. T_{nom}) is made equal to the average temperature in the model (i.e. T₀).

The plot in fig.7 shows the input voltage dependent device temperature with $\Delta T=10^\circ\text{K}$, T₀=310°K and $\tau=2\text{nsec}$.

The plot of the frequency spectrum from the output of the 2nd order CT $\Delta\Sigma$ modulator is shown in figs. 8-9 for different values of ΔT . The CT $\Delta\Sigma$ modulator has been simulated using Cadence Spectre simulator for 8,000 clock cycles with a single-tone signal of amplitude 200mV at 5MHz. The higher OSR (i.e. $f_s/2f_0=100$) keeps the quantization noise power low and accentuates the effect of noise generated by the thermal mismatch.

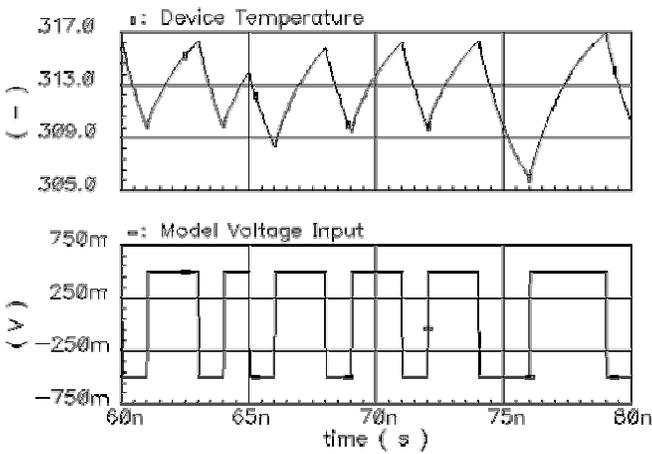


Fig. 6: Signal Dependent device temperature change with $\Delta T=10^\circ\text{K}$, T_{nom}=310°K, $\tau=2\text{nsec}$

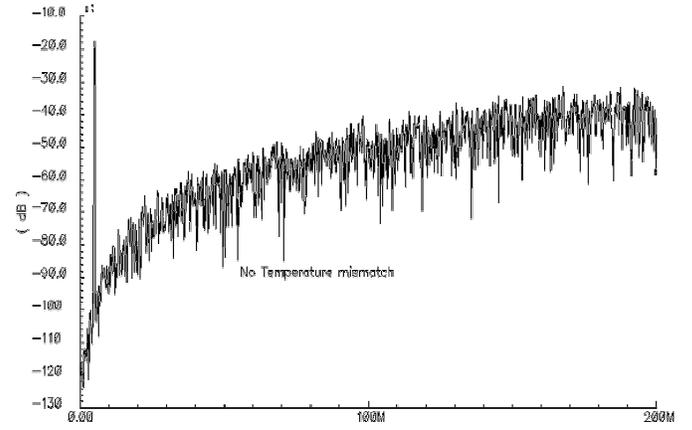


Fig. 7: Frequency Spectrum at 0°K (baseline plot without temperature mismatch)

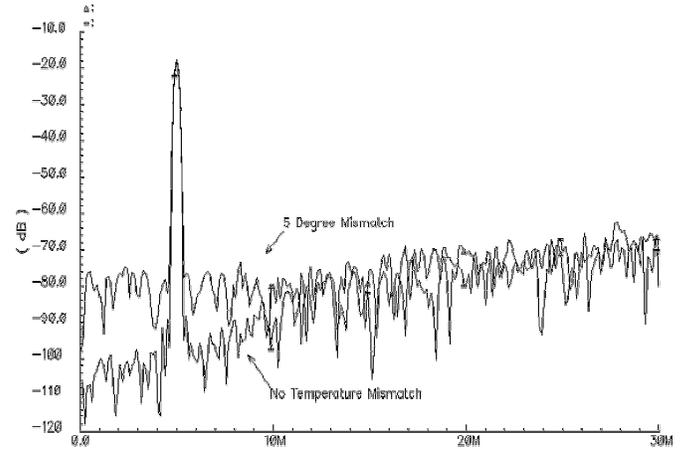


Fig. 8: Frequency Spectrum at ΔT at 0°K, 5°K showing 20db degradation in SNR at OSR=100

The plot below in fig.9 shows the effect of temperature and device mismatches. The devices have been mismatched by 10% changing β (beta), I_s (saturation current) and c (Rate of turn-on voltage).The device mismatch parameters are as follows:

Table 3: Device Mismatch Parameters:

Device Parameter	Q1	Q2
Saturation Current (I_s)	5e-15A	6e-15A
Beta (β)	50	55
dVbe,on/dT	1.11mV/°C	1.25mV/°C

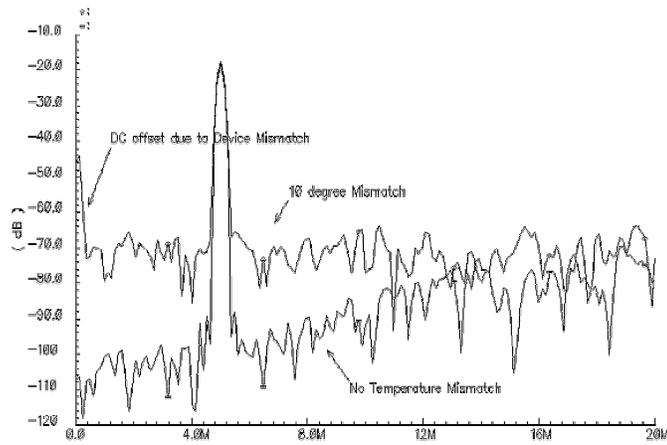


Fig. 9: Frequency spectrum with 10°K Temperature mismatch and 10% Device mismatch

Conclusion

The results from the model show the dependence of SNR in a CTΔΣ modulator on the thermal characteristics of the transistors. From figs. 7-9, one can make the following observations. The SNR degradation in a continuous time delta-sigma modulator is strongly correlated to the signal dependent temperature mismatch in the DAC. Any further increase in temperature mismatch can cause the modulator to go unstable. Mismatched devices introduce a DC offset voltage and DC offset current. This effect is seen with a significant DC component in the frequency spectrum. The SNR degradation gets worse with increasing OSR, since eventually noise due to thermal mismatch will exceed the quantization noise power.

Future work will be to make use of the model described in this paper to design compensation circuits to mitigate such effects. Accurate thermal time constant can give more realistic results and therefore more testing to measure the thermal resistance (i.e. R) and heat capacity of successive hemispherical shells around the emitter (i.e. C) in InP-based HBT devices is needed. Also, testing the model for 4th order band-pass CTΔΣ modulator will be done as further extension to this work.

References

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- [2] M. Hafizi, W. E. Stanchina, F. Williams Jr., J.F. Jensen, "Temperature Dependence of DC and RF Characteristics of AllInAs/GaInAs HBT's," IEEE Transactions on Electron Devices, vol. 40, No. 9, pp. 1583-1588, Sept. 1993.
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- [4] William Liu, "Transient Response of Junction Temperature in Power Heterojunction Bipolar Transistors," Jpn. J. Appl. Physics, Vol. 32 (1993), Pt. 1, No. 12A, pp. 5503-5507.
- [5] J.A. Cherry, W.M. Snelgrove, "Approaches to simulating Continuous Time Delta Sigma Modulators", Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, vol. 1, pp. 587-590, June 1998.

[6] G. Massobrio, P. Antognetti, "Semiconductor Device Modeling with SPICE", 2nd ed., McGraw Hill Inc., pp. 45-129, 1993.

Appendix

The Verilog-A code of the perturbation voltage which models thermal induced inter-symbol interference is as follows:

```

`include "constants.h"
`include "discipline.h"
module VJT(vminus,vplus);
inout vminus,vplus;
electrical vminus,vplus;

// temperature dependent parameters
parameter real tc = 2e-9; // thermal time constant
parameter real th = 310; // equilibrium temperature (High)
parameter real tl = 300; // equilibrium temperature (Low)
parameter real pw = 50e-12; // fixed time step;
parameter real c = 1.11e-3; // thermal coefficient [mV/degC]

real delt, to, tnom;
real real_time, prev_time, step, state;
real prev_devt, curr_devt, dvj, Vin;

analog begin
    @ ( initial_step or initial_step("static") ) begin
        to = (th + tl)/2;
        tnom = to;
        delt = (th - tl)/2;
        prev_devt = to;
        curr_devt = prev_devt;
        dvj = 0.0;
    end

    Vin = V(vminus);

// Modeling the input dependent Device Temperature
// rising edge of the input
    @ (cross(Vin,1.0)) begin
        state = 1;
        step = $abstime - prev_time;
        curr_devt = exp(-step/tc)*prev_devt
            + to*(1 - exp(-step/tc))
            - delt * (1 - exp(-step/tc));
        dvj = c*(curr_devt-tnom);
    end

// falling edge of the input
    @ (cross(V(vminus),-1.0)) begin
        state = -1;
        step = $abstime - prev_time;
        curr_devt = exp(-step/tc)*prev_devt
            + to*(1 - exp(-step/tc))
            + delt * (1 - exp(-step/tc));
        dvj = c*(curr_devt-tnom);
    end
end

```

```

// At every time step
@ (timer(0,pw)) begin
    step = 0.0;
    prev_time = $abstime;
    prev_devt = curr_devt;
    if (state == 1) begin
        curr_devt = exp(-pw/tc)*prev_devt
            + to*(1 - exp(-pw/tc))
            + delt * (1 - exp(-pw/tc));
    end

    else begin
        curr_devt = exp(-pw/tc)*prev_devt
            + to*(1 - exp(-pw/tc))
            - delt * (1 - exp(-pw/tc));
    end

// Changing the emitter base junction potential
    dvj = c*(curr_devt-tnom);
end
V(vminus,vplus) <+ dvj;
end

```

Verilog-A code for the quantizer is as follows:

```

quantizer(inp,inn,outp,outn,clk);
input inp,inn,clk;
output outp,outn;
electrical inn,inp,outp,outn,clk;
parameter real quantizer_vth = 0.0;
parameter real clk_vth = 0.0;
parameter real vlevel = 0.5;
parameter real tr = 50p;
parameter real tf = 50p;
real vout,vint;

analog begin
@ (cross(V(clk) - clk_vth,1))
begin
    vint = V(inp,inn);
    // differential input quantizer
    if (vint > quantizer_vth) vout = vlevel;
    else vout = -vlevel;
end
V(outp) <+ transition(vout,0,tr,tf);
V(outn) <+ transition(-vout,0,tr,tf);
end
endmodule

```