Synthesis of CCs and CFOAs by manipulation of VFs and CFs

Leticia Torres-Papaqui
INAOE
Department of Electronics
lpapaqui@inaoep.mx

Esteban Tlelo-Cuautle
INAOE
Department of Electronics
e.tlelo@ieee.org

ABSTRACT

A systematic synthesis methodology is introduced for the automatic design of current conveyors (CCs) and current feedback operational amplifiers (CFOAs), at the transistor level. The synthesis procedure for these active devices is executed in four steps: selection of generic cells composed of nullators/norators; addition of norators/nullators to form joined nullator-norator pairs; addition of the biasing circuitry and finally; synthesis of the joined pairs by transistors. The proposed synthesis-method has the capability to generate novel active devices, from which the best transistor-circuit design is selected among all the generated-topologies according to their frequency response by using SPICE.

Keywords

Analog synthesis, current conveyor, current feedback operational amplifier, biasing transistor circuits, nullor.

1. INTRODUCTION

Fully automated design of analog circuits remains quite complicated due to their topological complexity [1]-[2]. That is, there is no simple rule neither to describe nor to establish the number of possible topologies even with a few components. Although several efforts has been devoted to enhance the capability of synthesis for several active devices [3]-[5], the selection of a correct topology along with the biasing problem, constitutes the most complicated part of analog design automation of transistor circuits [1],[6]-[7].

The basic procedure to select topologies can be referred to the methods given in [5] and [6], which explore all combinations to connect generic two-terminals elements, namely: impedances, nullators, and norators. Furthermore, this paper sets the guidelines to aid the automatic synthesis of active devices by manipulation of generic cells composed of nullators and norators. In this manner, in section 2 are introduced several generic topologies to implement voltage- (VF), and current-followers (CF). In section 3, is described where and how to add norators and nullators to form joined nullator-norator pairs, this step generates multiple combinations from which the ones suitable for synthesis purposes are selected by applying heuristic reasoning. In section 4 is introduced the manner in which the biasing circuitry is automatically added, in this step several relocation operations for norators and nullators are done to obtain an efficient biased circuit. The synthesis of current conveyors (CCs) and current feedback operational amplifiers (CFOAs), at the transistor level is shown in section 5. Finally, the conclusions are summarized in section 6.

2. GENERIC CELLS

The synthesis of CCs and CFOAs can be related to the generation of the small-signal design for VFs and CFs, the addition of their biasing circuitry, and the coupling or superimposing of VFs and CFs [2],[4]-[6].

2.1 Voltage followers

For the design automation of VFs, it is quite useful to model their ideal behavior by using nullators [6]. So that its small-signal design can be modeled by a single floating nullator, two nullators, or a four nullators-bridge, as shown in Fig. 1. By applying the voltage-property of the nullator, for which the voltage across its terminals equals to zero [3], then $v_o = v_i$.

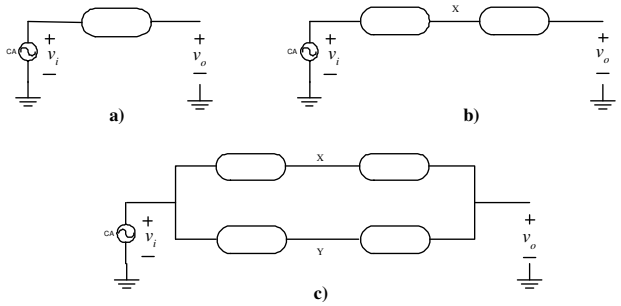

Figure 1: Generic cells to implement a VF.

2.2 Current followers

As for the VF, the CF can be modeled by a generic cell implemented with a single or some norators, as shown in Fig. 2. By applying the current-property of the norator, for which the current through its terminals becomes the same [3], then $i_o = i_i$.

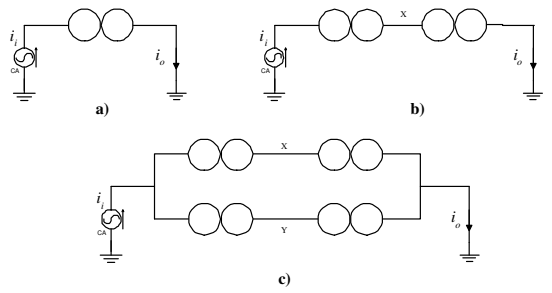

Figure 2: Generic cells to implement a CF.

3. JOINING NULLATOR-NORATOR PAIRS

This section introduces the manner in which an automatic system adds one norator (P) to each nullator (O), and vicevera, in order to form joined nullator-norator pairs suitable

for biasing and synthesis purposes. Lets consider the VF shown in Fig. 1a, to form a joined pair there exist three combinations to add a norator, as shown by Fig. 3. However, since for a VF the norator is basically used to stabilize the output, the joined pair shown in Fig. 3a, is not suitable for biasing and synthesis purposes at the transistor level. That is, by replacing the joined pair by either a BJT or a MOSFET [3],[6], v_i being connected between either the emitter-collector or the source-drain terminals, which results in an impractical topology. Also, by applying circuit analysis [8], the circuit shown in Fig. 3a is impractical to formulate a system of equations. Furthermore, the others joined pairs could be suitable for biasing and synthesis purposes, since by applying circuit analysis, ideally v_o=v_i.

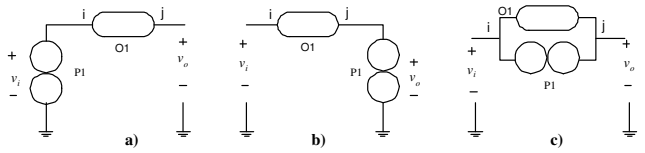

Figure 3: Addition of a norator to a nullator: (a) at node i, (b) at node j, and (c) between nodes i and j.

As one sees, the number of combinations to form a joined pair, can be established by (1), which also applies to form joined pairs for the CFs shown in Fig. 2. n denotes the number of nullators/norators. So that by forming joined pairs for the VF shown in Fig. 1c, 6 combinations suitable for biasing purposes are shown in Fig. 4. For the CF shown in Fig. 2c, 4 combinations are shown in Fig. 5.

$$combinations = 3^n \tag{1}$$

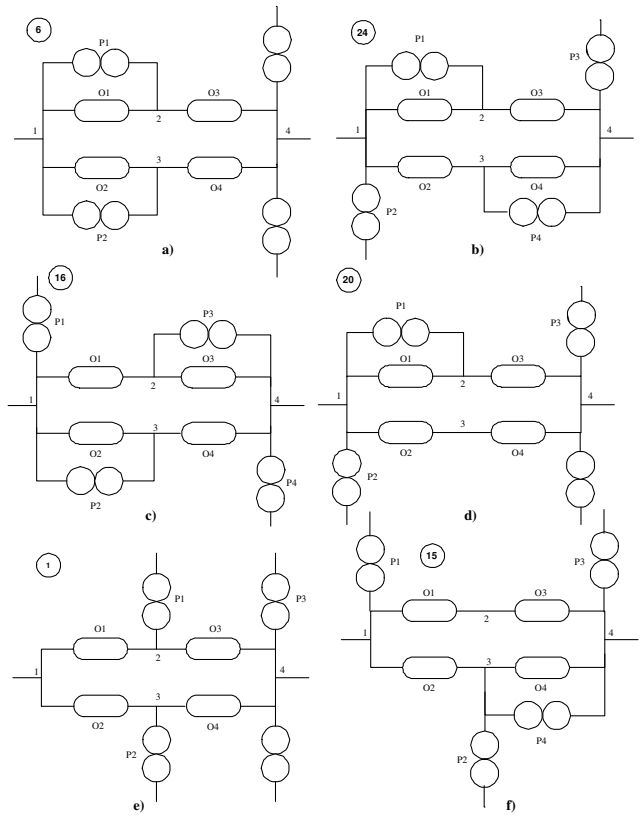

Figure 4: 6 of the 81 combinations to add norators to Fig. 1c.

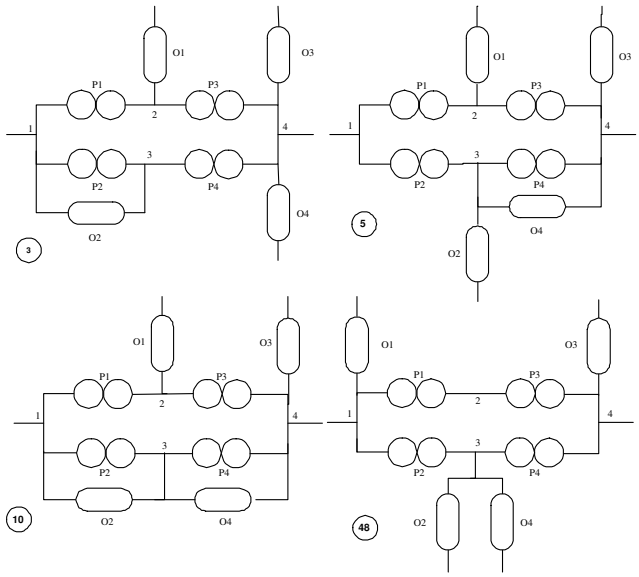

Figure 5: 4 of the 81 combinations to add nullators to Fig. 2c.

4. ADDING THE BIASING CIRCUITRY

The addition of the biasing circuitry can be divided in two steps: Addition of voltage bias levels, which are mainly added to nullators, and addition of current bias levels, which are mainly added to norators [6]. It can be automatically added as follows:

1. From the small-signal nullor-circuit, generate two structures including nullators (O) and norators (P). All nodes should be ordered numerically.
2. Add dc global-bias voltage-sources.
3. Search all combinations to connect Os first, and secondly Ps to the global-bias, but avoiding its connection to the input or output port.
4. Add dc local-bias voltage-sources to nullators which need a bias level, and also add dc local-bias current-sources to norators.
5. Determine the uniqueness of the dc operating point [7]. If it is guaranteed, then the resulting biased circuit is suitable for synthesis purposes.

Lets consider the VF shown in Fig. 3b, the addition of the biasing circuitry is done as follows:

The net-lists including the names and nodes of Os and Ps are shown in Table 1.

Table 1: Net-list of nullators and norators

Nullator	nodes	Norator	nodes
O1	1,2	P1	2,0

The addition of the global-bias voltage-source (V_{GBS}) generates the global nodes (3,0), as shown in Fig. 6b. There are two forms to connect O1 to node 3, however both nodes of O1 (1 and 2), are directly connected to the input and output port, therefore: neither node 1 nor node 2 can be connected to node 3 [6]. By searching all combinations to connect P1 to node 3, there are also two forms: node 2 of P1 is discarded, since it is connected with O1 to form a joined pair. So that P1 should be relocated to node 3, as shown

in Fig. 6c. A resistor R should be inserted where P1 was connected in order to measure v_o.

There is one possibility to add a local-bias voltage-source (V_{LBS}) to node 1 of O1, where it is superimposed [4], to the input voltage signal as shown by Fig. 6d.

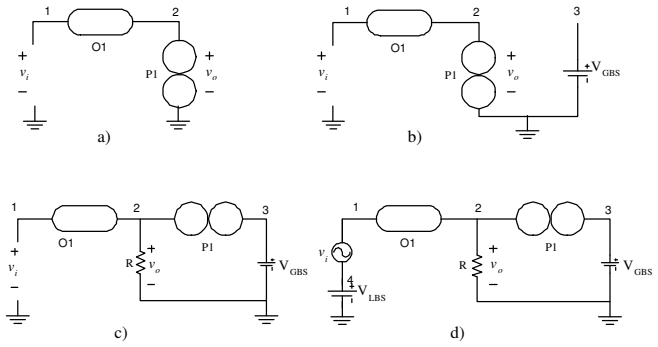

Figure 6: Biasing the nullor circuit from Fig. 3b.

It is not necessary to add local-bias current-sources, since the circuit is fully biased. Finally, the uniqueness of the dc operating point [7], is guaranteed.

For the VF shown in Fig. 3c, it is impossible to obtain a biased circuit, since neither the nullator can be connected to a voltage source nor the norator can be relocated because both nullator and norator must remain connected in parallel. In this manner, although three combinations were generated for the VF according to (1), only one of them was well suited for biasing purposes, the one shown by Fig. 3b.

5. SYNTHESIS OF THE CC AND CFOA

If a biased nullor-circuit performs the desired behavior [8]-[10], then each joined pair can be synthesized by either a BJT or a MOSFET. So that for the VF shown by Fig. 6d, as O1 and P1 form a joined pair, it can be synthesized by either a BJT or a MOSFET, as shown by Fig 7a and Fig. 7b, respectively.

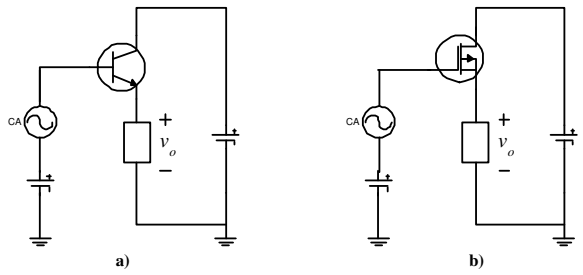

Figure 7: Synthesis of the nullor circuit shown by Fig. 6d.

By biasing the VFs shown in Fig. 4, and by synthesizing them by using MOSFETs, the resulting circuits are shown by Fig. 8. The transistor sizing can be done by applying well established methods, as the ones sketched in [1].

By biasing the CFs shown in Fig. 5, and by synthesizing them by using MOSFETs, the resulting CFs at the transistor level are shown by Fig. 9.

5.1 Synthesis of the CC and CFOA

Among all the methodologies to design active devices, the CC and CFOA can be synthesized by cascading VFs and CFs as shown by Fig. 10 [2],[6], in which both active devices has been connected to perform the integration function.

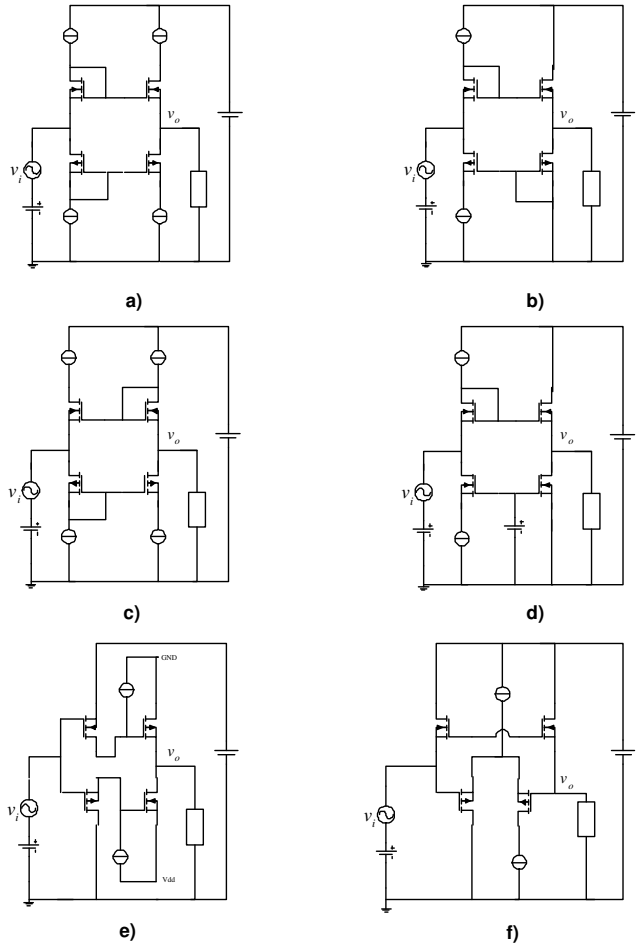

Figure 8: Synthesis of the VFs from Fig. 4.

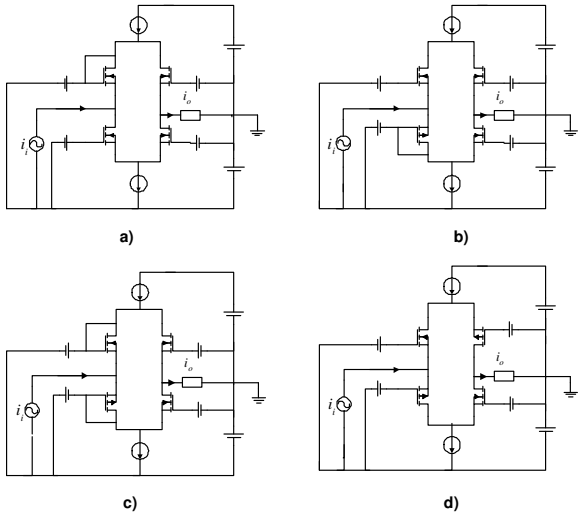

Figure 9: Synthesis of the CFs from Fig. 5.

Henceforth, by superimposing the VF shown in Fig. 8a, with the CF shown in Fig. 9c, the resulting circuit behaves as a CC, as shown by Fig. 11. Furthermore, by simply cascading another VF (the one shown in Fig. 8a), to the output port of the CC, the resulting active device performs the behavior of a CFOA, as shown by Fig. 12.

By sizing the CC and CFOA [1],[11], and by simulating the time response of the integrators shown in Fig. 11 and Fig. 12 by using SPICE, simulation results are shown by Fig.

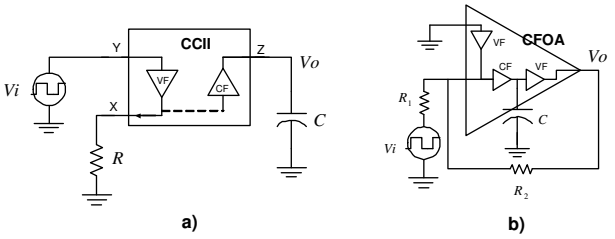

Figure 10: Synthesis of the CC and CFOA

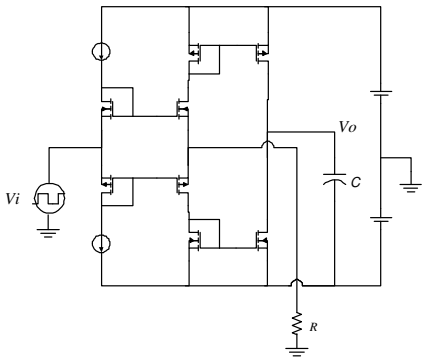

Figure 11: Synthesis of the CC by superimposing one VF with one CF, and connected to perform the integration function.

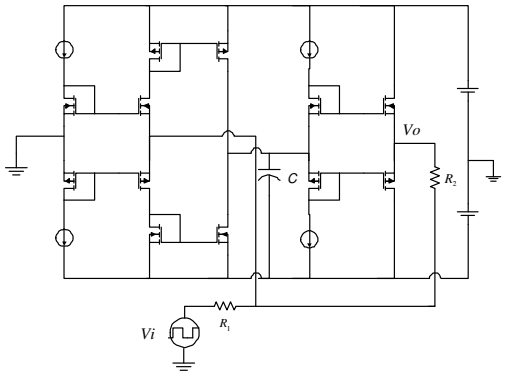

Figure 12: Synthesis of the CFOA by cascading a CC with one VF, and connected to perform the integration function.

13 and Fig. 14, respectively. As a result, one can conclude on the suitability of the proposed synthesis methodology to design active devices by manipulation of generic cells, e.g. VFs and CFs.

Acknowledgment

This work is supported by CONACyT-MEXICO under project number J40321-Y.

6. CONCLUSION

It has been introduced a systematic synthesis methodology focused on the automatic design of active devices at the transistor level. It has been shown that this methodology is well suited to generate new transistor circuits.

The proposed synthesis method has been divided in four steps: selection of a generic cell implemented with nullators or norators, the manner in which an automatic system adds nullators or norators to form joined pairs suitable for biasing purposes, the manner in which an automatic system adds

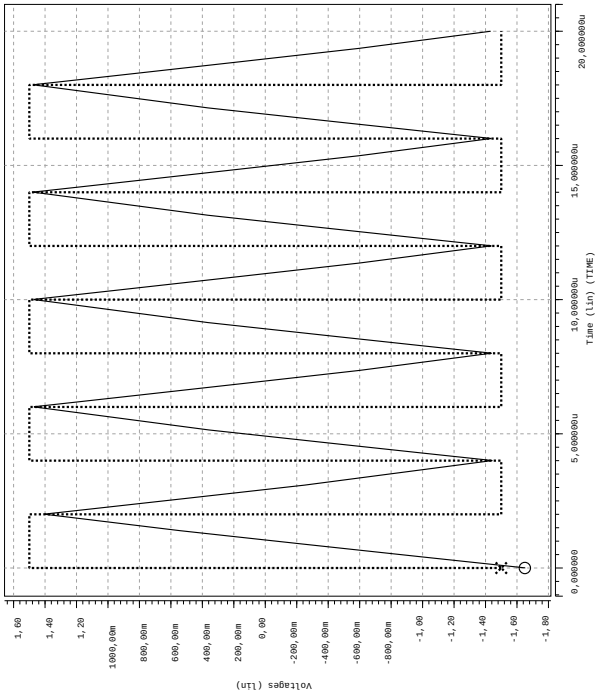

Figure 13: SPICE simulation of the integrator shown by Fig. 11.

the biasing circuitry, and the manner in which each joined pair is synthesized by a BJT or a MOSFET. Optimization techniques must be applied to the generated designs, in order to obtain the better behavior and high performance of the final transistor circuit design.

Finally, the method has been highlighted by synthesizing the CC and CFOA, for which SPICE simulations results show the suitability and capability of the proposed technique to generate novel active devices.

7. REFERENCES

[1] Rob A. Rutenbar, Georges G. E. Gielen and Brian A. Antao, Computer-Aided Design of Analog Integrated Circuits and Systems, IEEE Press Piscataway NJ (2002)

[2] C. Toumazou, B. Gilbert, G. S. Moschytz, Trade-Offs in Analog Circuit Design, Kluwer Academic Publishers London (2002)

[3] H. Schmid, Approximating the universal active element, IEEE TCAS-II, vol. 47, no. 11 (2000) 1160-1169

[4] Hajime Shibata and Nobuo Fujii, Analog circuit synthesis by superimposing of sub-circuits, IEEE ISCAS, vol. V (2001) 427-430

[5] David Haigh, Fang Qun Tan and Christos Papavassiliou, Systematic synthesis method for analogue circuits Part III All-Transistor circuit synthesis, IEEE ISCAS, vol. I (2004) 709-712.

[6] E. Tlelo-Cuautle, A. Diaz-Sánchez, An heuristic circuit-generation technique for the design-automation of analog circuits, IEEE ISCAS, vol. I (2003) 193-196.

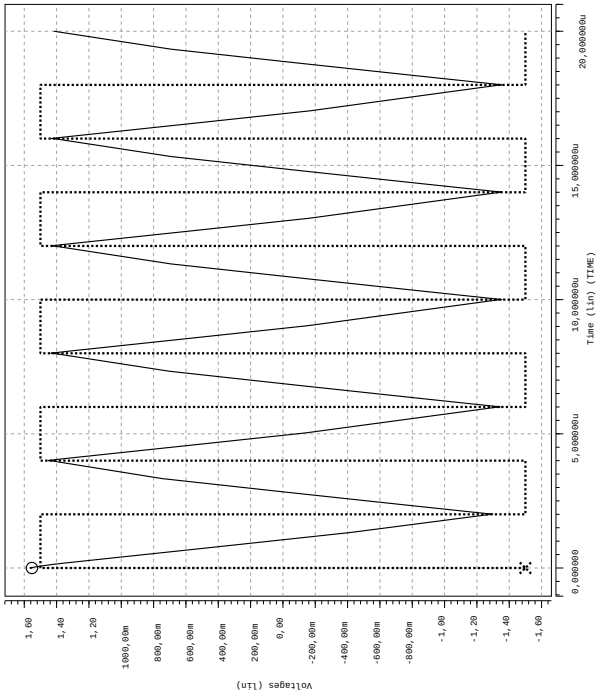

Figure 14: SPICE simulation of the integrator shown by Fig. 12.

[7] Tlelo-Cuautle E., Computing the elements embedded into a positive feedback loop, IEEE ISCAS, vol. III (2002) 531-534.

[8] E. Tlelo-Cuautle, A. Quintanar-Ramos, G. Gutiérrez-Pérez, M. González de la Rosa, SIASCA: Interactive system for the symbolic analysis of analog circuits, IEICE Electron. Express, vol. 1, no. 1 (2004) 19-23

[9] Aguila-Meza J., Torres-Papaqui L., Tlelo-Cuautle E., Improving symbolic analysis in CMOS analog integrated circuits, IEEE ISCAS, vol. V (2004) 193-196.

[10] Junjie Yang Sheldon, X.-D. Tan, Behavioral Modeling of Analog Circuits by Dynamic Semi-Symbolic Analysis, IEEE ISCAS, vol. V (2004) 105-108.

[11] Kenneth R. Laker and Willy M.C. Sansen, Design of Analog Integrated Circuits and Systems, McGraw-Hill (1994)