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ARCHITECTURAL AND PARAMETRIC OPTIMIZATION OF LOW-PASS RF FILTERS IN VHDL-AMS BASED HIGH-LEVEL SYNTHESIS

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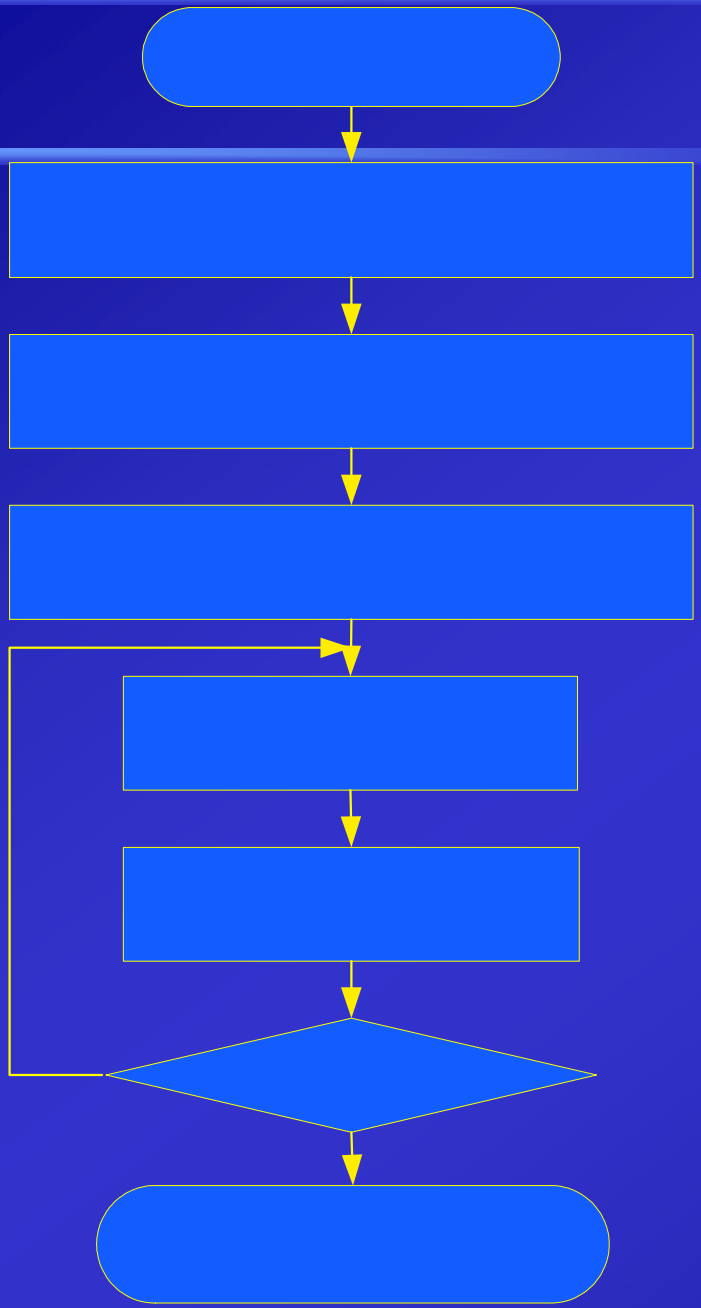
Summary

- RF filter modelling in VHDL-AMS for automated architectural synthesis
- Cell selection and architectural optimization using patterns in VHDL-AMS parse tree
- Three-tier parametric optimization embedded in synthesis
- Case study



Architectural filter synthesis from VHDL-AMS

VHDL-AM

filter de

FIST – filter synthesis system

Parser produ

Scan parse tree

Filter cell models

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2nd order cell type	Time-domain equation	Equivalent VHDL-AMS simultaneous statement
Low pass	$V_{in} = Coeff_1 \times \frac{d^2V_{out}}{dt^2} + Coeff_2 \times \frac{dV_{out}}{dt} + Coeff_3 \times V_{out}$	vin == coeff1*vout'dot'dot + coeff2*vout'dot + coeff3*vout
Band pass	$\frac{dV_{in}}{dt} = Coeff_1 \times \frac{d^2V_{out}}{dt^2} + Coeff_2 \times \frac{dV_{out}}{dt} + Coeff_3 \times V_{out}$	vin'dot == coeff1*vout'dot'dot + coeff2*vout'dot + coeff3*vout
High pass	$\frac{d^2V_{in}}{dt^2} = Coeff_1 \times \frac{d^2V_{out}}{dt^2} + Coeff_2 \times \frac{dV_{out}}{dt} + Coeff_3 \times V_{out}$	vin'dot'dot == coeff1*vout'dot'dot + coeff2*vout'dot + coeff3*vout

Sample description of a 1GHz low pass filter

```
architecture behavioral of filter is
      constant a: real:= 4.15e-10;
      constant b: real:= 8.64e-20;
      constant c: real:= 1.05e-29;
      constant d: real:= 7.88e19;
      constant e: real:= 6.41e-40;
      constant num: real_vector:= (0,0,a);
      constant den: real_vector:= (b,c,d,e,1.0);
begin
      Vout == Vin'LTF(num,den);
end architecture behavioral;
```

Butterworth 4th order

LTF – Laplace Transfer Function

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Architectural optimization process in FIST

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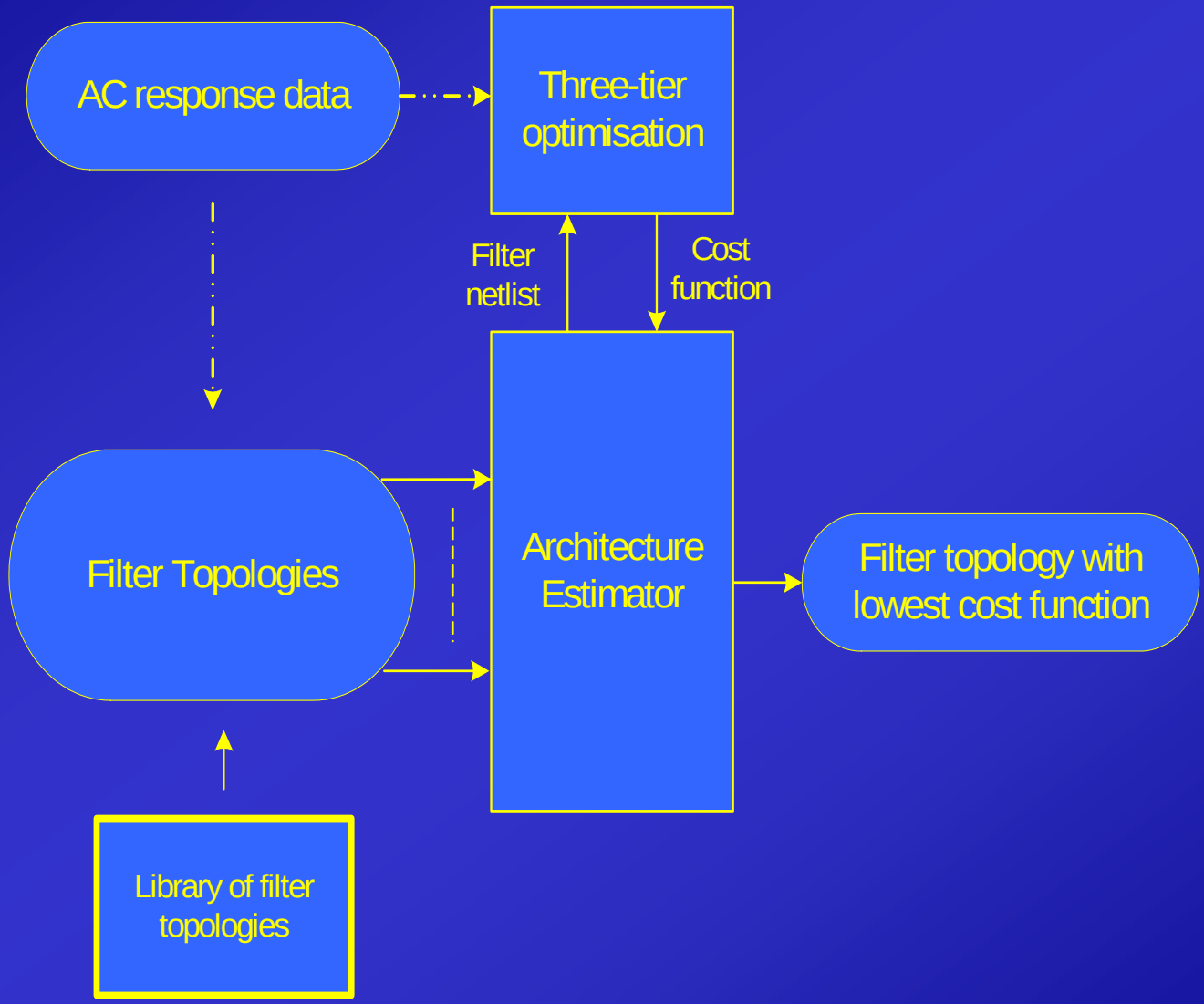
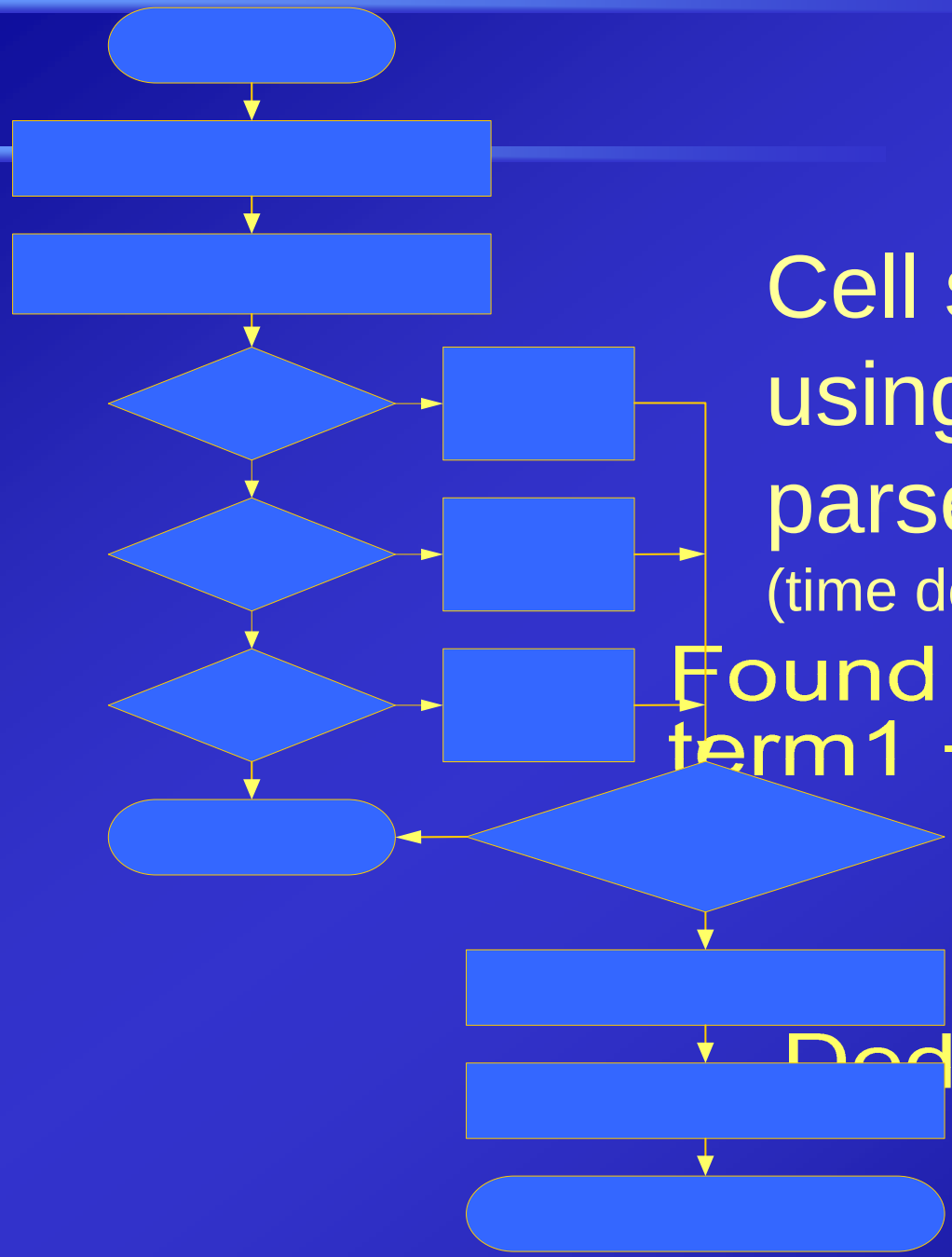


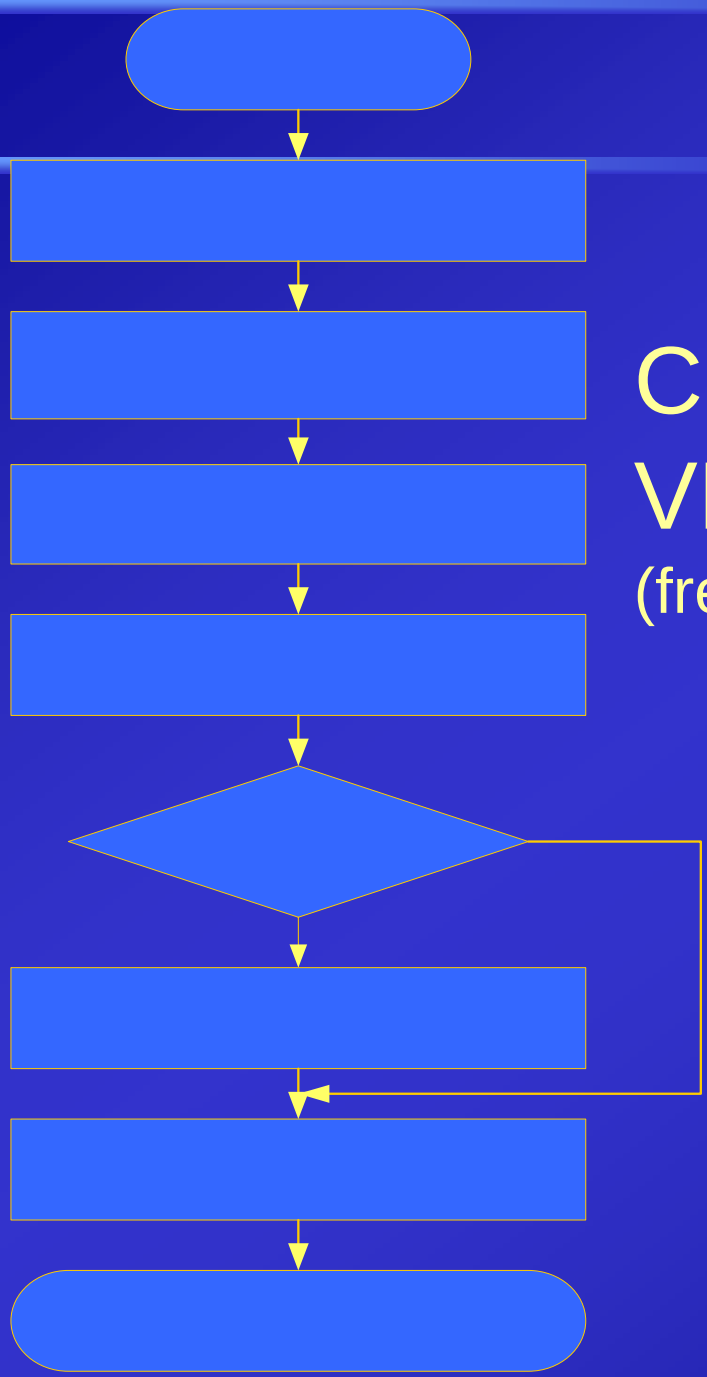


Cell selection
using VHDL-AMS
parse tree
(time domain model)

VHDL-AMS p
tree

Found SSS in the for
term1 + term 2 + term

Reduce filter type f



Cell selection using VHDL-AMS

VHDL-AMS parse tree

(frequency domain model)

Found SSS in the f

Q2'LTF(num, den)

Static calculator to

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Performance criteria

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Accuracy of AC response:

$$err_{total} = [\frac{1}{n} \cdot \sum_{i=1}^{n} err_i^{\,2}]^{1/2}$$

where

$$err_i = \frac{M_i - C_i}{\max(MINVAL, M_i)}, i = 1, n$$

Combined performance criterion:

$$CF = err_{total} \cdot w + Power$$

Three-tier parametric optimization

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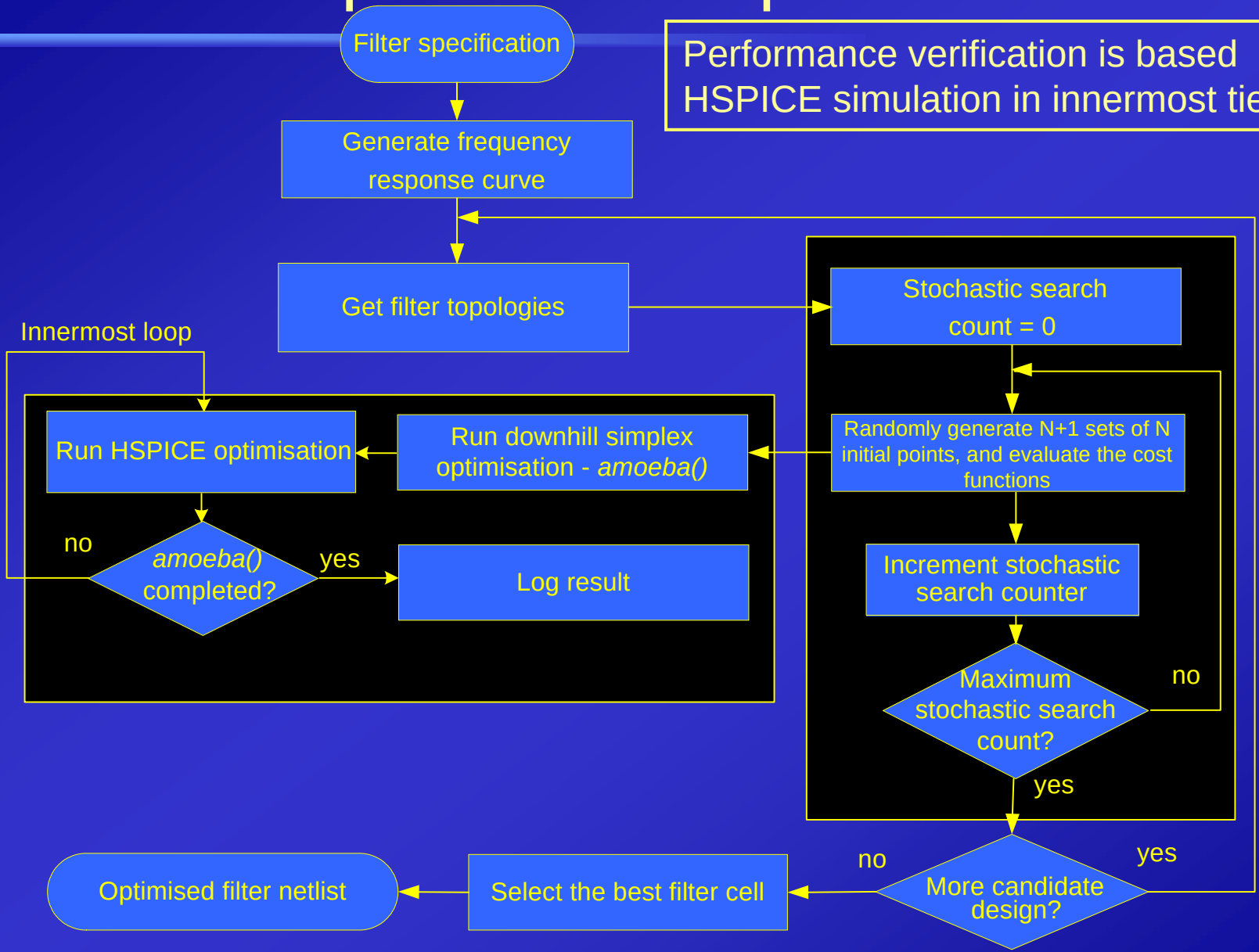
Performance verification is based on full HSPICE simulation in innermost tier



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Case study: 4th-order low-pass 1GHz

configurations selected by synthesiser

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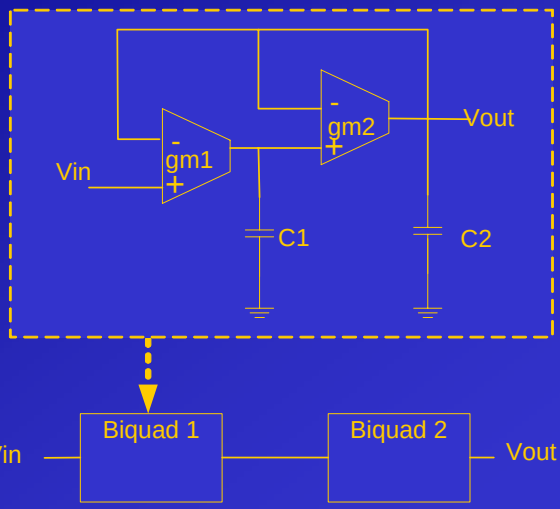
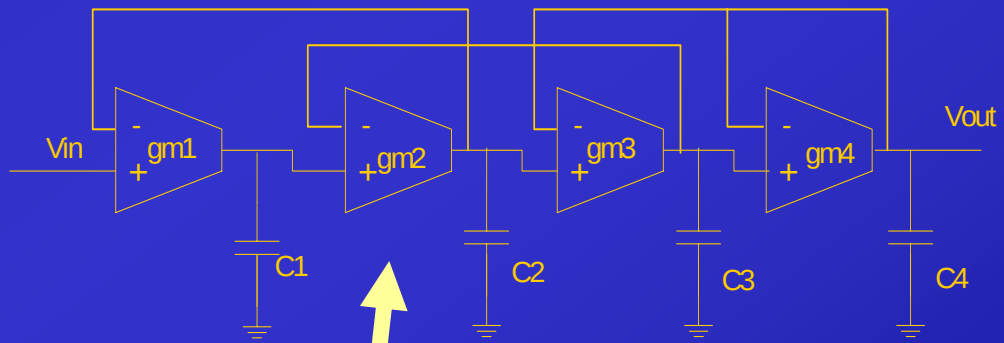
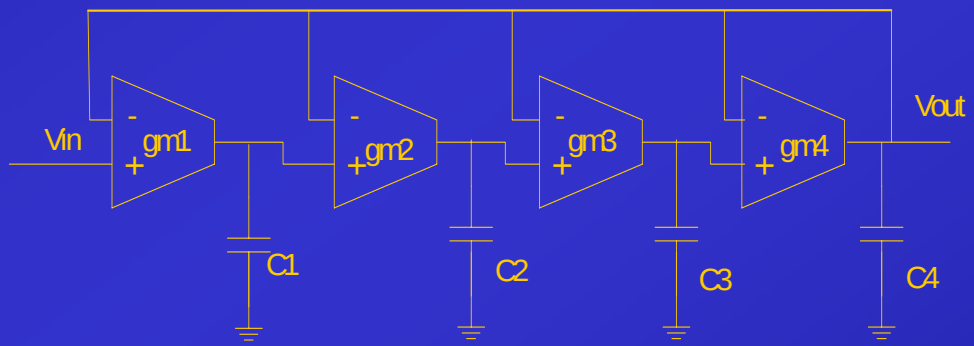


1. Simple OTA cascade
2. Wide-swing OTA cascade



3. LF with simple OTA (BEST)

4. LF with wide-swing OTA



5. IFLF with simple OTA
6. IFLF with wide-swing OTA

Case study: 4th-order low-pass 1GHz

synthesis results

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BEST

	Topology	Error figure	Size (no of MOSFETs)	Power (mW)
1	Simple OTA cascade	0.663	20	160
2	Wide-swing OTA with output buffer cascade	0.513	64	2900
3	LF with simple OTA	0.307	20	163
4	LF with wide-swing OTA with output buffer	0.634	64	2900
5	IFLF with simple OTA	0.458	20	111
6	IFLF with wide-swing OTA with output buffer	380	64	420

Case study: 4th-order low-pass 1GHz

HSPICE simulation results showing ideal curve and curve for best configuration

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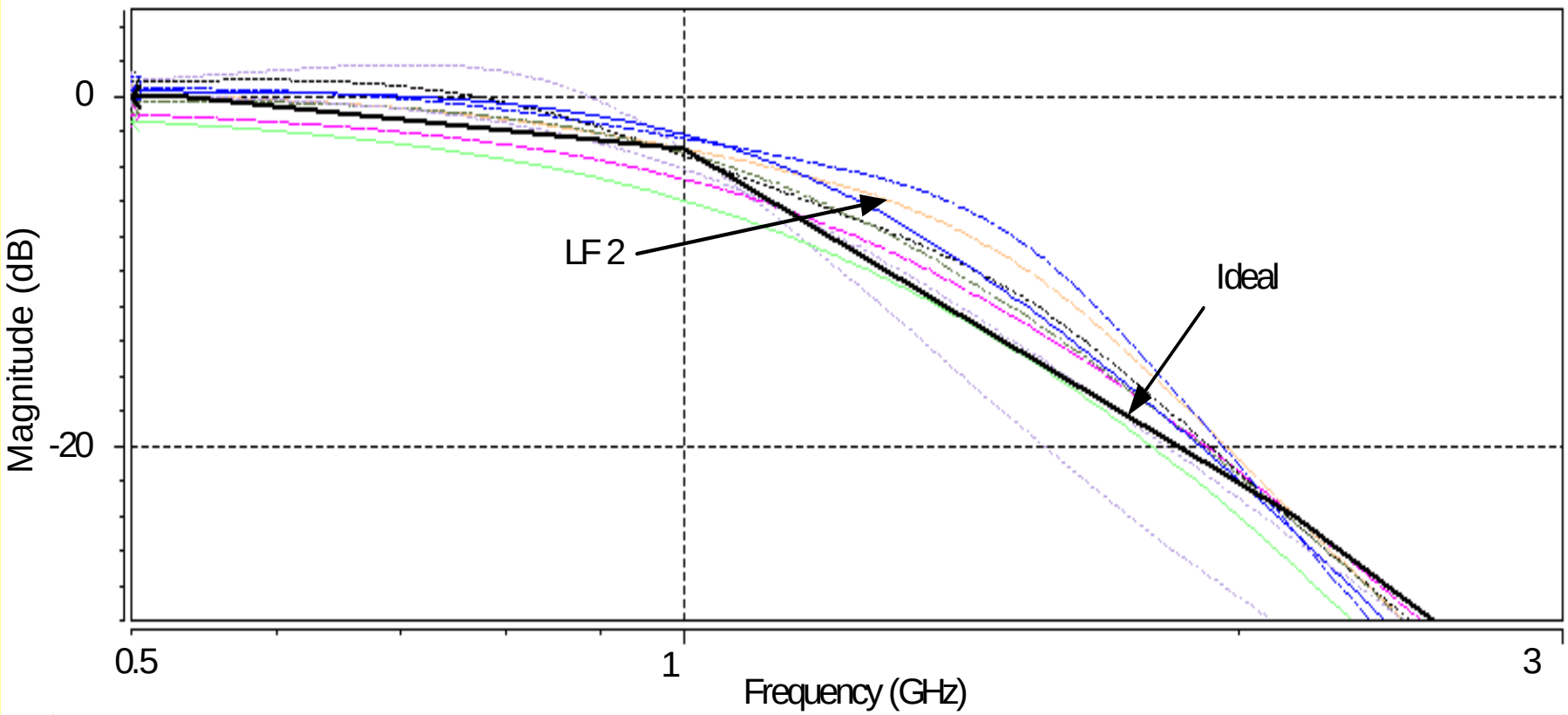

Conclusion

- A methodology has been developed for behavioural modelling in VHDL-AMS and synthesis of RF analogue filters and its implementation named FIST.
- The synthesis algorithm used by FIST is based on the parse tree of the behavioural VHDL-AMS description.
- Inclusive and vital in the synthesis methodology is the parametric optimisation step which works on a selection of filter cells from a library to give the best filter circuit in terms of accuracy.
- Main application is targeted for integrated RF use; the filter cells as well as the optimisation formulation are geared for this application area.
- The feasibility of the presented method has been demonstrated with two case studies of 1GHz 4th order filter synthesis.