Behavioral Modeling in Industrial IC Design

(Experiences and Observations)

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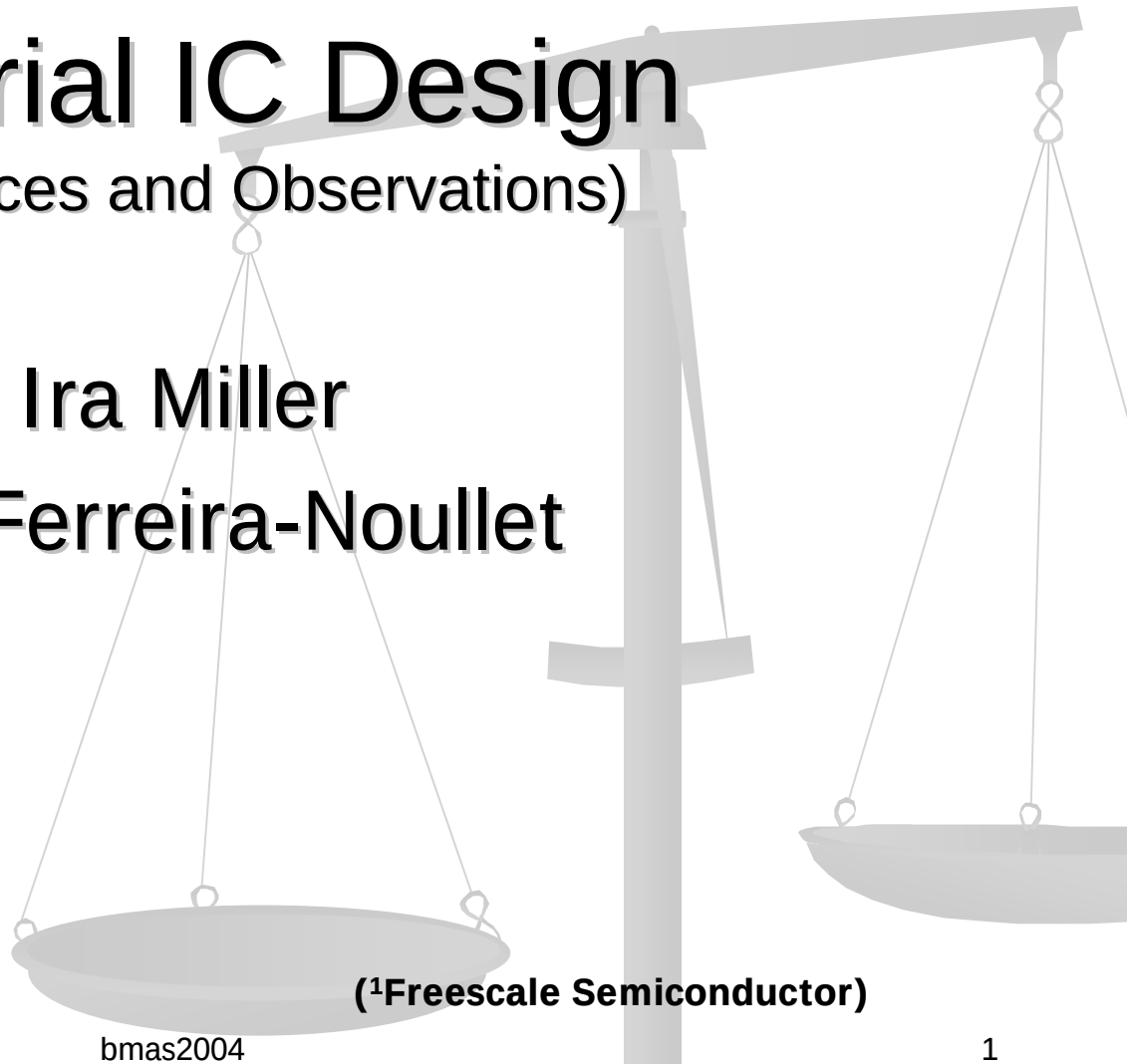
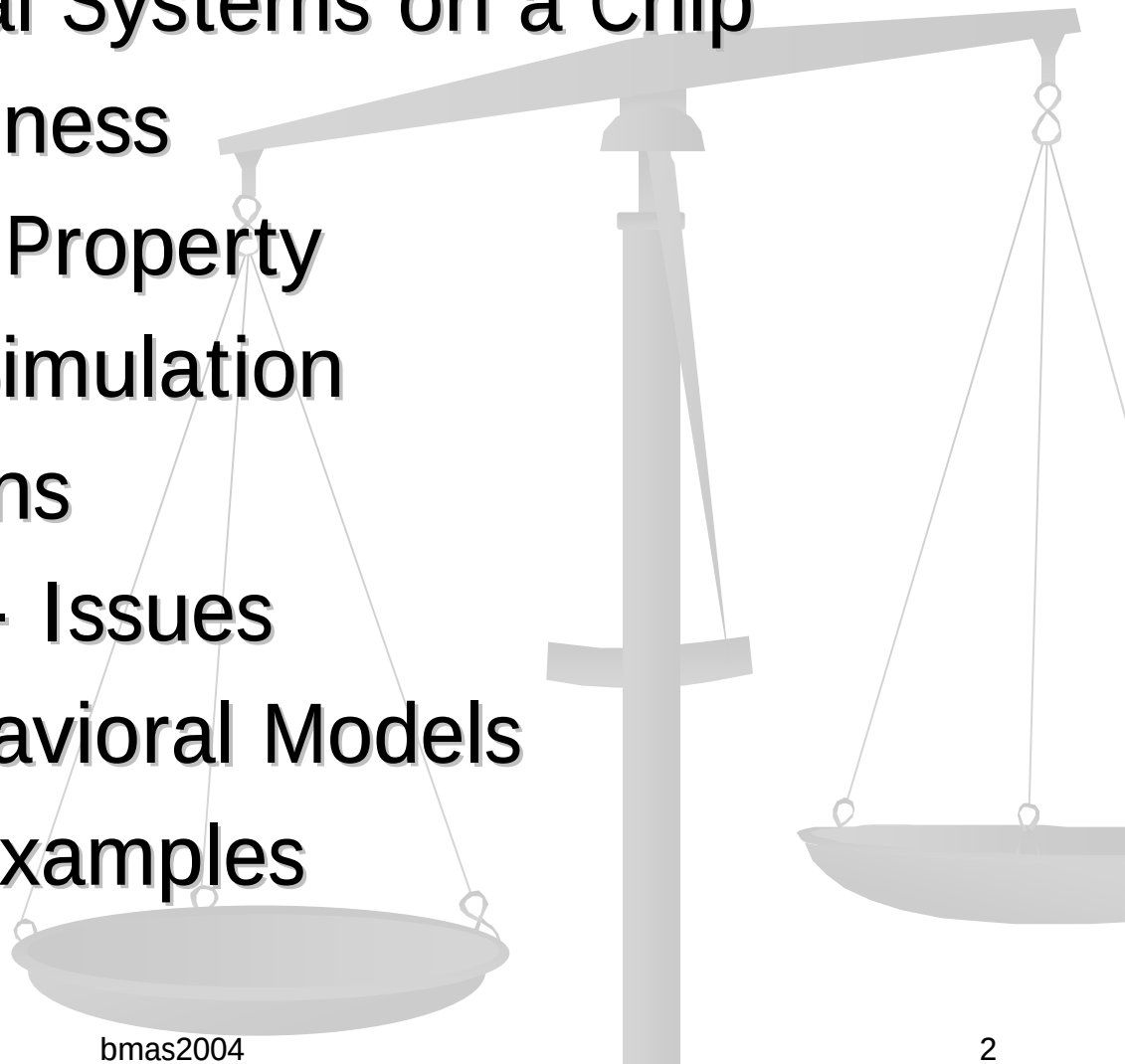


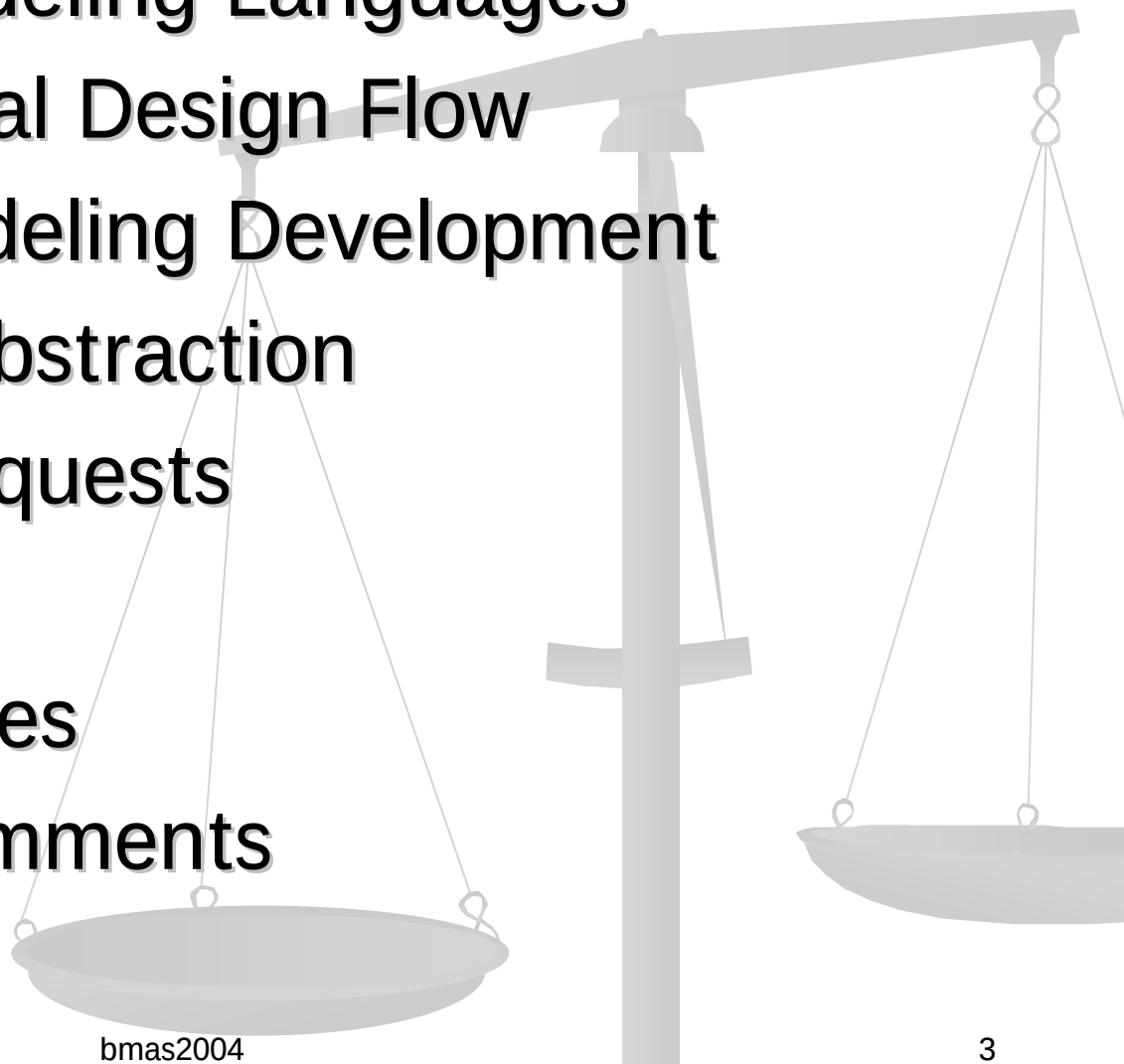
Topics of the Presentation

- ✓ Mixed Signal Systems on a Chip
- ✓ MSSoC Business
- ✓ Intellectual Property
- ✓ Top Level Simulation
- ✓ Specifications
- ✓ Sharing IP - Issues
- ✓ Analog Behavioral Models
- ✓ Analog IP Examples



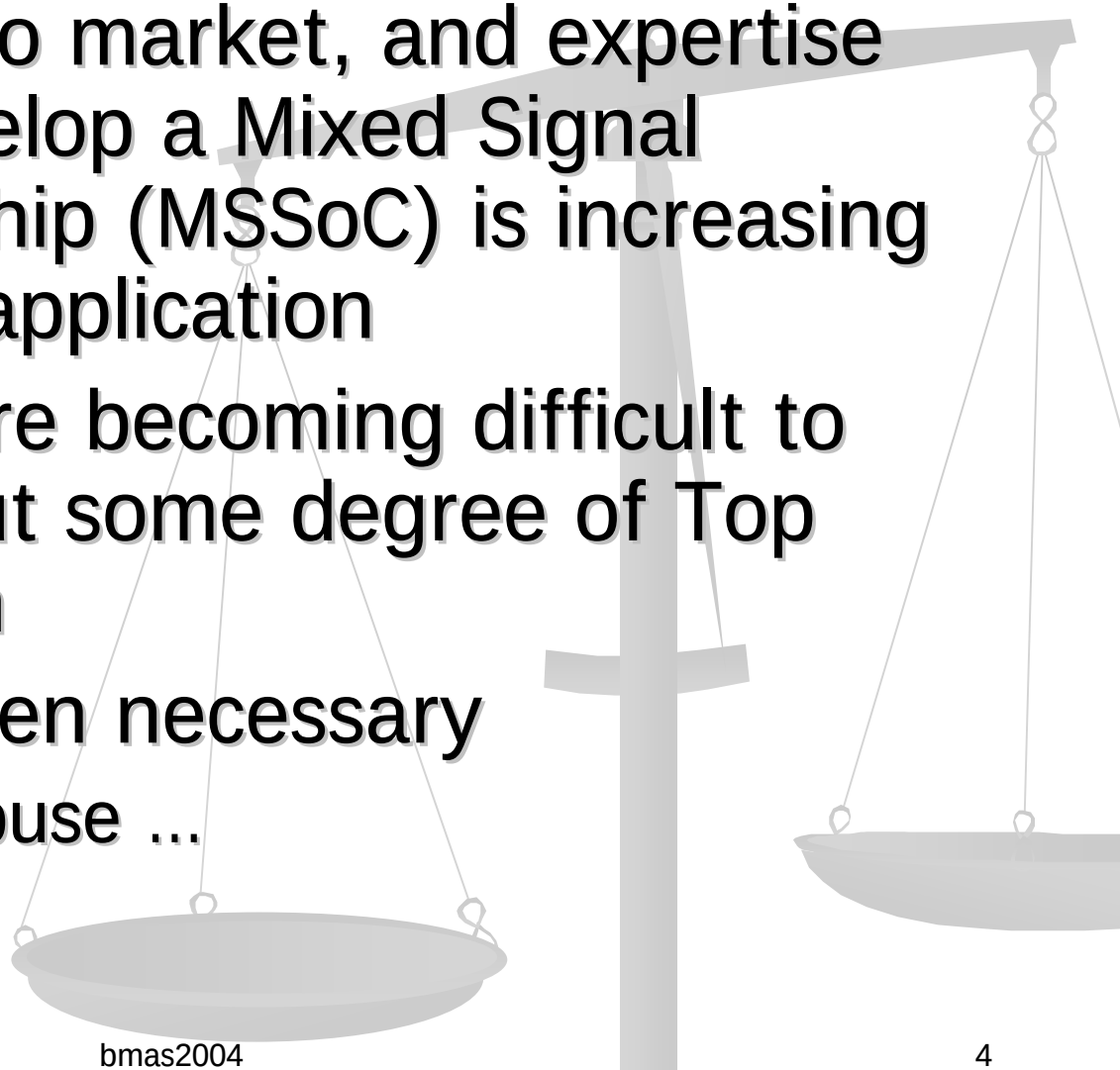
Topics of the Presentation

- ✓ Analog Modeling Languages
- ✓ Mixed Signal Design Flow
- ✓ Analog Modeling Development
- ✓ Levels of Abstraction
- ✓ Feature Requests
- ✓ Training
- ✓ Test Benches
- ✓ Closing Comments



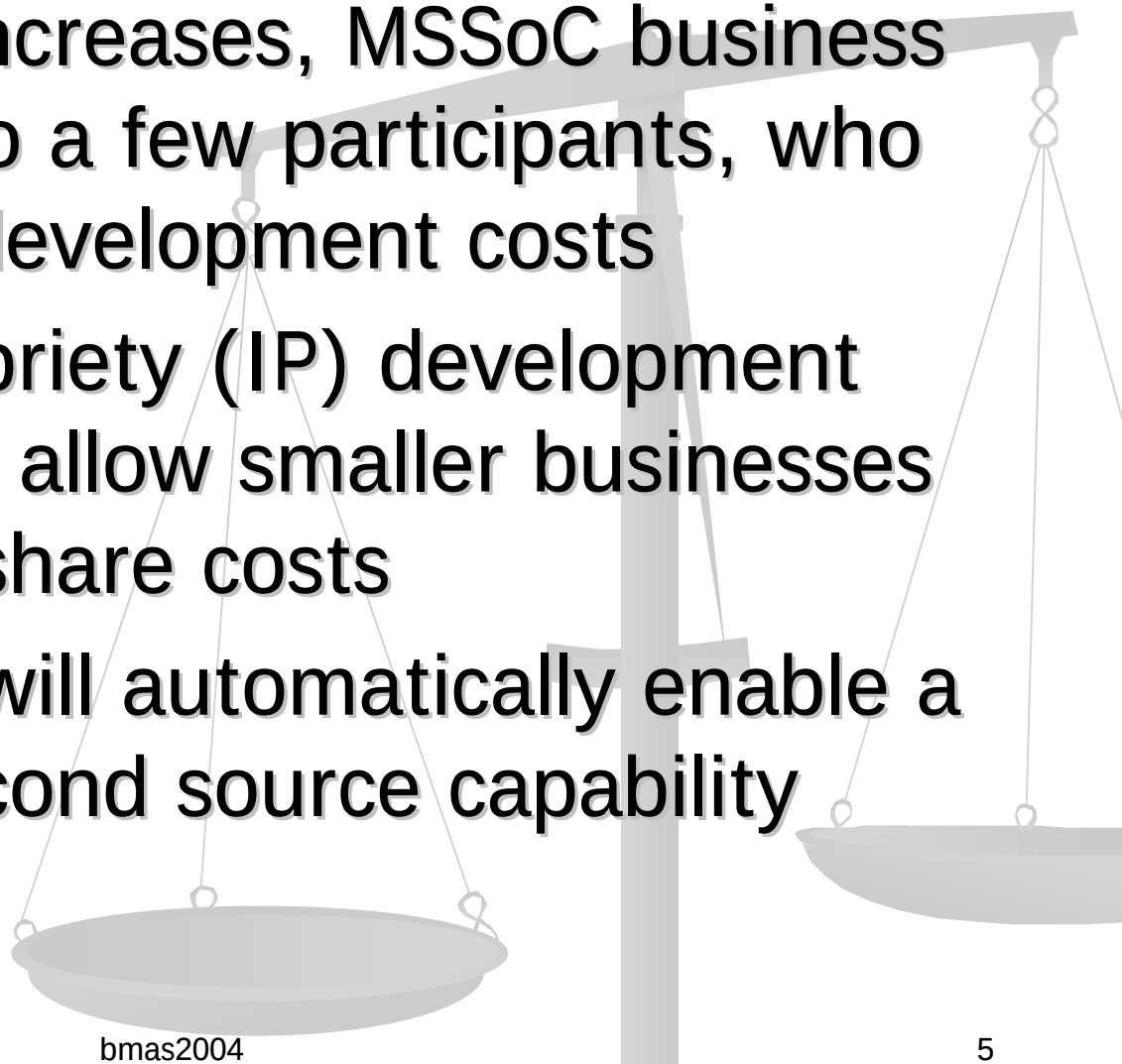
Mixed Signal Systems on a Chip

- ✓ The cost, time to market, and expertise required to develop a Mixed Signal Systems on a Chip (MSSoC) is increasing with each new application
- ✓ Specifications are becoming difficult to establish without some degree of Top Level simulation
- ✓ Re-spins are often necessary
  - ✓ FAB capacity abuse ...



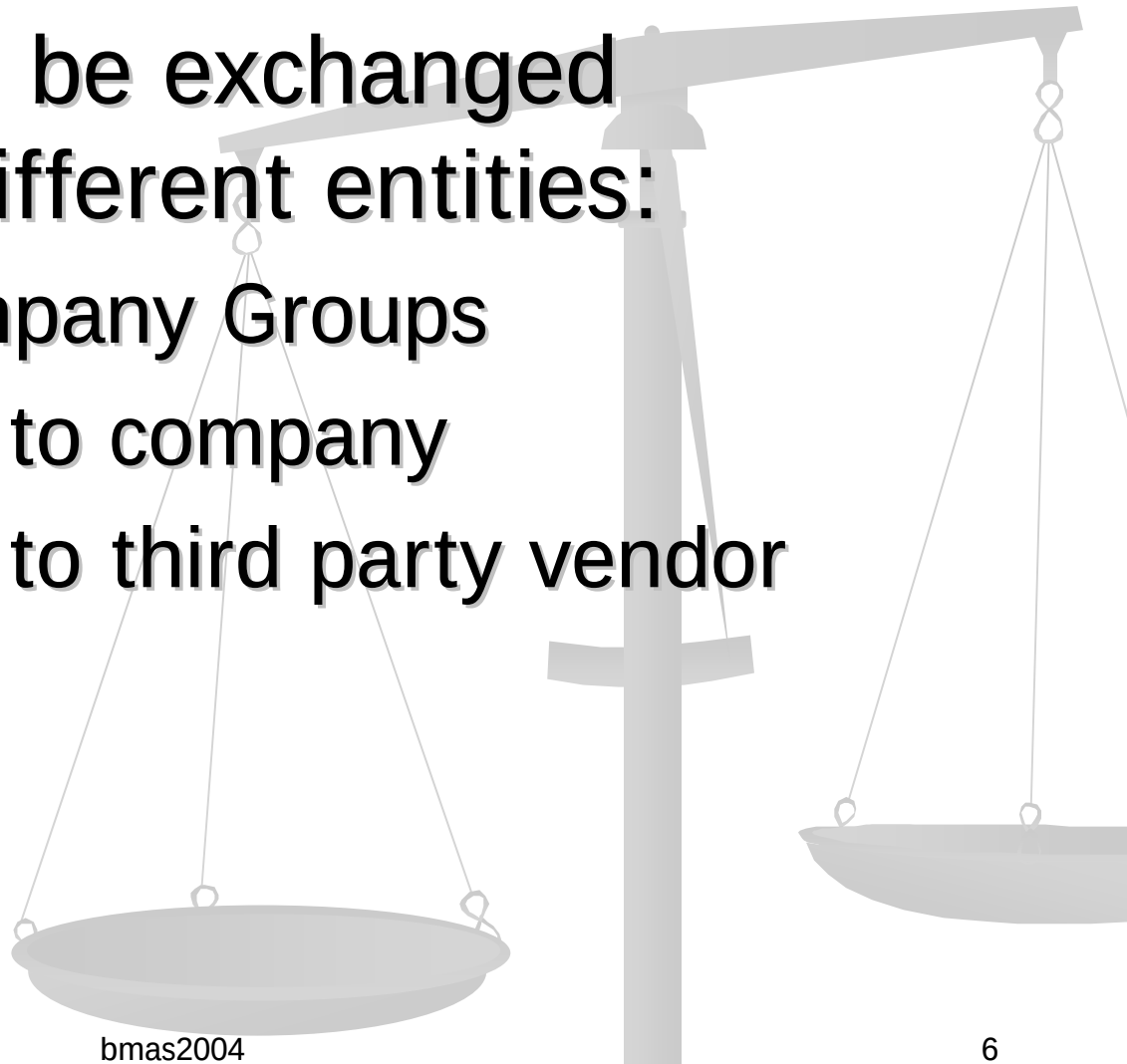
MSSoC Business

- ✓ As complexity increases, MSSoC business will be limited to a few participants, who can afford the development costs
- ✓ Intellectual Propriety (IP) development and sharing will allow smaller businesses to partner and share costs
- ✓ And ... sharing will automatically enable a new form of second source capability



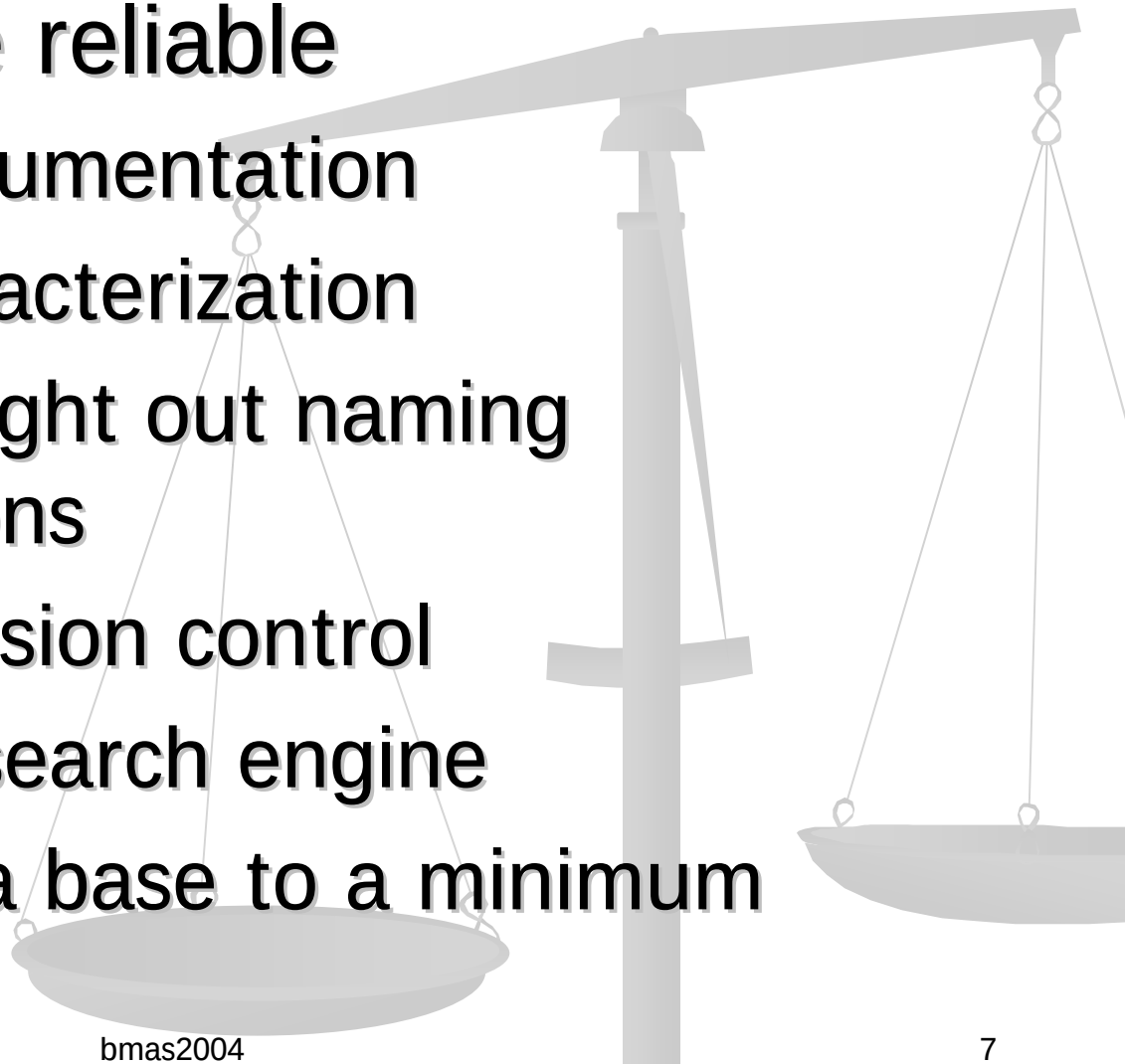
Intellectual Property

- IP that will be exchanged between different entities:
  - Inter-Company Groups
  - Company to company
  - Company to third party vendor



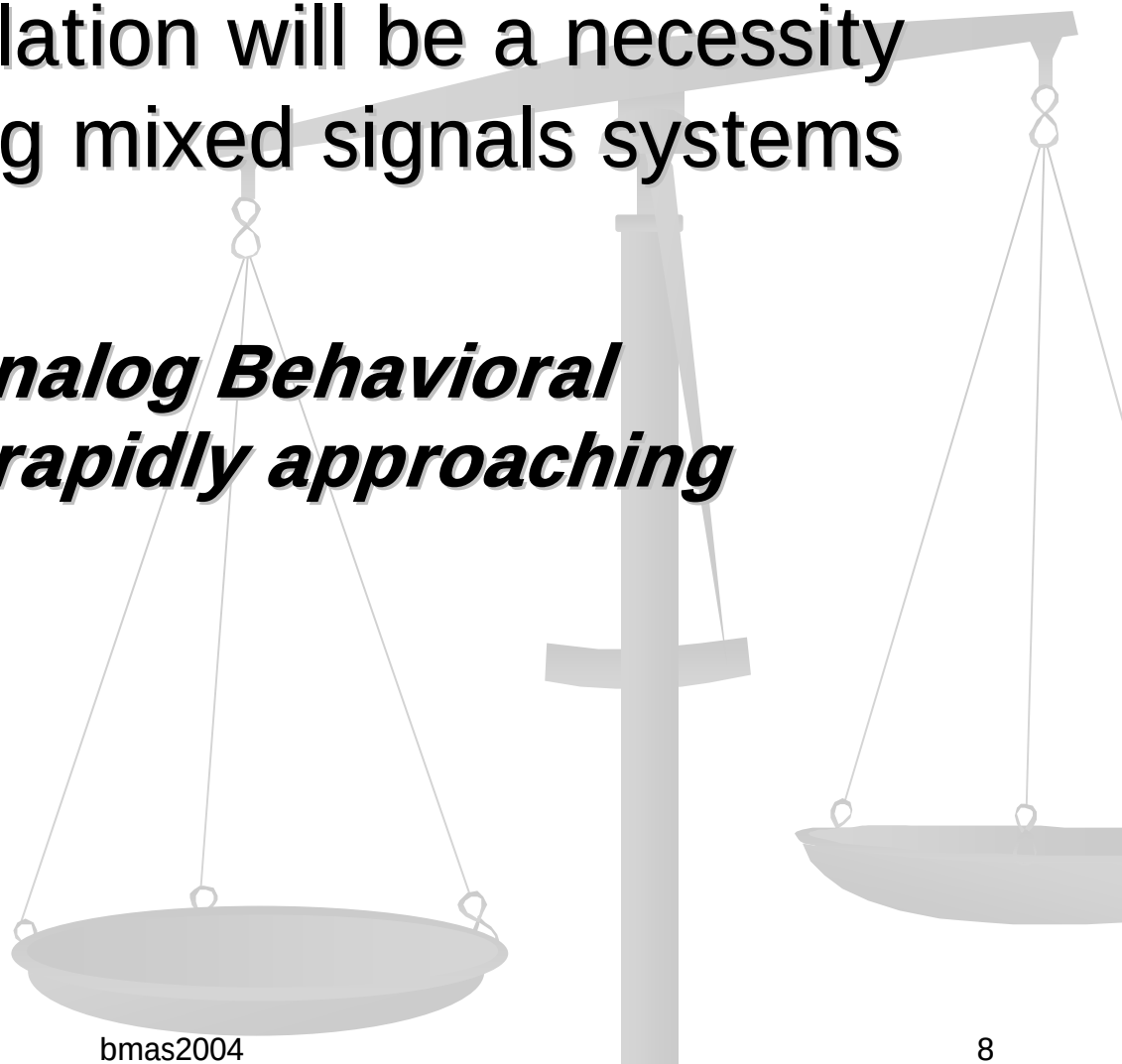
Intellectual Property

- ... must be reliable
  - Good documentation
  - Well characterization
  - Well thought out naming conventions
  - Good revision control
  - Efficient search engine
  - Keep data base to a minimum



Top Level Simulation

- ✓ Top level simulation will be a necessity for large analog mixed signals systems
  - ✓ ***The era of Analog Behavioral Modeling is rapidly approaching***

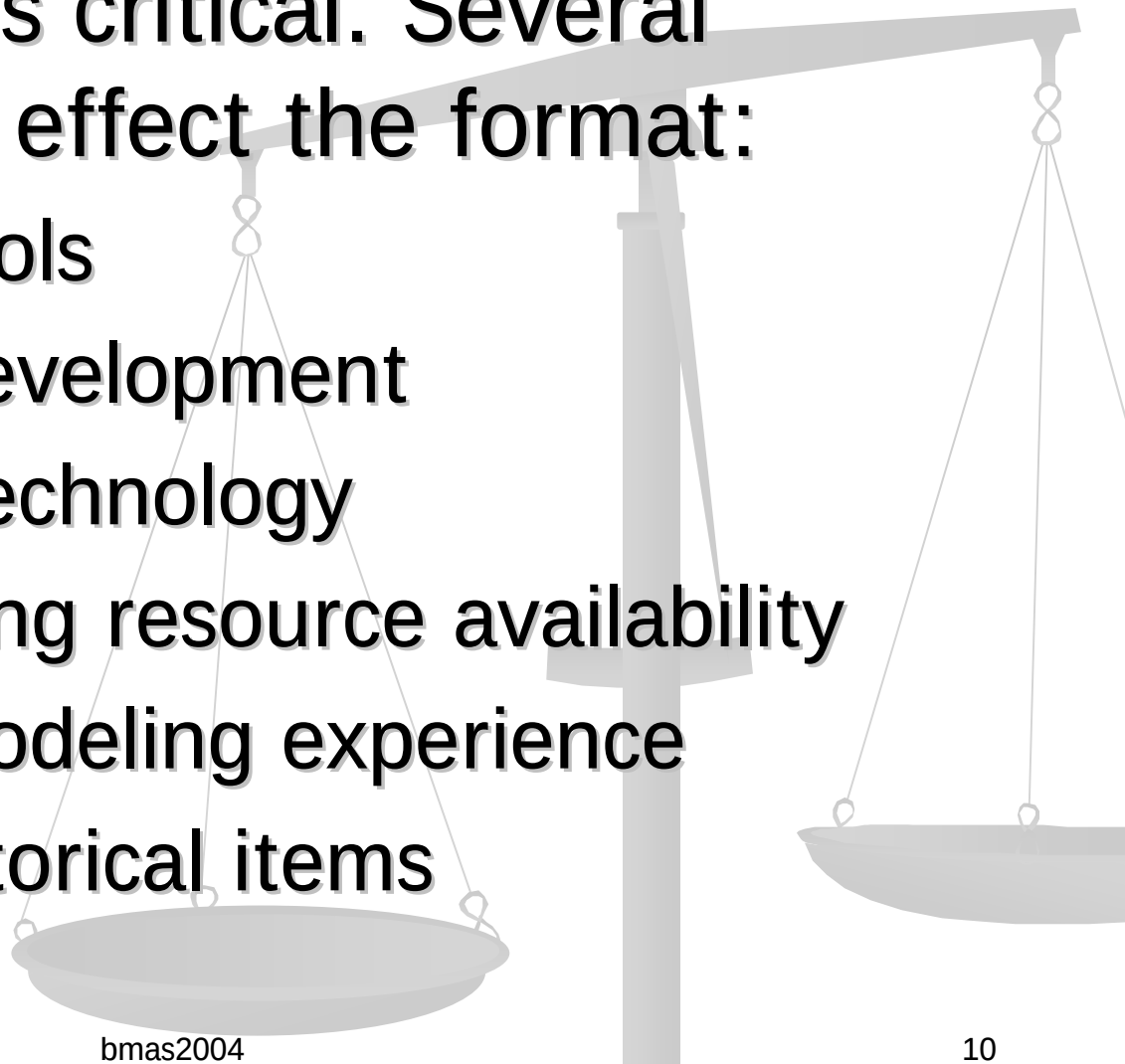


Specifications

- ✓ Sharing product development will require well defined “frozen” specifications
- ✓ Early top level simulation will be required to define the specification
- ✓ A well thought out strategy will be required to achieve a “specification traceable to silicon”

IP Sharing Issues

- IP format is critical. Several things can effect the format:
  - Design tools
  - Cost of development
  - Process technology
  - Engineering resource availability
  - Analog Modeling experience
  - Other historical items



Analog Model IP

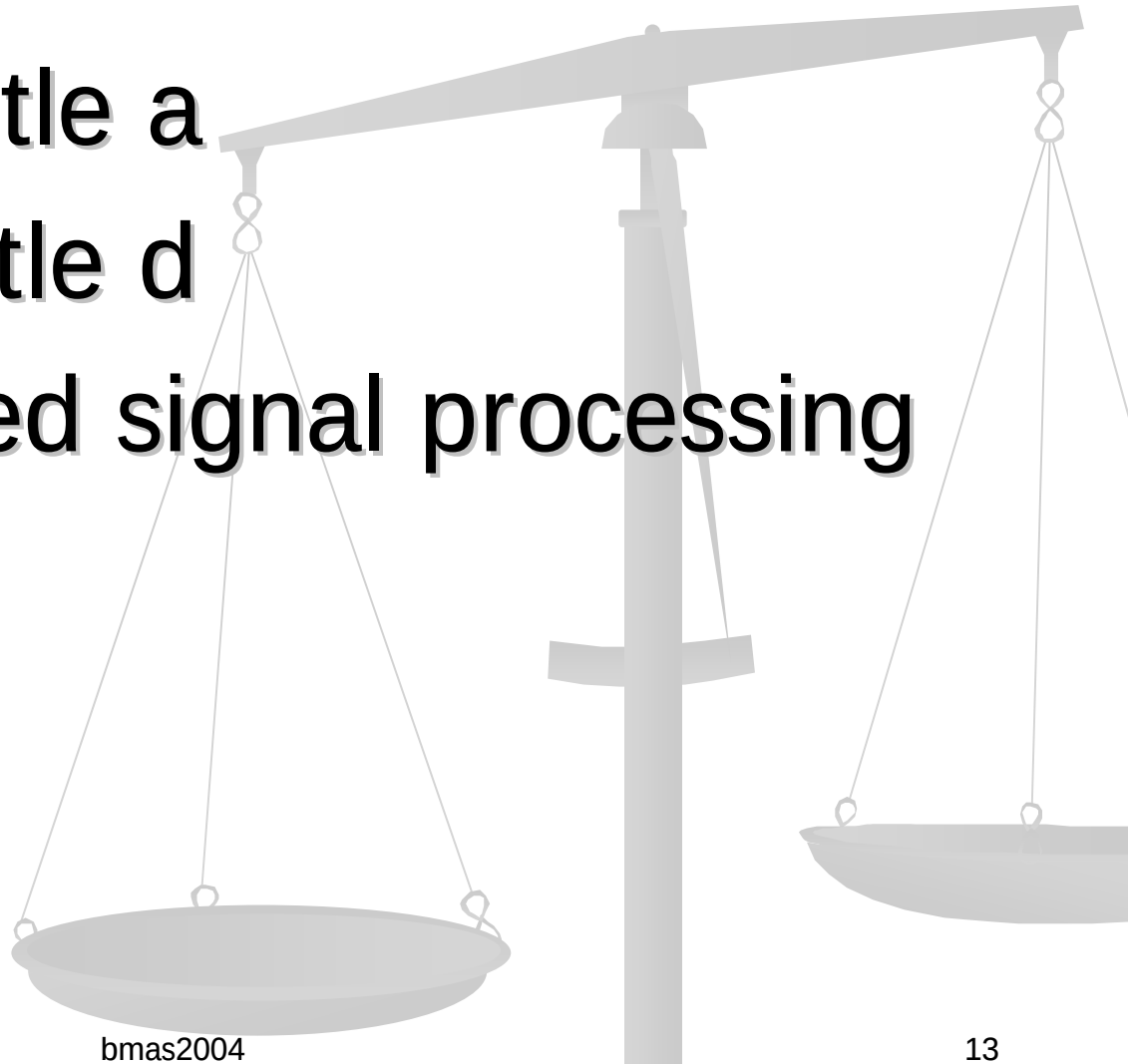
- ✓ Still difficult to reuse
- ✓ How to keep a database to a minimum number of accurate reliable models
- ✓ No consistent cataloging methodology can pose a problem
  - ✓ Naming conventions not well thought out
  - ✓ Revision controls vary
    - ✓ Major change
    - ✓ Minor change

Analog Blocks

- ✓ Have different architectures due to:
  - ✓ Design tools
  - ✓ Cost
  - ✓ Process
  - ✓ Resources
  - ✓ Expertise and other historical reasons
- ✓ IP from different sources usually do not interface well to each other

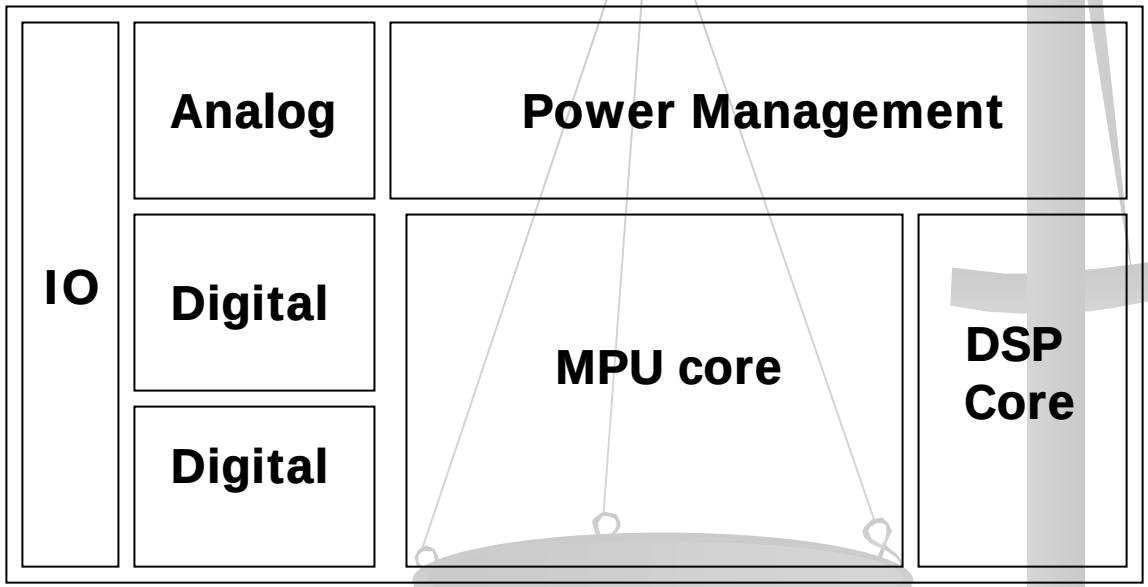
Mixed Signal ICs

- ✓Big D – little a
- ✓Big A – little d
- ✓Multi-mixed signal processing



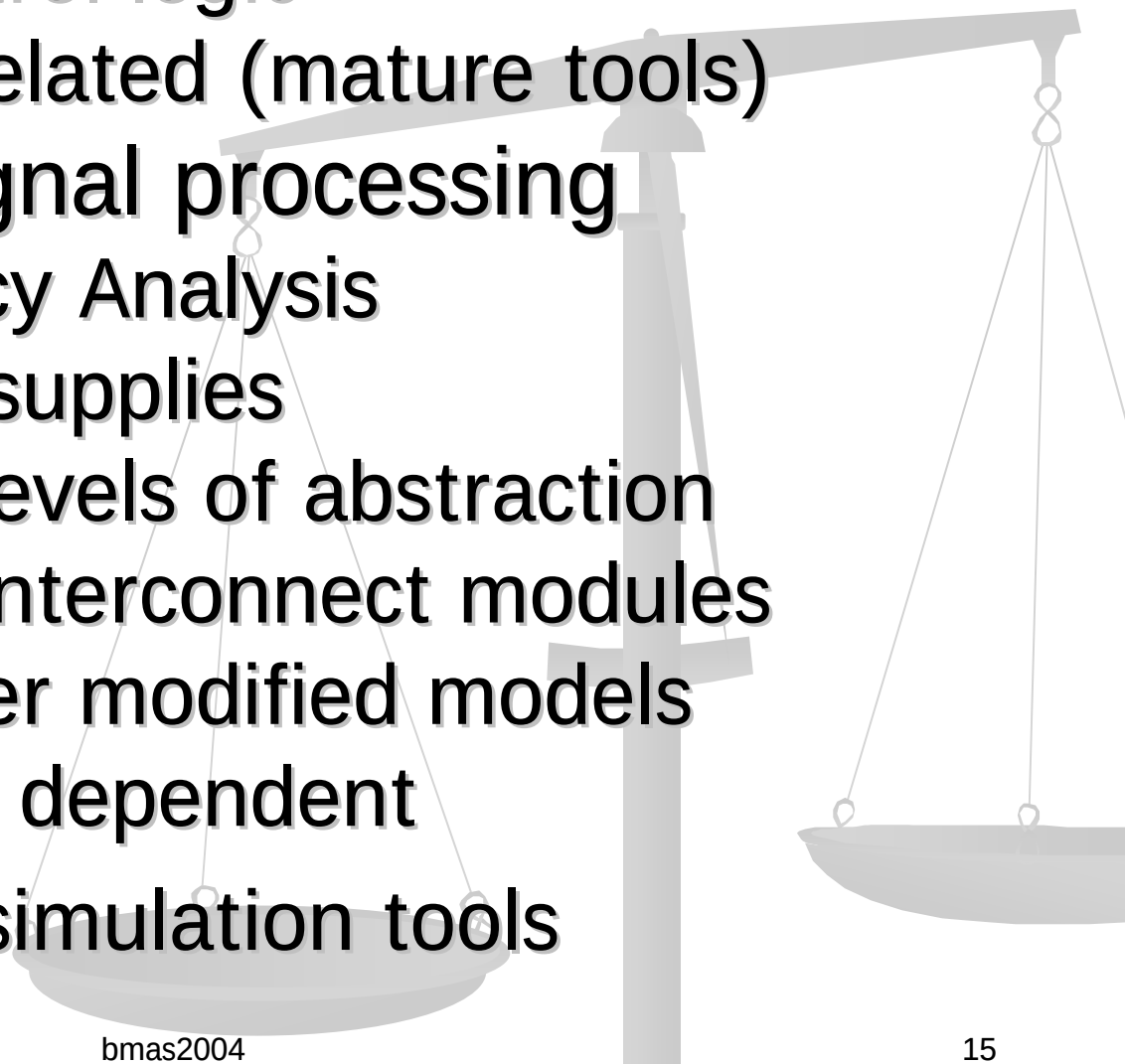
Big D - little a

- ✓ The digital blocks have a good tool support
- ✓ Analog blocks have a mix of immature tool support



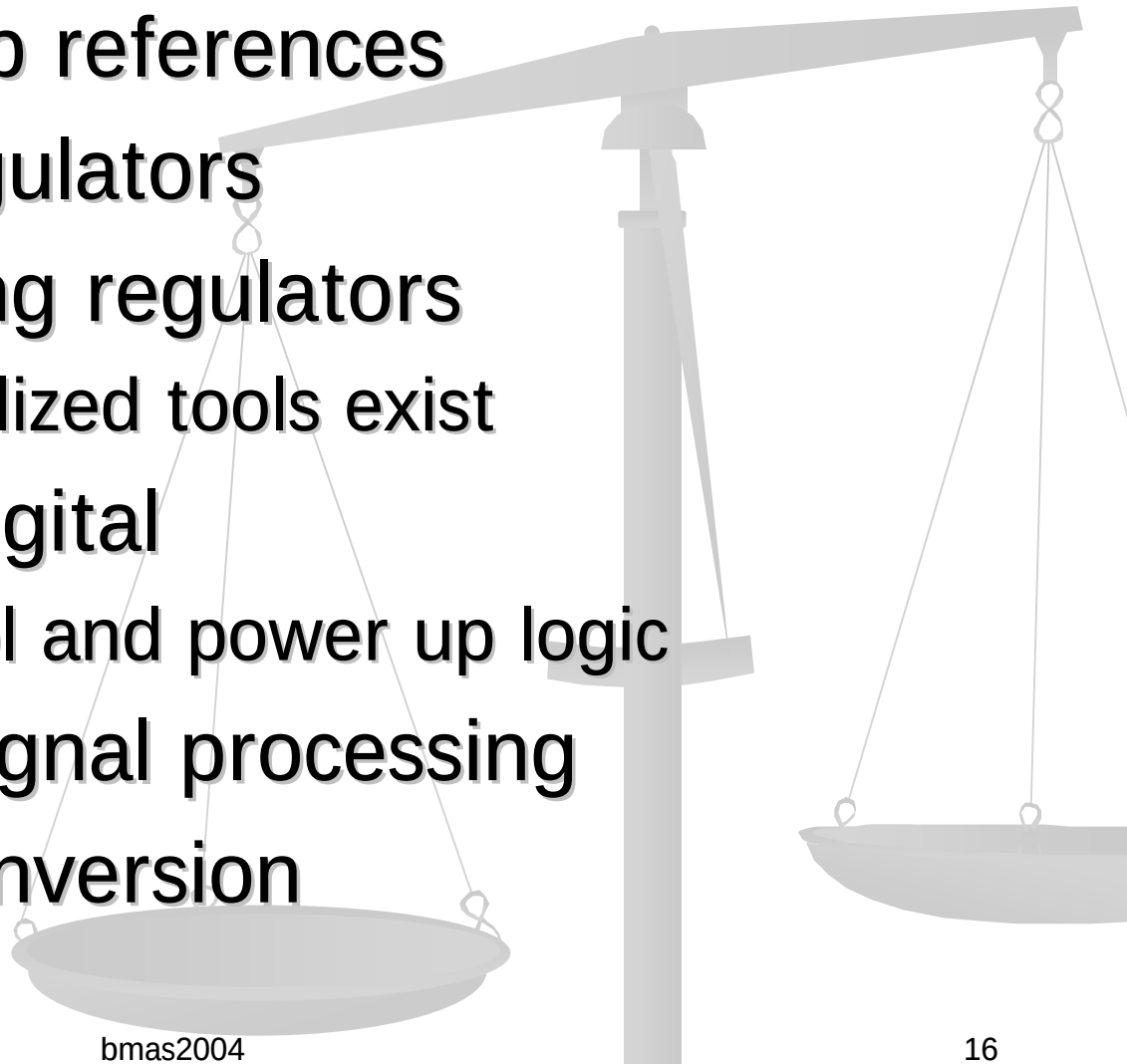
Big A – little d

- ✓ Power management
  - ✓ Digital control logic
    - ✓ Verilog related (mature tools)
  - ✓ Analog signal processing
    - ✓ Frequency Analysis
    - ✓ Multiple supplies
    - ✓ Various levels of abstraction
    - ✓ Various interconnect modules
    - ✓ Parameter modified models
    - ✓ More pin dependent
    - ✓ Custom simulation tools



Big A – little d
(Spice spoken here)

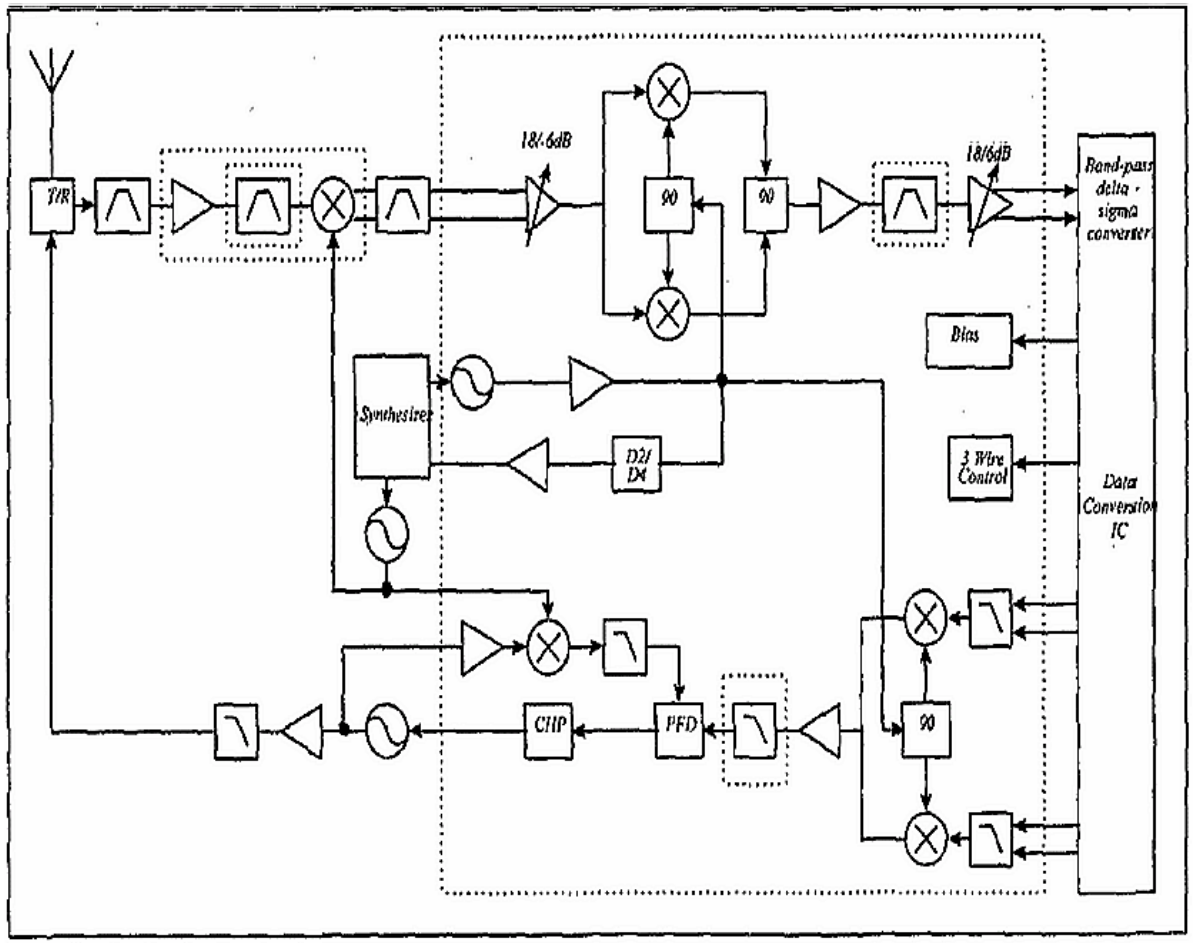
- ✓ Bandgap references
- ✓ LDO regulators
- ✓ Switching regulators
  - ✓ Specialized tools exist
- ✓ Some digital
  - ✓ Control and power up logic
- ✓ Audio signal processing
- ✓ Data conversion



Multi-mixed Signal Processing

Transceiver

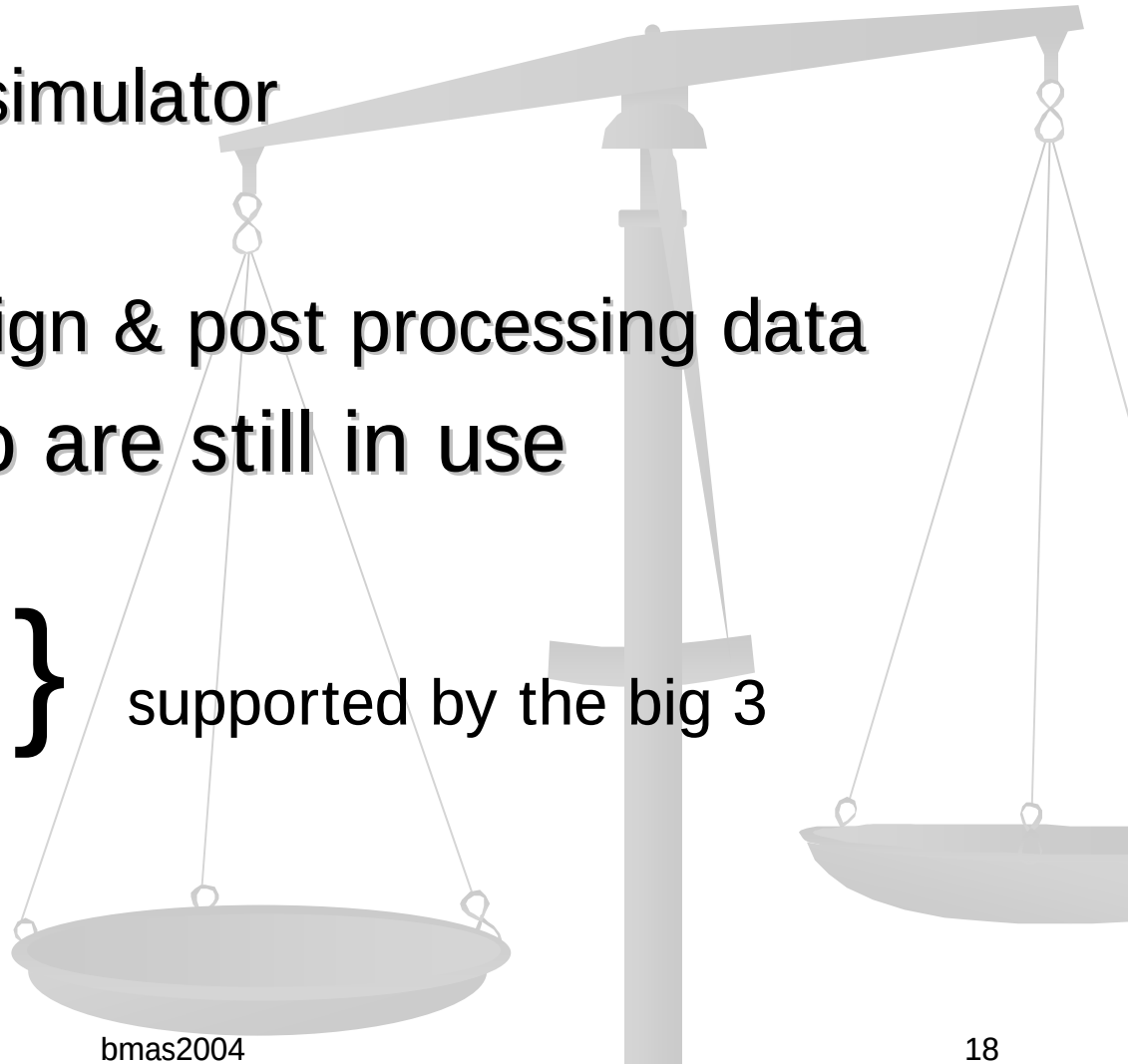
>>stub<< cells are used to verify connectivity



Analog Simulation Tools

- ✓ Spice
  - ✓ Dominate simulator
- ✓ MathLab
  - ✓ System design & post processing data
- ✓ Saber & Eldo are still in use
- ✓ VHDL-AMS
- ✓ Verilog-A
- ✓ Verilog-AMS

} supported by the big 3



Mixed Signal Design Flow

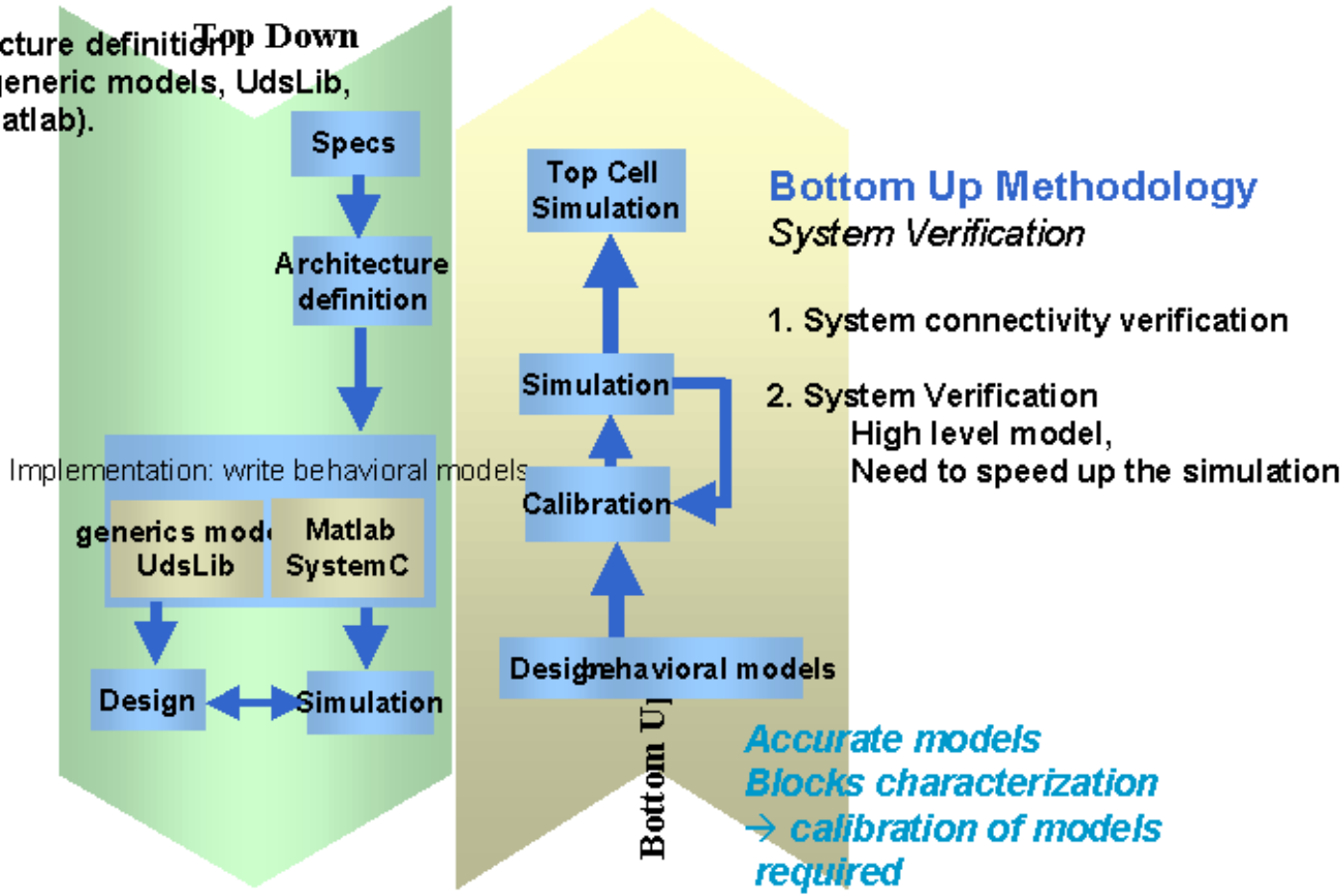
Top Down Methodology

System implementation

(power management example)

1. System Validation

2. New architecture definition
   (Use of generic models, UdsLib,
   Use of matlab).



Bottom Up Methodology

System Verification

1. System connectivity verification

2. System Verification
   High level model,
   Need to speed up the simulation

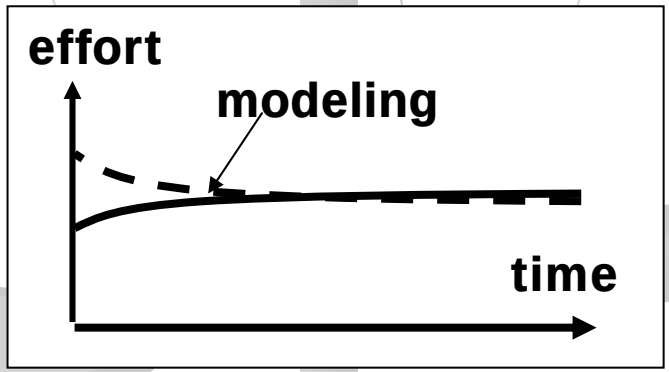
Accurate models
Blocks characterization
→ calibration of models required

Mixed Signal Design Flow Tool Set Example

Vendor	Cadence	Mentor	Synopsys
Behavioral Language based	Verilog-AMS	VHDL-AMS Verilog-AMS	VHDL-AMS Verilog-AMS
AMS Simulator Tool	AMS-Designer	ADV-AMS	Discovery-AMS
Suported Description levels	Verilog-D Verilog-A Verilog-AMS Transistor level Gate level	Verilog-D Verilog-A Verilog-AMS Transistor level Gate level	Verilog-D Verilog-A Verilog-AMS Transistor level Gate level
FAST-SPICE Tool	ULTRASIM	MACH-TA	NANOSIM
AMS+Fast Spice Solution	AMS-ULTRA	ADV-AMS	Discovery-AMS

Analog Modeling Development

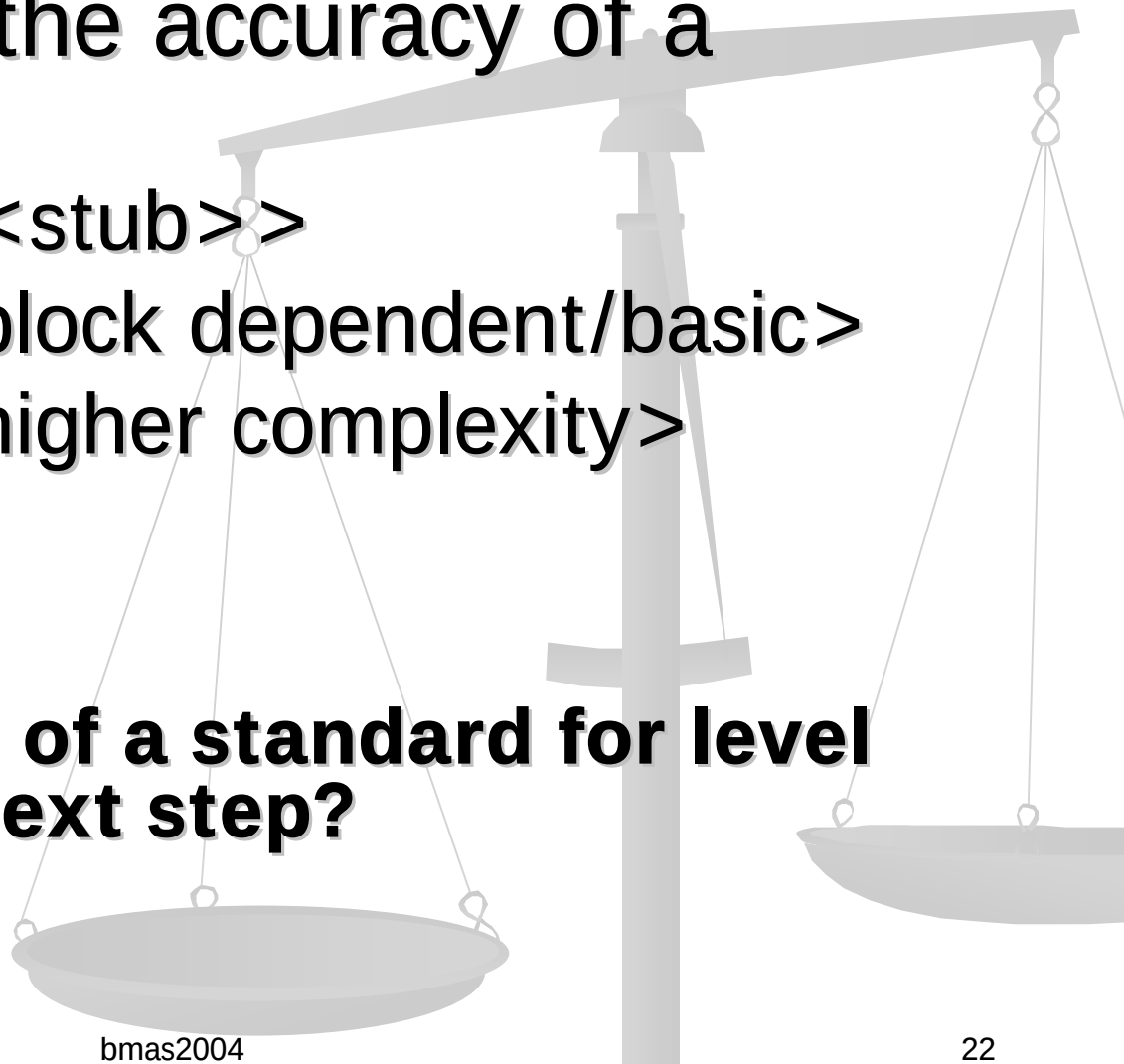
- ✓ AM is related to what is affordable
- ✓ Larger companies are forming centralized model development
  - ✓ Smaller companies are left out
- ✓ AM is a function of available tool sets, time and engineering resources to take on the burden of development and characterization



Analog Models & Verification

- What defines the accuracy of a model?
  - Level 0 <<stub>>
  - Level 1 <block dependent/basic>
  - Level 2 <higher complexity>
  - Level n

- **Is some form of a standard for level definition a next step?**

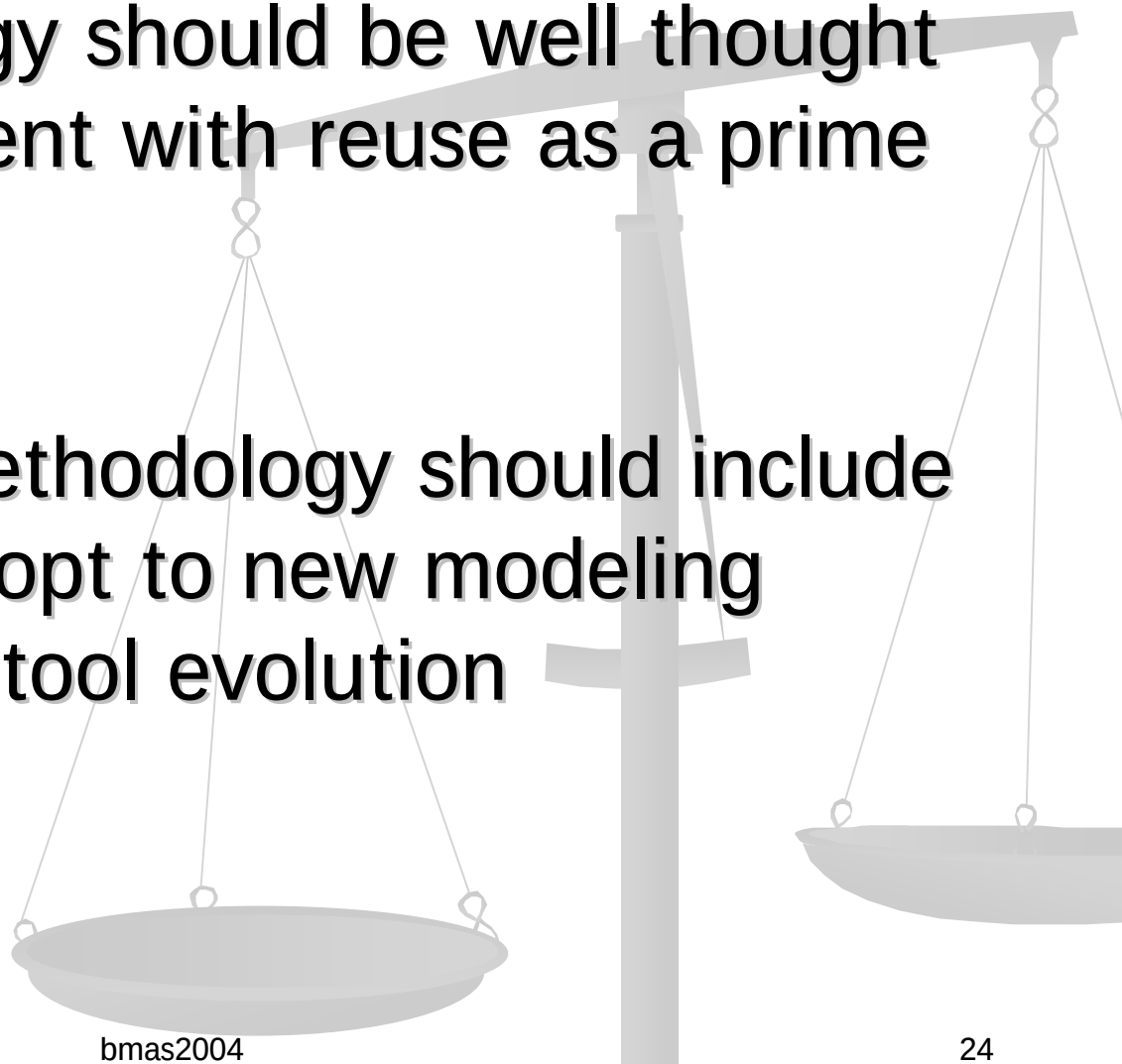


Levels of Abstraction

- ✓ Stub cells and basic generic cells
  - ✓ Used for connectivity verification
  - ✓ Full chip verification
  - ✓ Test development (results to MatLab)
- ✓ More advanced generic cells
  - ✓ Functional verification
  - ✓ Full chip verification
  - ✓ Test development
- ✓ Detailed cells used sparely with generic
  - ✓ Block verification and characterization
  - ✓ Traceability to silicon
    - ✓ Functional model parameters that are related to process parameters

Analog Modeling Methodology

- ✓ The methodology should be well thought out and consistent with reuse as a prime goal
- ✓ A part of the methodology should include the ability to adopt to new modeling techniques and tool evolution



Analog Behavioral Models

- ✓ Development tools are appearing
- ✓ Quite a lot of activity in the past couple of years
- ✓ But ... ad hoc modeling techniques ... and no clear methodology exists for the development of Analog IP
  - ✓ Would a standard help or will the tools drive consistency?

Analog Model Test Benches

- ✓ Test benches should be included with all analog behavioral models, allowing automated simulation and automated results presentation in a consistent repeatable format
- ✓ Be able to make speed & accuracy trade-offs to accommodate System evaluation, Circuit analysis, Final Test Development, Applications, and failure analysis

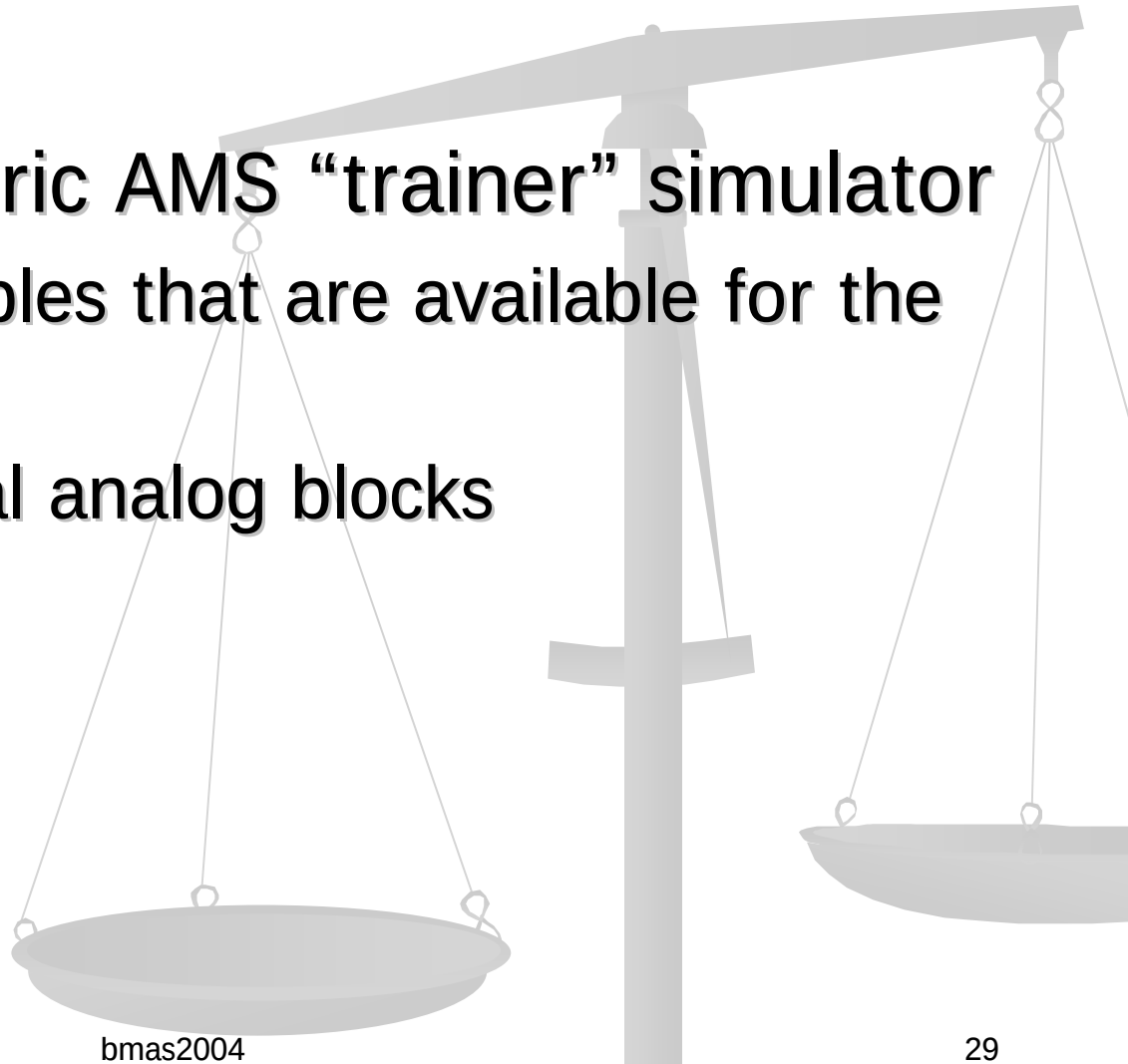
Feature Requests

- ✓ Tools to automatically generate Analog Models from schematic descriptions
- ✓ Hooks to the models for simulation speed and accuracy tradeoff selection
- ✓ Full test development potential
- ✓ Technology transfer capability
- ✓ Better parameterization features to allow traceability to silicon

Analog Behavioral Modeling (Training)

- ✓ Tool vendor courses are available
  - ✓ But they are costly and take the analog designer off the project
- ✓ University courses are emerging
  - ✓ But they do not train the seasoned analog designer
- ✓ Internet classrooms are emerging
  - ✓ But a simulator to support that environment is not readily available.

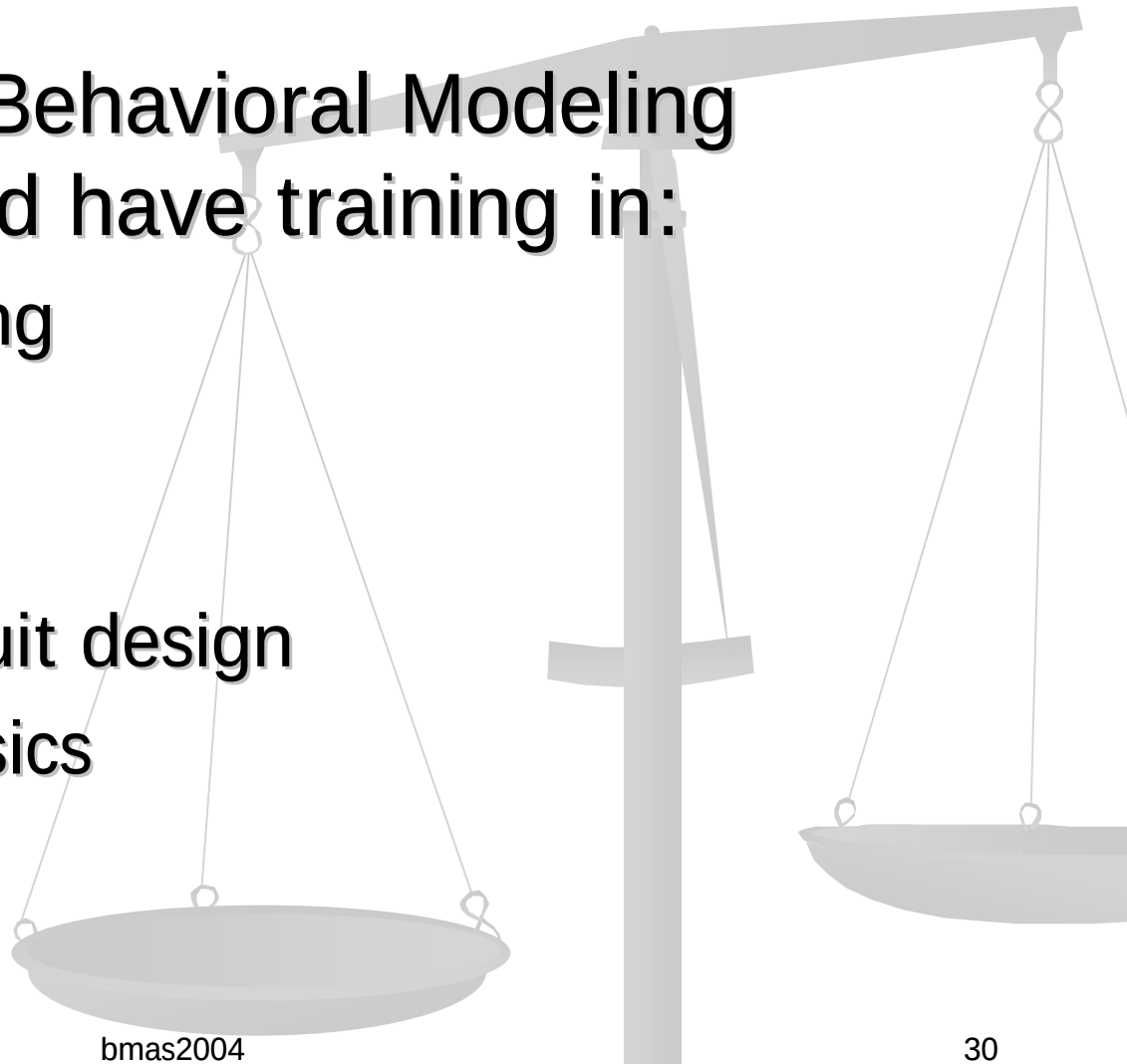
Analog Behavioral Modeling (Training Wish List)



- ✓ A low cost generic AMS “trainer” simulator
  - ✓ Plenty of examples that are available for the simulator
  - ✓ Ability to do real analog blocks

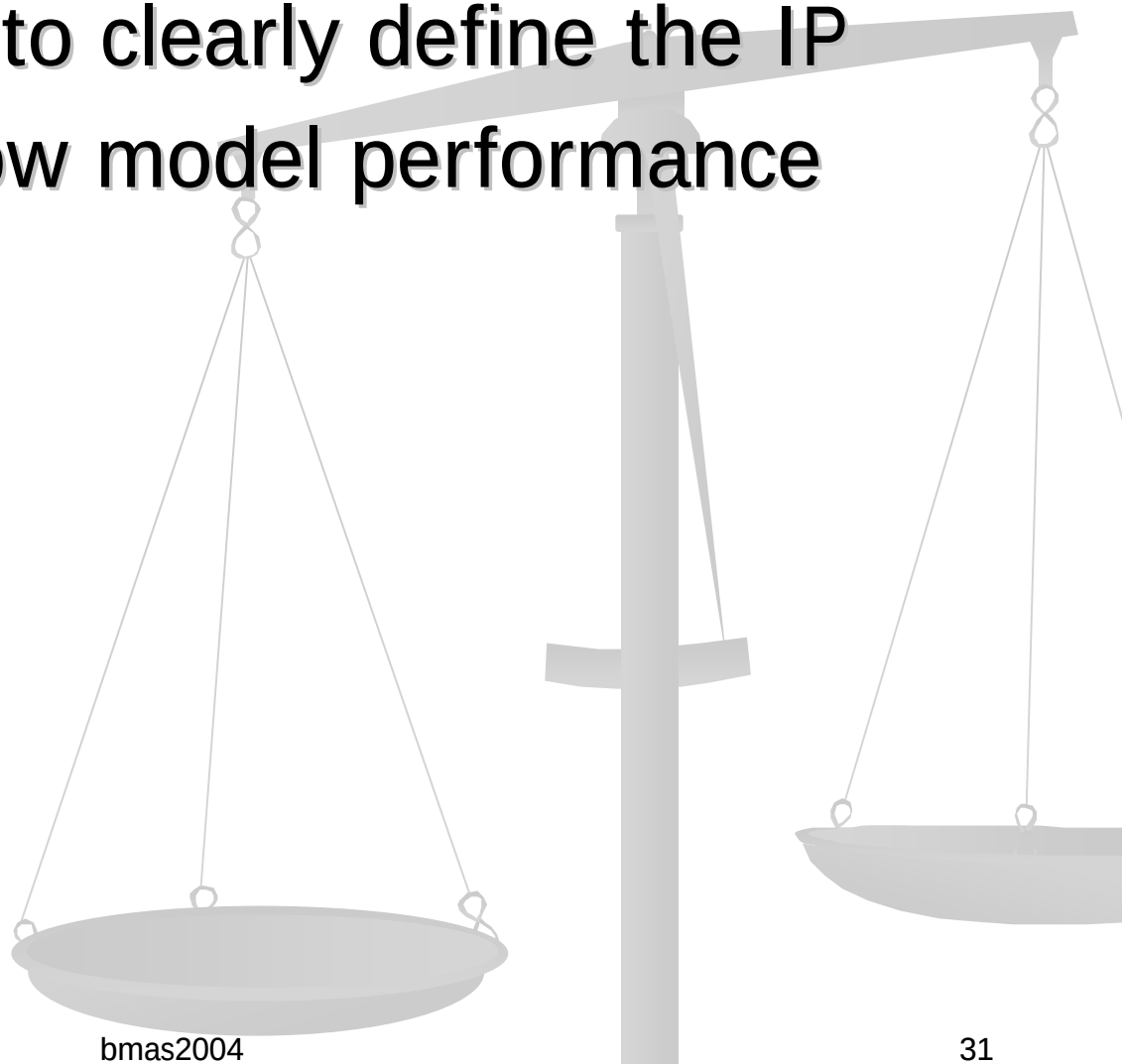
Analog Behavioral Modeling (Training Observation)

- The Analog Behavioral Modeling expert should have training in:
  - Programming
  - Verilog
  - Spice
  - Analog circuit design
  - Device physics



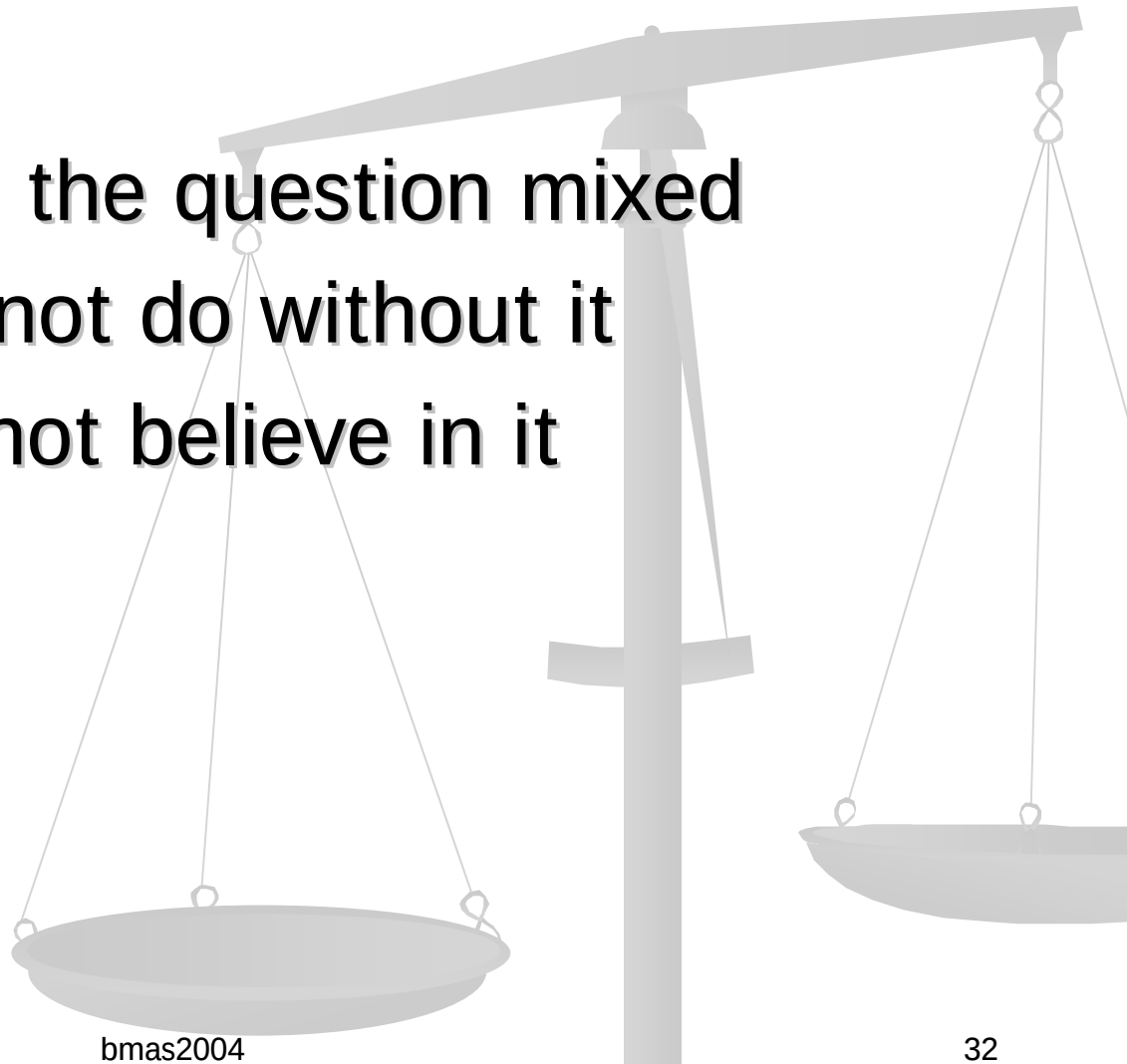
Documentation

- ✓ Documentation to clearly define the IP
- ✓ Results that show model performance results



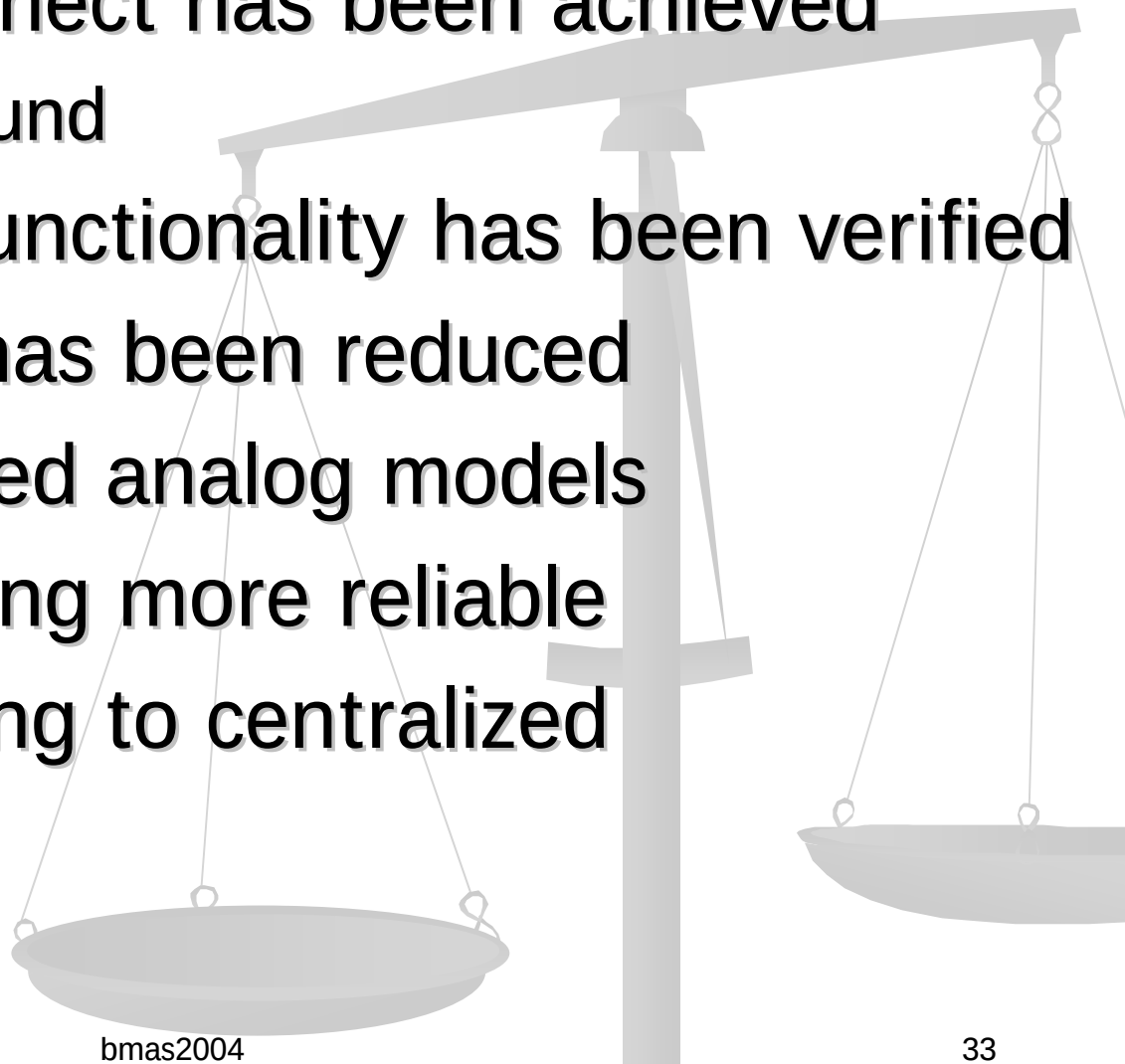
Is Analog Modeling being used?

- ✓ Response to the question mixed
  - ✓ Some cannot do without it
  - ✓ Some do not believe in it



Comments - pros

- ✓ Full chip interconnect has been achieved
  - ✓ Several errors found
- ✓ Power on reset functionality has been verified
- ✓ Simulation time has been reduced
- ✓ Reuse has included analog models
- ✓ Tools are becoming more reliable
- ✓ Modeling is moving to centralized organizations



Comments - cons

- ✓ Has taken longer to evolve than initially expected
- ✓ Limited training tools have appeared
- ✓ Hard to allocate engineering resources to developing and verifying models
- ✓ Some have refused to adopt it at all
  - ✓ Want full transistor simulation before level sign off
  - ✓ Claim the pay back for the investment is not enough