Modeling Thermal Induced Inter-Symbol Interference of Feedback DACs in Delta-Sigma Modulators

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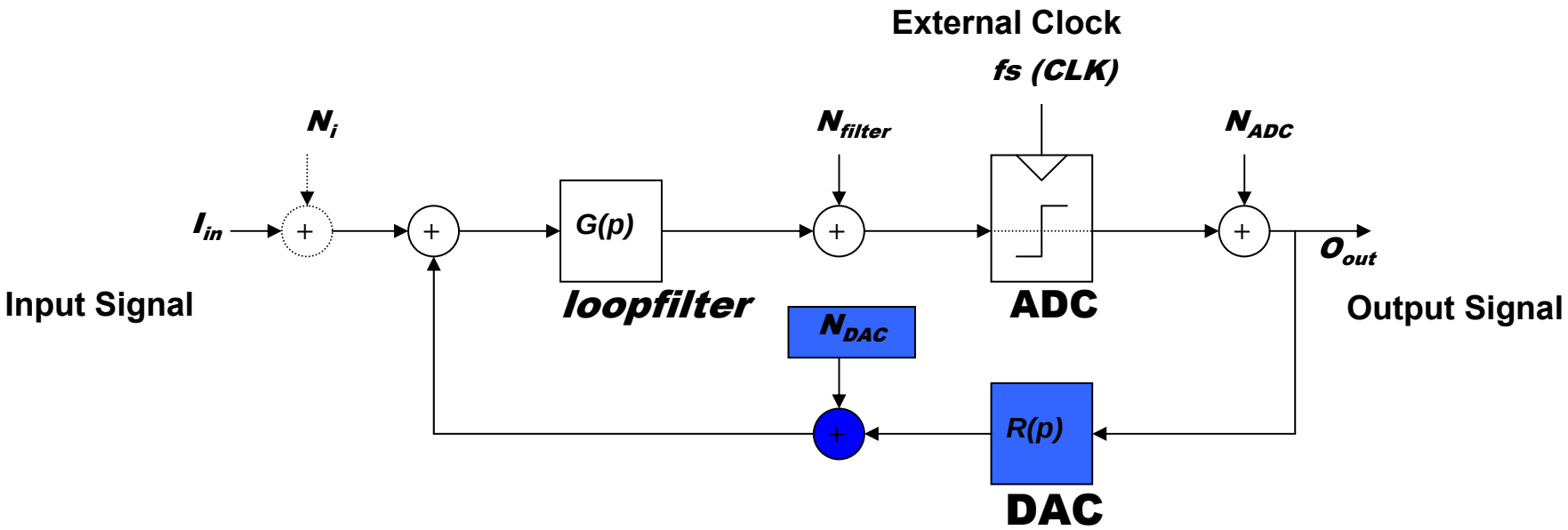
Outline

- DAC noise in Continuous Time Delta-Sigma Modulator
- Thermal Induced Inter-Symbol Interference (ISI)
- Top-level Model of Thermal Induced ISI in Delta-Sigma Modulators
- Case Study : 2nd Order $\Delta\Sigma$ Modulator designed using IBM's 7HP BiCMOS Process
- Summary and Conclusion

Continuous Time ΔΣ Modulator with Noise Sources

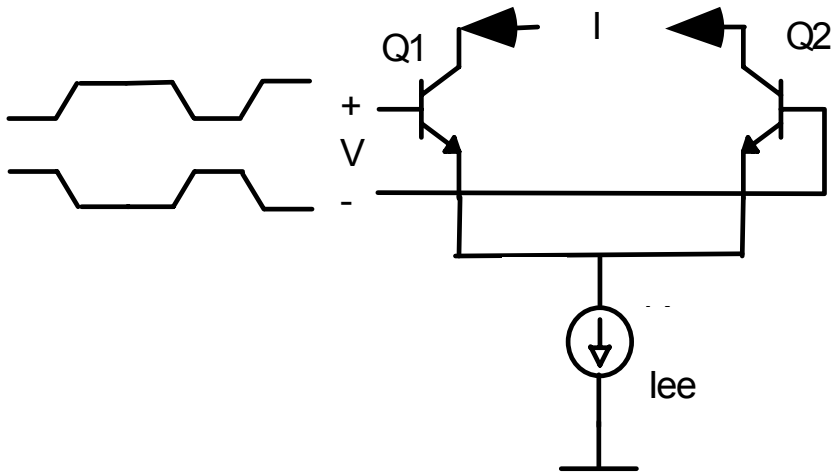


Equivalent Input Noise Power

$$N_i = \frac{N_{filter}}{\int_{\omega=0}^{\infty} |G(j\omega)|^2} + N_{DAC}$$

DAC noise is not reduced by loop filter gain

Temperature Mismatch in Current Steering DAC



Current Steering DAC

ON Transistor Q1

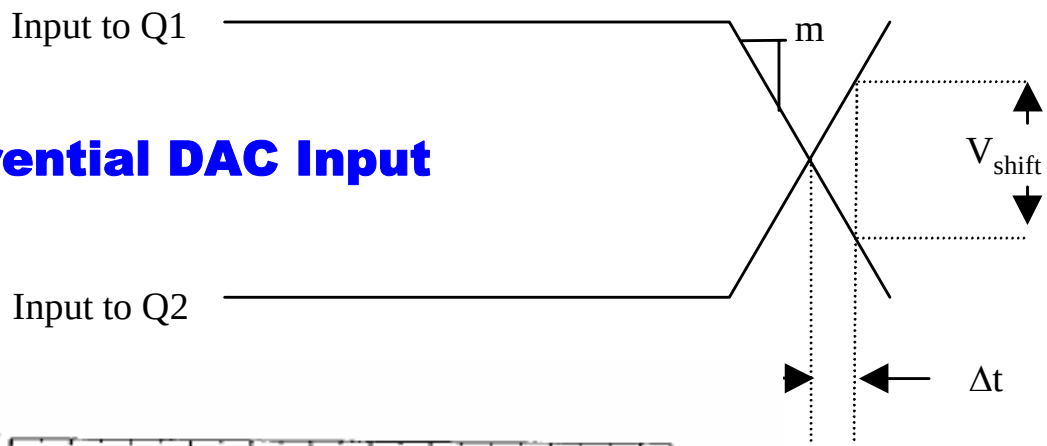
$$T_1(n) = e^{-P/\tau} T_1(n-1) + T_0(1-e^{-P/\tau}) + \Delta T(1-e^{-P/\tau})\,|S(n-1)|$$

OFF Transistor Q2

$$T_2(n) = e^{-P/\tau} T_2(n-1) + T_0(1-e^{-P/\tau}) - \Delta T(1-e^{-P/\tau})\,|S(n-1)|$$

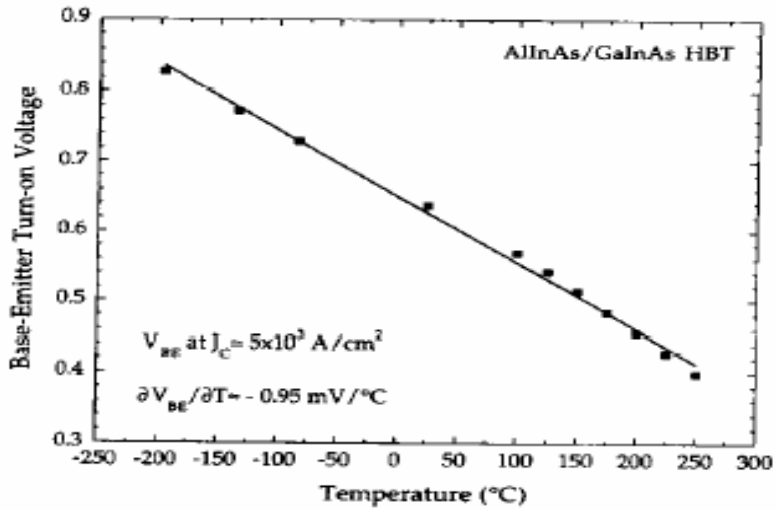
P = Time step
t = Thermal time constant
T_0 = Ambient temperature
ΔT = Max Temperature mismatch
S(n) = Input Signal

Thermal Induced Inter-Symbol Interference



Differential DAC Input

$$\Delta t(n) = \frac{V_{shift}(n)}{2m}$$

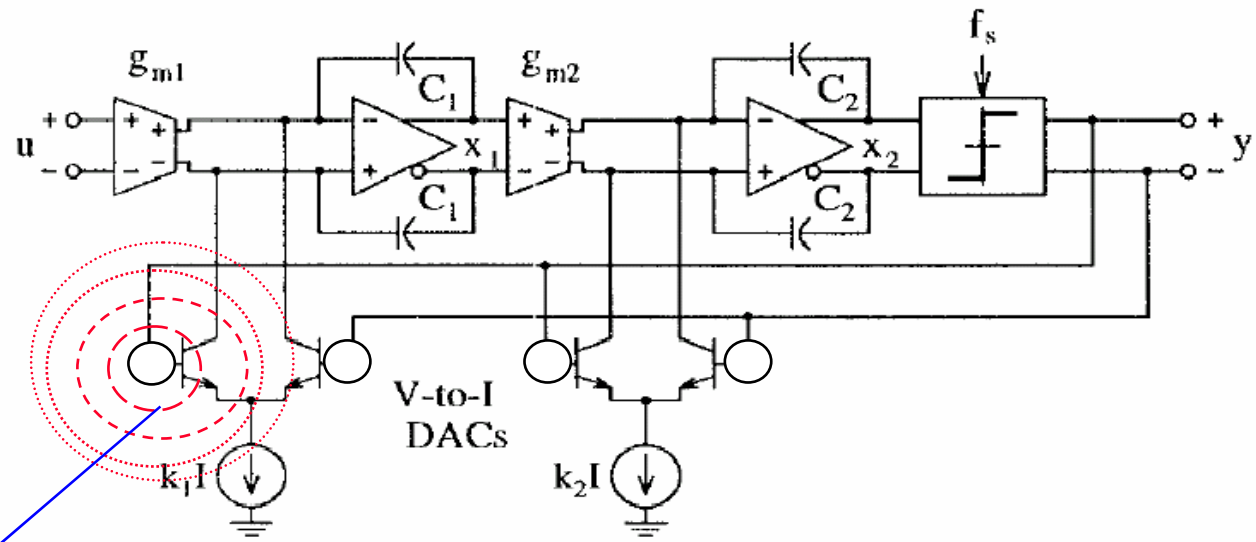


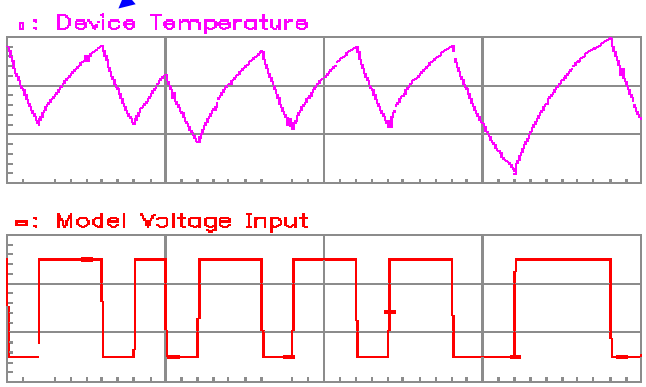
$$V_{shift}(n) = V_{be1}(n) - V_{be2}(n)$$
$$= c(T_1(n) - T_2(n))$$

Base-Emitter Voltage versus Temperature

Temperature mismatch leads to shift in switching time

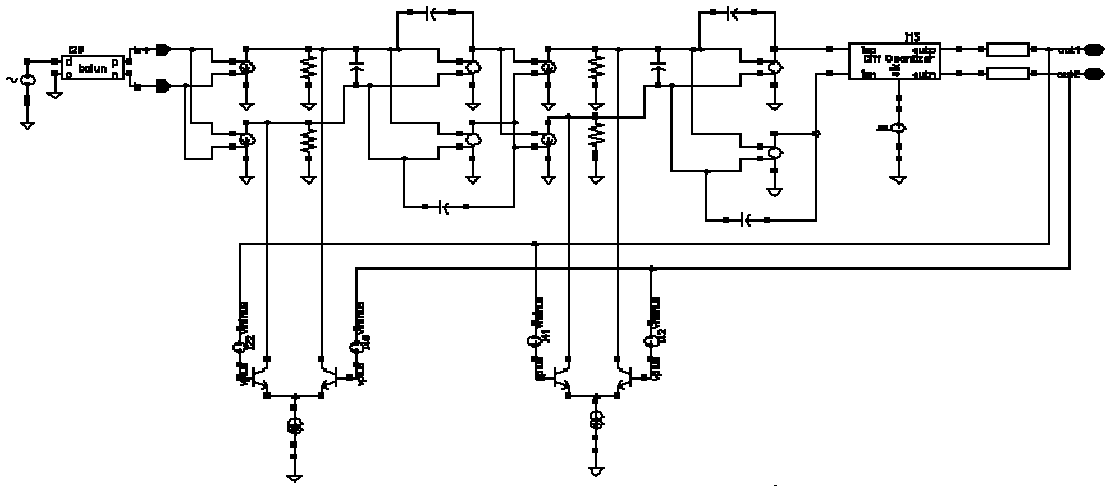
2nd Order Continuous Time ΔΣ Modulator with Thermal Induced ISI





Thermal Time constant	**2 ns**
Quantizer Output Rise/Fall Time	**50ps/50ps**
dV_{be}/dT	**1.11 mV/°C**
Time-Step	**50ps**
Ambient Temperature (T_0)	**310°K**
Min–Max equilibrium Temp	**300°K-320°K**

Baseline Behavioral Model

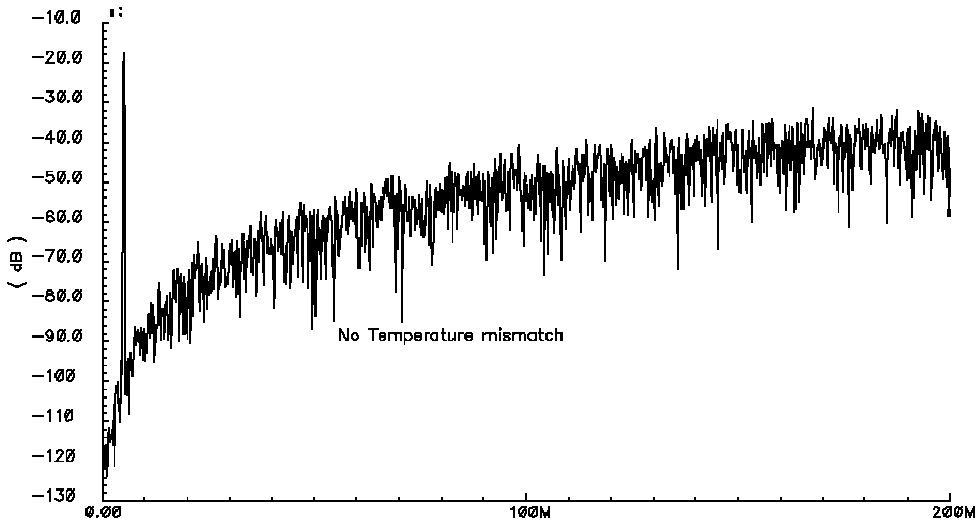


Parameters for 2nd Order CTΔΣ modulator

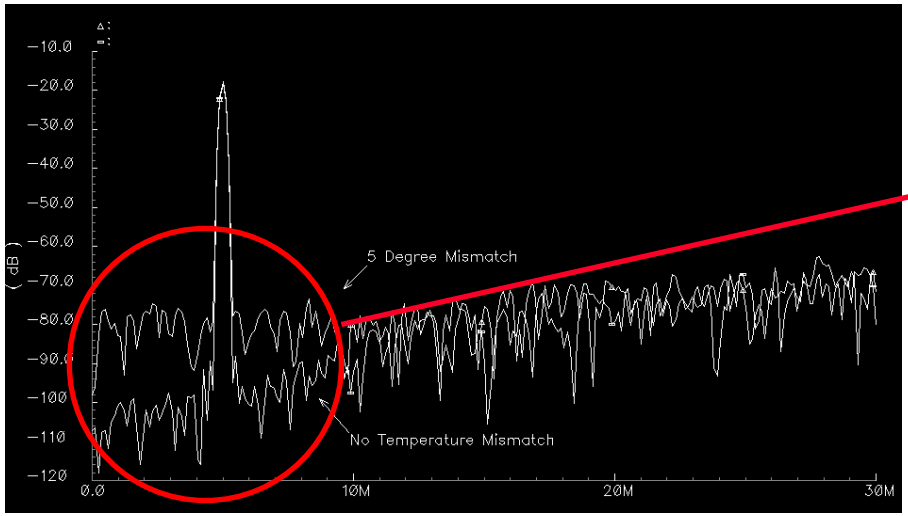
G_{m1}	500uA/V	G_{m2}	500uA/V
C1	2pF	C2	2pF
K_1	2.13mA	K_2	1.34mA
f_s	1 GHz	f_{in}	5MHz

Frequency Spectrum

No Temperature Mismatch



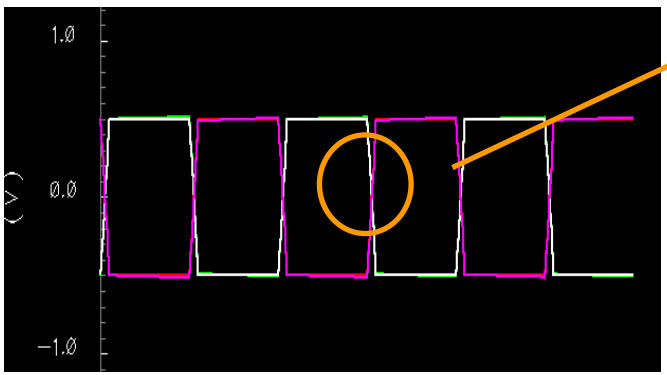
Simulation Results using Baseline Model

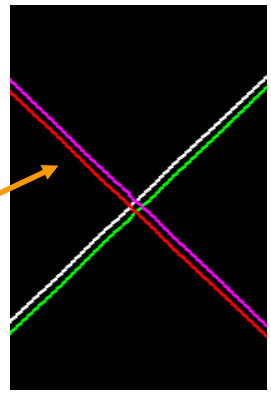


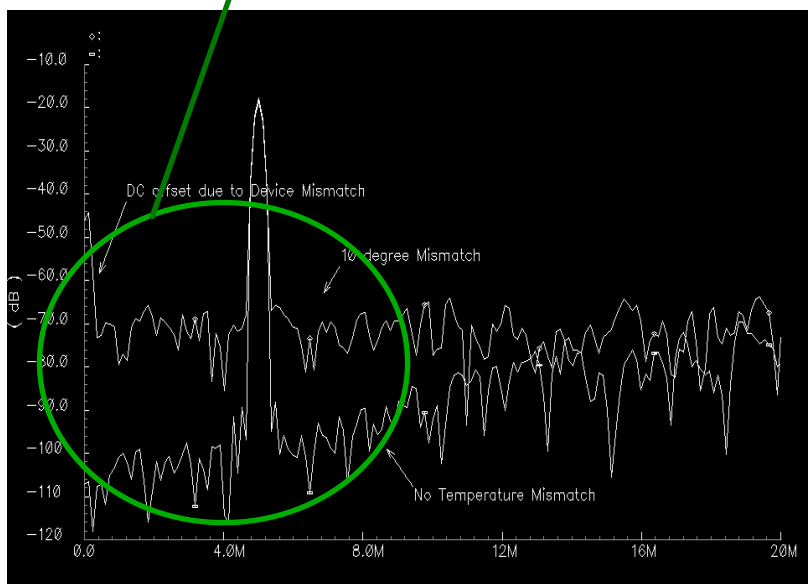
5°C Temperature mismatch causes 10 dB degradation in SNR

10°C Temperature mismatch causes 15 db degradation in SNR

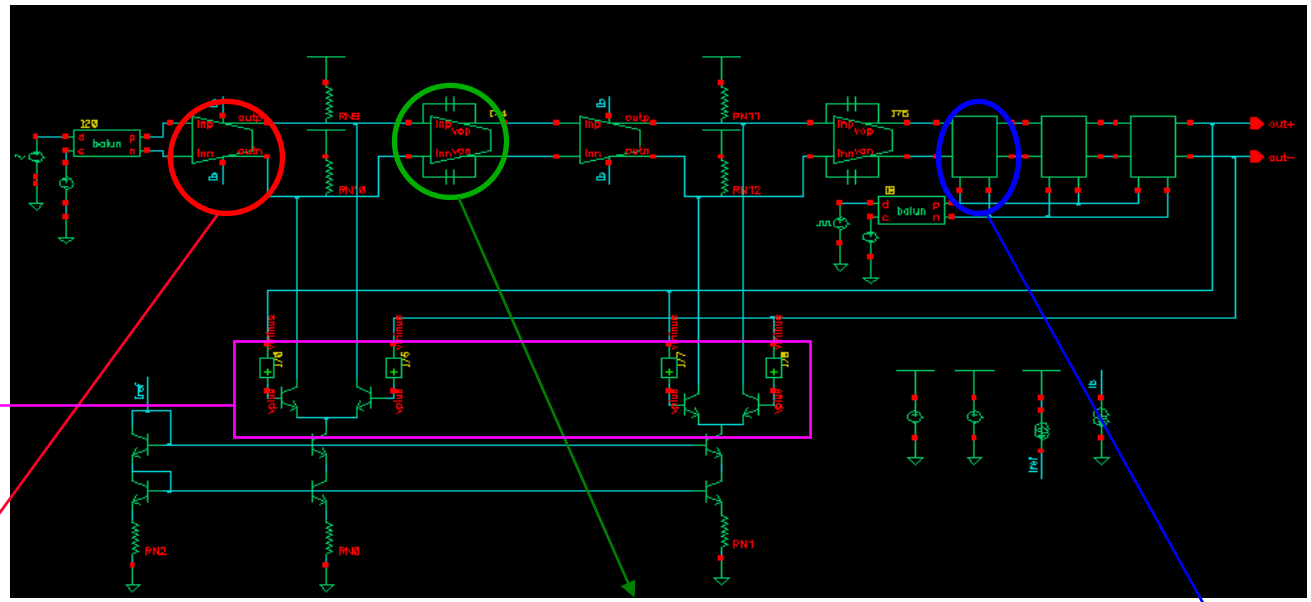
Output showing shift in Δt



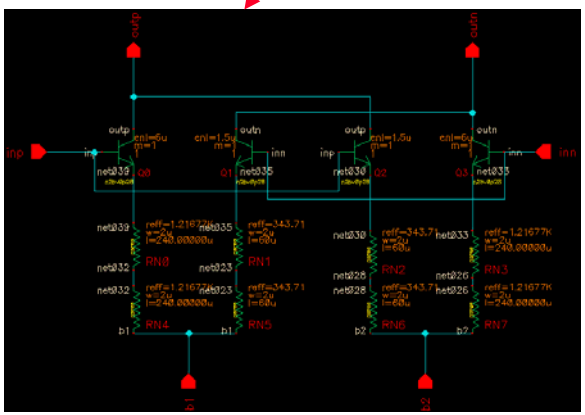




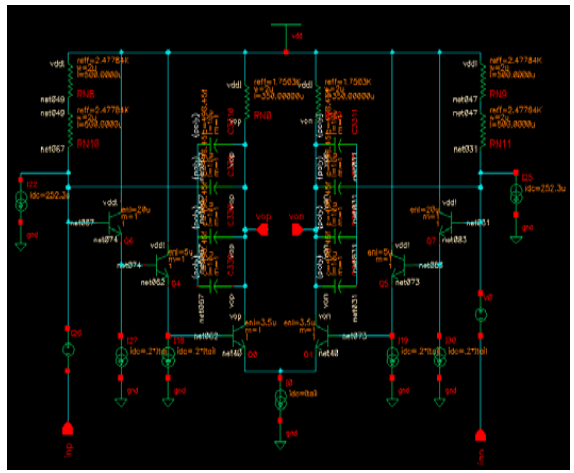
Transistor-level Model : 2nd Order ΔΣ Modulator with IBM's 7HP BiCMOS Process



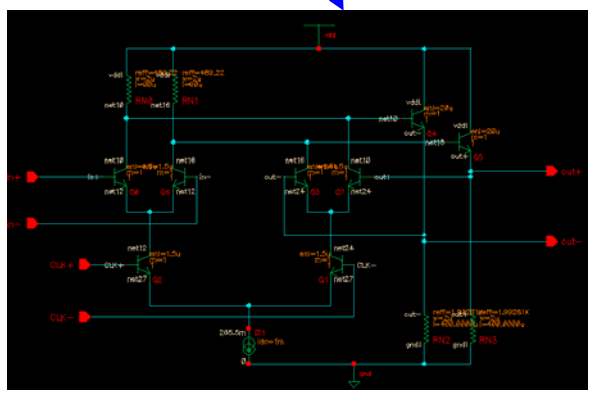
DAC with Thermal Induced ISI model



Gm-Cell

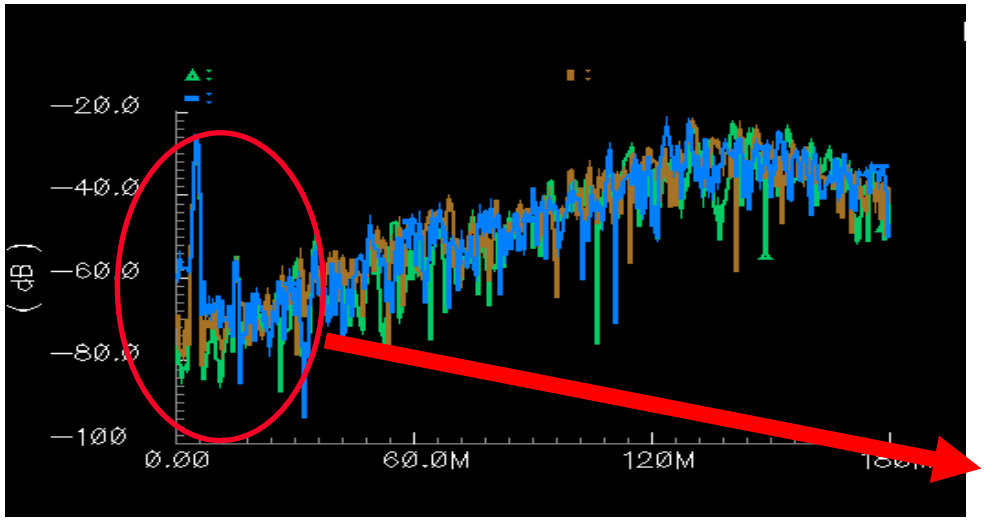


Differential Integrator

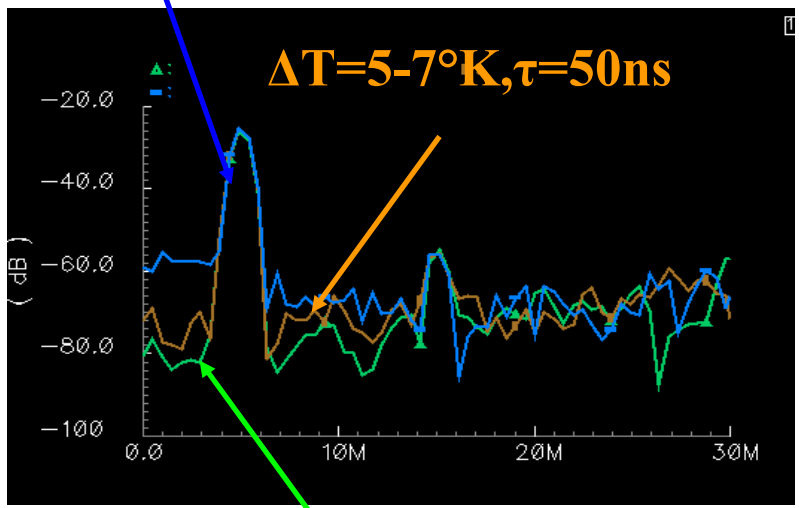


Latch

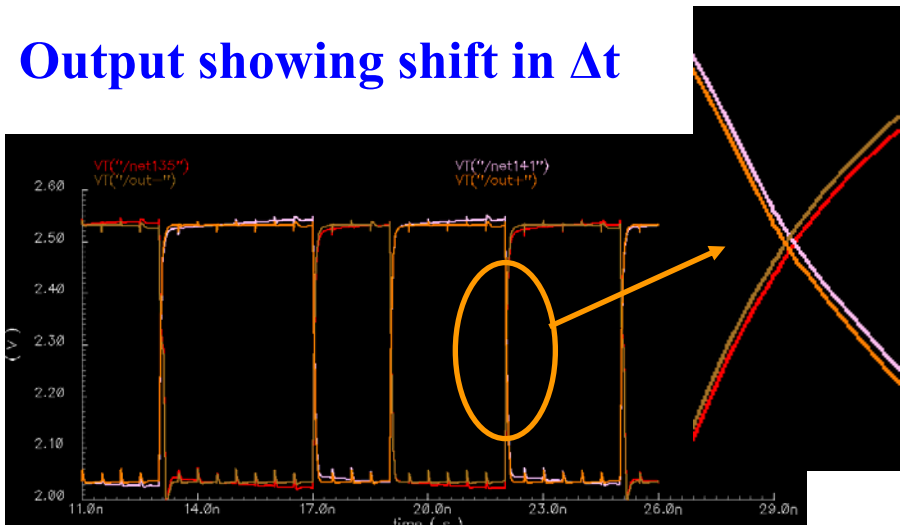
Transistor-level Simulation Results



ΔT=10-15°K,τ=5ns



Output showing shift in Δt

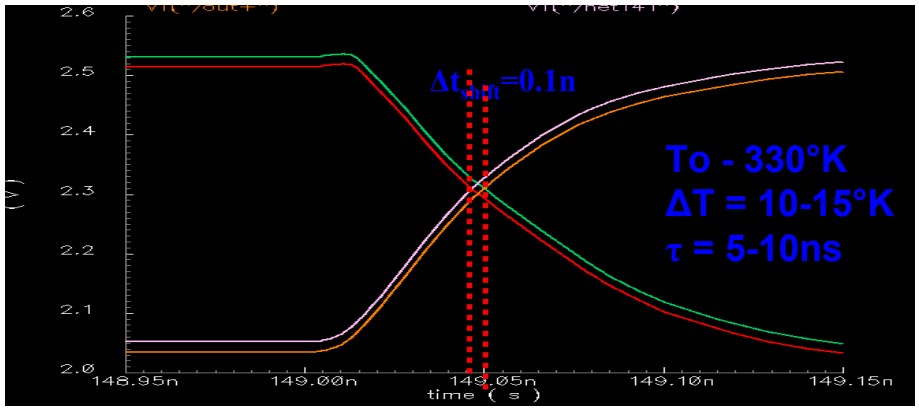


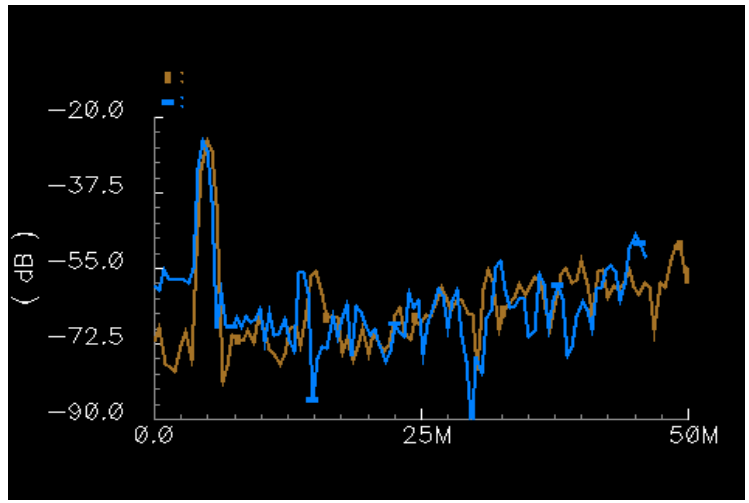
No Temperature Mismatch

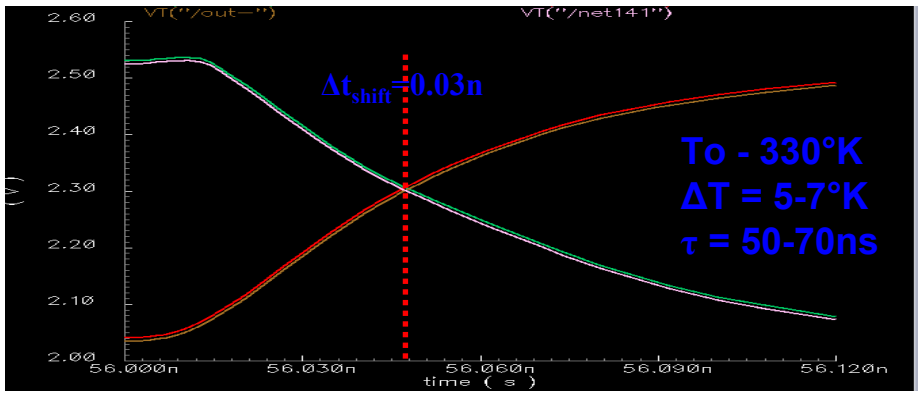
SNR Degradation and Switching Distortion

$$= \frac{\sqrt{\quad}}{\sigma}$$

OSR = Oversampling ratio
σ_T = Max Time shifts in seconds
f_{in} = Input frequency



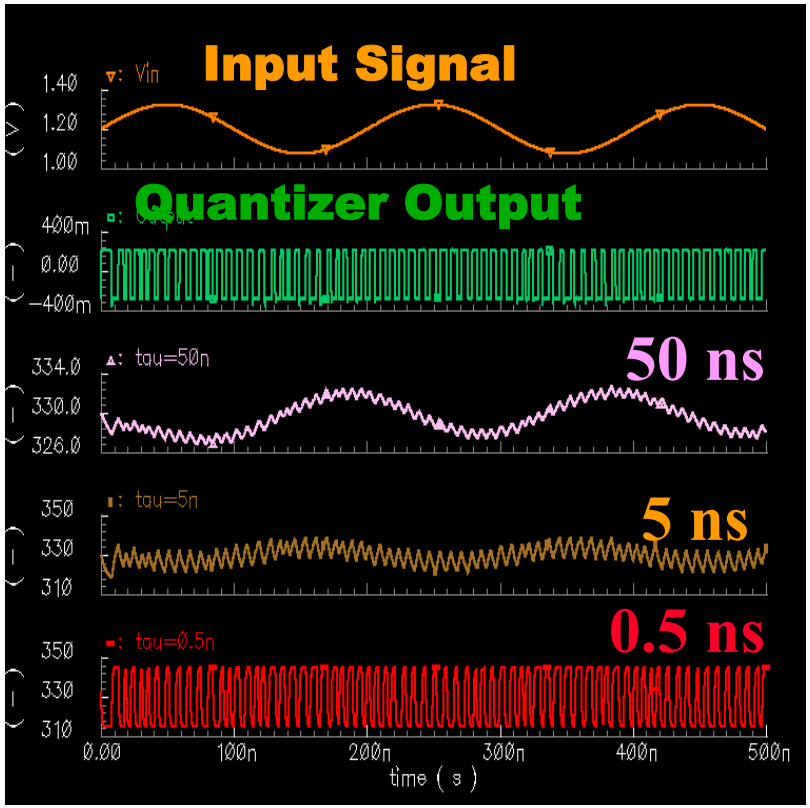


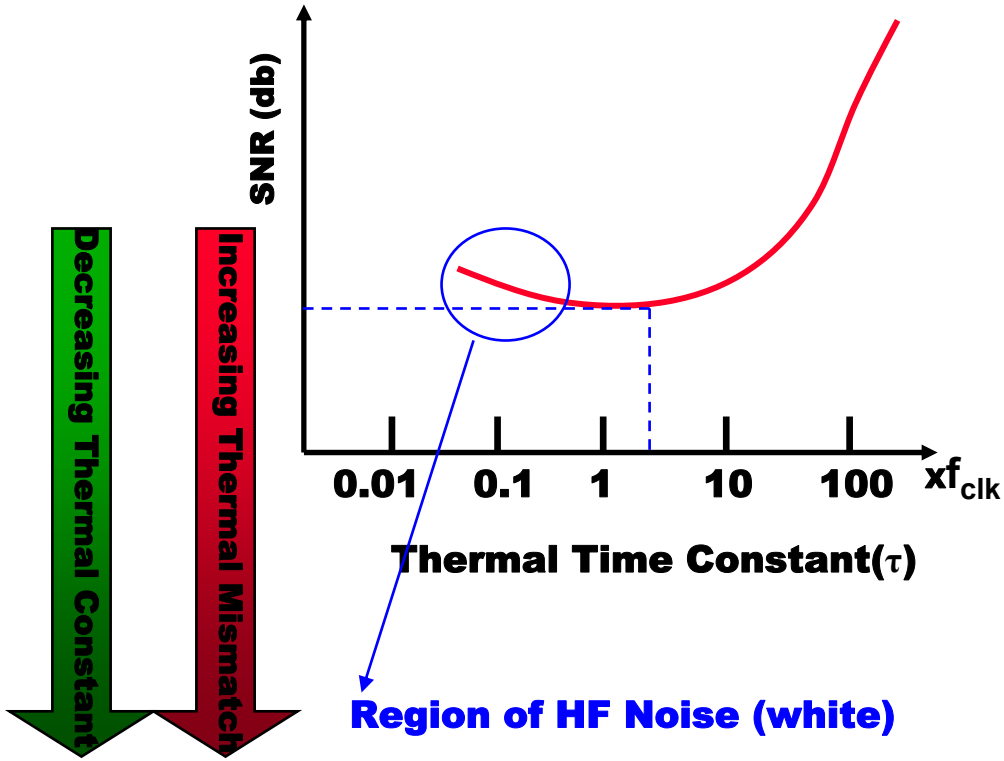


$$\mathrm{SNR}_{\tau=5ns} - \mathrm{SNR}_{\tau=50ns} = 20\log\frac{\sigma_{\tau=5ns}}{\sigma_{\tau=50ns}} \approx 10\mathrm{dB}$$

SNR degradation is dependent on Switching distortion

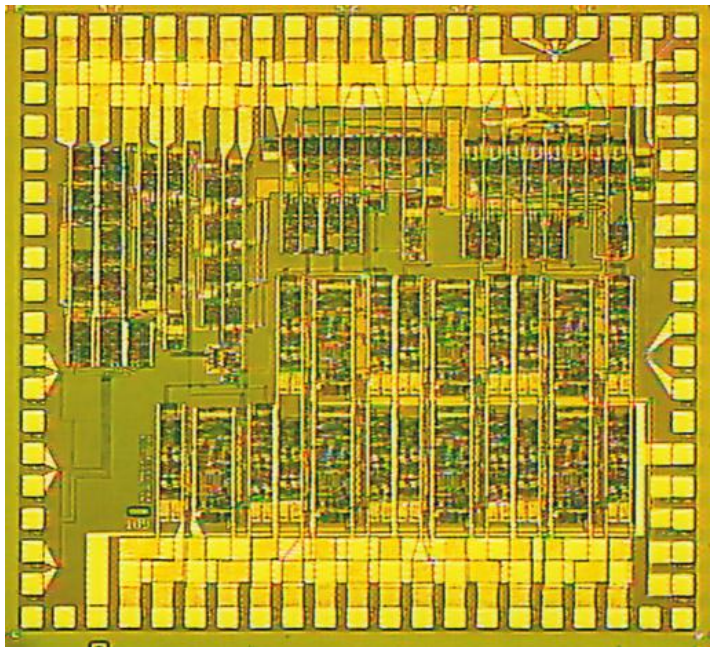
SNR and Thermal Time Constant





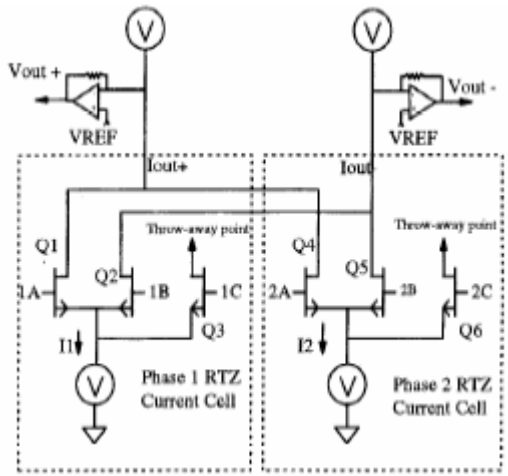
Decreasing Thermal Time Constant Results in Lower Input-Correlated Noise

Compensation Strategies to Mitigate DAC Noise



3-bit, mismatch-shaped ΔΣ modulated DAC generates tunable narrowband signal between 250 MHz and 750 MHz With 68dB SNR and 74 dB SFDR (T. Kaplan, et.al, ISSCC 2004)

- **With Bleeder Transistors for Uniform Heating (Adams et. al. ISSCC, 1996), (Cosand, patent, HRL)**



- **Pulse Shaped DAC architectures (B. Zhang et.al, 1996) (S. Luschas et.al, 2002)**

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Summary and Conclusion

- Controlling Thermal induced Intersymbol interference is critical to achieving high resolution ΔΣ Modulator
- Increasing thermal response time of current-mode differential DACs reduces ISI
- Decreasing Thermal Time Constant results in lower Input-Correlated Noise
- Transistor-level simulations using BiCMOS process validate Physics-based behavioral models