A General Method for Multi-Port Active Network Reduction and Realization

Pu Liu, Zhenyu Qi, Amalia Aviles, and Sheldon X.-D. Tan

Department of Electrical Engineering
University of California, Riverside, CA 92521, USA

ABSTRACT

This paper presents a novel compact modeling technique for linear(ized) active analog circuits. The new method is based on a recently proposed general *s*-domain hierarchical modeling and analysis method. In this work, based on the characteristics of analog circuits, we propose a constrained linear least square based method to optimize the order reduced admittance matrices with respect to both magnitude and phase responses up to the given frequency range. Theoretically we show that the hierarchical reduction does not change the reciprocity property of the linear circuit. For analog active circuits, which typically are non-reciprocal, so do the order-reduced circuit admittance matrices after hierarchical reduction. We propose a novel general multi-port, non-reciprocal network realization method. The resulting modeling algorithm can take in the SPICE netlists of active circuits and generate high-fidelity compact macro models of the active circuits with easily controlled model accuracy and complexity. The experimental results on two low-pass active filters demonstrate effectiveness of the proposed algorithm.

1. INTRODUCTION

Model order reduction for passive interconnect circuits has been intensively studied in the past due to increasing complexity of parasitic layouts of digital circuits. Many efficient algorithms have been proposed to reduce the interconnects modeled as RC/RCL/RLCK circuits such as Krylov subspace projection based methods [12, 3, 17, 7, 11] and local node reduction based methods [2, 15, 1, 14, 16, 18].

For linear or linearized active circuits like filters, opamps etc., which dominate many analog, mixed-signal and radio-frequency (RF) circuits, less studies have been done to reduce those active circuits and realize the reduced circuit matrices using compact models [5]. On the other hand, simulation of analog, mixed-signal and RF circuits is a very time-consuming process. For instance, RF circuit simulation is an extremely time-consuming process due to very long simulation time to accommodate both the fastest and the slowest tones in the input signals [10]. As more analog, RF components are manufactured on-chip using the latest digital VLSI technologies [8], parasitics which are associated with many digital circuits are also needed to be considered in the integrated analog, RF circuits. This leads to increasing sizes of analog, RF circuits and makes RF simulation a more challenging task. As a result, reduction and compact modeling of circuits with both passive and active circuits are important for fast mixed-signal and RF circuit design and verification.

Active circuits are different from passive circuits in several respects. First many active circuits are nonlinear in nature. But they often exhibit linearity when input signals are small so that the operational points do not change significantly. Such linearized circuits are good enough for predicting many useful characteristics of the analog and RF circuits such as gain, noise figures, bandwidth, noise margin for early stage verification. Second, active circuits may generate energy, which means they are not passive. Thus no passive reduction and passive enforcements are required. But the phase responses of many active circuits like opamps are important as they determine the stability of the circuits due to internal or external feedback loops [9]. But existing model order reduction approaches only match the magnitude (or real and imaginary) part of the circuit responses. Explicit matching of phase response is desired in analog circuit modeling in addition to the magnitude matching in frequency domain. Third, active circuits typically don't have the reciprocity property [1]. Mathematically a reciprocal network has a symmetric matrix, which has been exploited by many existing reduction approaches for RLCK circuits by iterative approaches. But this is not the case for general active circuits, which will make those methods less efficient. Also the reduction process should not change the reciprocity property of the circuit during the reduction process. But this is not the case for most of projection based reduction algorithms like PRIMA [12] except for the recent work [4]. Also how to realize general non-reciprocal (non-symmetric) order-reduced circuit matrices remains a less studied problem.

In this paper, we propose a general reduction and macro-modeling technique of the linear or linearized active circuits. Our new reduction process is based on the recent hierarchical multi-point reduction algorithm, which allows reduction and realization of both passive and active circuits up to very wide frequency ranges [13]. Our new contributions of this work are as follows: (1) Theoretically, we show that the hierarchical model order reduction [18] does not change the reciprocity property of the circuits. (2) Practically, we apply a constrained linear least square based optimization method to match both magnitude and phase responses of the admittance in the reduced matrix after the hierarchical reduction for modeling active circuits. (3) We propose a general multi-port network realization process to realize any multi-port non-symmetric circuit matrices for macromodeling of non-reciprocal active circuits based on relaxed one-port Foster's canonical form network synthesis technique. The resulting modeling algorithm can generate high-fidelity multi-port macromodels of any linear active networks with easily controlled model accuracy and complexity up to the given frequency range.

The paper is organized as follows. Section 2 reviews the hierarchical multi-point modeling technique and also shows theoretically that the hierarchical reduction does not change the reciprocal property of the circuit matrices. Section 3 presents the optimization process for matching both magnitude and phase responses of admittances in the reduced circuit matrix up to the given frequency range. In section 4, we describe the realization process of non-symmetrical admittance circuit matrices. The experimental results and conclusions are presented in section 5 and section 6, respectively.

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[1]A reciprocal network is one in which the power losses are the same between any two ports regardless of direction of propagation [20].

2. HIERARCHICAL MULTI-POINT MODEL ORDER REDUCTION

The general *s*-domain hierarchical model order reduction method[18] is a general model order reduction technique that can be applied to any linear networks (passive or active). Considering a subcircuit with some internal structures and terminals, the circuit's unknowns—the node-voltage variables and branch-current variables—can be partitioned into three disjoint groups x^I, x^B, and x^R, where the superscripts *I, B, R* stand for, respectively, *internal* variables, *boundary* variables and the *rest* of variables. Assume that modified nodal analysis (MNA) is used for circuit matrix formulation. With this, the system-equation set $MX = b$, can be rewritten in the following form (Schur decomposition):

$$\begin{bmatrix} M^{II} & M^{IB} & 0 \\ M^{BI} & M^{BB} & M^{BR} \\ 0 & M^{RB} & M^{RR} \end{bmatrix} \begin{bmatrix} x^I \\ x^B \\ x^R \end{bmatrix} = \begin{bmatrix} b^I \\ b^B \\ b^R \end{bmatrix}. \quad (1)$$

The matrix, M^{II}, is the *internal* matrix associated with internal variable vector x^I.

Hierarchical reduction is to eliminate all the variables in x^I, and to transform (1) into the following reduced set of equations :

$$\begin{bmatrix} M^{BB*} & M^{BR} \\ M^{RB} & M^{RR} \end{bmatrix} \begin{bmatrix} x^B \\ x^R \end{bmatrix} = \begin{bmatrix} b^{B*} \\ b^R \end{bmatrix}, \quad (2)$$

where $M^{BB*} = M^{BB} - M^{BI}(M^{II})^{-1}M^{IB}$ and $b^{B*} = b^B - M^{BI}(M^{II})^{-1}b^I$. Suppose that the number of internal variables is t, and the number of boundary variables is m. Assuming $det(M^{II}) \neq 0$, Then each matrix elements in the modified M^{BB} and b^B can be written in the following expanded forms:

$$a^{BB*}_{u,v} = \frac{det(A[1,...,m,u|1,...,m,v])}{det(A^{II})}, \quad (3)$$

where $u, v = 1,...,l$ and element in the RHS can be written in the following form:

$$b^{B*}_u = \frac{det(A[1,...,m,u|1,...,m] + b^I)}{det(A^{II})}, \quad (4)$$

where, $M[1,...,m,u|1,...,m,v]$ is the submatrix that consists of matrix M^{II}, which actually is $M[1,...,m|1,...,m]$, plus row u and column v of matrix A; $M[1,...,m,u|1,...,m] + b^I$ is the submatrix that consists of matrix M^{II} plus row u of matrix M and the right hand side column b^I.

Hierarchical node reduction algorithm is to compute the new admittances $a^{BB*}_{u,v}$ and new right-hand side element b^{B*}_u in terms of order-limited rational functions of *s* hierarchically.

However, like AWE methods, it suffers the numerical problems for computing high order terms due to polynomial divisions. The multi-point hierarchical method has been proposed to alleviate this problem [13], where multiple expansions along real or complex frequency axis are performed and poles obtained from different expansion poles are combined to get more accurate models over wide frequency ranges.

Given a reciprocal network and its symmetric circuit admittance matrix, the reduced circuit matrix is still symmetric after hierarchical reduction. On the other hand, given non-symmetric circuit matrix of a non-reciprocal circuit, the reduced circuit matrix is still not symmetric. Therefore, we have the following result:

THEOREM 1. *The hierarchical reduction method process does not change the reciprocity property of a linear circuit.*

Proof Sketch: We first show that given a symmetric circuit matrix, the reduced circuit metric is also symmetric. This can found by using Eq.(3) again. We first study a circuit with circuit matrix M. The circuit has one subcircuit with circuit matrix M^{II}. Assume that original circuit matrix is symmetric (its subcircuit is also symmetric, i.e. both M and M^{II} are symmetric) due to reciprocity.

After reduction, the reduced circuit matrix becomes a $m \times m$ matrix where each matrix element at row u and column v is shown in Eq.(3). We then look at the element at row v and column u, which is

$$a^{BB*}_{v,u} \frac{\det(M[1,...,m,v|1,...,m,u])}{\det(M^{II})}, \quad (5)$$

Notice that matrix M is symmetric, so the row u in Eq.(3) are column u in Eq.(5) are same. This is true for column v in Eq.(3) and row v in Eq.(5). As a result we have

$$M[1,...,m,v|1,...,m,u] = M[1,...,m,u|1,...,m,v]^T \quad (6)$$

$$det(M[1,...,m,v|1,...,m,u]) = det(M[1,...,m,u|1,...,m,v]^T) \quad (7)$$

Hence, $a^{BB*}_{u,v} = a^{BB*}_{v,u}$ and reciprocity is preserved in the reduced circuit matrix when one subcircuit is reduced. In the hierarchical reduction, we reduce one subcircuit at a time and the reduced circuit matrix is still symmetric after reduction. So the reduced circuit matrix after all the subcircuits are reduced is still symmetric.

For non-symmetric circuit M, the row u in Eq.(3) are column u in Eq.(5) are not same in general. This is true for column v in Eq.(3) and row v in Eq.(5). Hence, $a^{BB*}_{u,v}$ is no longer the same as $a^{BB*}_{v,u}$. The resulting reduced circuit matrix is not symmetric also. This completes the proof of this theory.

3. OPTIMIZATION CONSIDERING MAGNITUDE AND PHASE RESPONSES

3.1 Motivation for considering both phase and magnitude responses

Existing model order reduction tools typically match the admittance responses in terms of magnitudes (or real and imaginary parts). But for active circuits, phase responses are also important as they are related to the stability of the active circuits as many active circuits have internal feedbacks. Fig.1 shows the optimized admittance response of $Y_{12}(s)$ of reduced two-port admittance matrix of $\mu A725$ opamp circuit without considering matching phases. As can be seen, the phase part discrepancy are quite large at low frequency range even the magnitudes are matched perfectly. This reduced 2×2 circuit model will give incorrect phase responses, which may result in unstable or oscillating response of the whole system in time domain under some input stimulus in given frequency range. As a result, we have to explicitly match the phase response during the optimization process shown below.

3.2 Constrainted Least Square Based Optimization

After the multi-point hierarchical model reduction, a *n*-port order reduced admittance matrix of the original circuit is generated as shown in Eq.(8),

$$\hat{\mathbf{Y}}(s) = \begin{bmatrix} \hat{Y}_{1,1}(s) & \cdots & \hat{Y}_{1,n}(s) \\ \vdots & \ddots & \vdots \\ \hat{Y}_{n,1}(s) & \cdots & \hat{Y}_{n,n}(s) \end{bmatrix} \quad (8)$$

where, each of the rational admittance $\hat{Y}_{ij}$ can be represented in the partial fraction form as shown in Eq.(10). The hierarchical multi-point reduction process typically finds all the dominant poles in the given frequency ranges for each admittance, but their residues may not be accurate due to multi-point expansions. As a result, we need

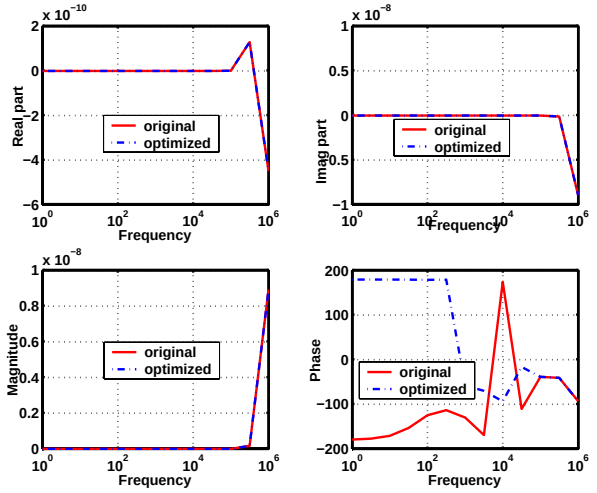

Figure 1: The admittance Y_{21} response of $\mu A725$ Opamp without considering phase

to adjust the residues so that admittance responses match well with the exact ones in both magnitude and phase. This can be done by the constrained least square optimization process.

Assume that we have obtained the admittance matrix of a order reduced system $\hat{\mathbf{Y}}(s)$ with a set of T frequency sampling points. Let $\tilde{Y}_{p,q}(s_k)$ be the exact values of the admittance at the entry (p,q) at the kth frequency point, which can be obtained by the exact hierarchical symbolic analysis [19].

Let's first consider the magnitude only. Then the optimization problem is to determine the residues of poles such that the following least square cost function is minimized:

$$min(\sum_{k=1}^{T} \|\hat{Y}_{p,q}(s_k) - \tilde{Y}_{p,q}(s_k)\|_2^2) \tag{9}$$

In order to format the optimization problem, we need to rewrite each rational function at the entry (p,q) of the admittance matrix in the following partial fraction form:

$$\hat{Y}(s) = s\hat{Y}_\infty + \hat{Y}_0 + \sum_{m=1}^{M} \frac{rr_m}{s - pr_m} + \sum_{n=1}^{N} (\frac{rc_n}{s - pc_n} + \frac{rc_n^*}{s - pc_n^*}) \tag{10}$$

where we have N-pair conjugate poles pc_n and M real poles pr_m.

For a given frequency point s_k, we define

$$A_k = [\ a_1^r(s_k) \quad \cdots \quad a_M^r(s_k) \quad a_1^c(s_k) \quad \cdots \quad a_{2N}^c(s_k) \quad 1 \quad s_k\ ] \tag{11}$$

and

$$x = [\ x_1^r \quad \cdots \quad x_M^r \quad x_1^c \quad \cdots \quad x_{2N}^c \quad Y_0 \quad Y_\infty\ ]^T \tag{12}$$

For each pole lying on real axis of s plane, we have

$$a_m^r(s_k) = \frac{1}{s_k - pr_m} \tag{13}$$

and x_m^r is the residue corresponding pole pr_m. In the case of complex poles, we have

$$a_n^c = \frac{1}{s_k - pc_n} + \frac{1}{s_k - pc_n^*}, a_{n+1}^c = \frac{j}{s_k - pc_n} - \frac{j}{s_k - pc_n^*} \tag{14}$$

and consequently x_n^c and x_{n+1}^c are the real parts and imaginary parts of the conjugate residues of the complex poles respectively.

For T frequency points, we define

$$A_{lin} = \begin{bmatrix} re(A) \\ im(A) \end{bmatrix}, Y_{lin} = \begin{bmatrix} re(\tilde{Y}) \\ im(\tilde{Y}) \end{bmatrix} \tag{15}$$

We then can rewrite Eq.(9) as

$$min(\|A_{lin}x - Y_{lin}\|_2^2) \tag{16}$$

In this way, all the variables (the real and imaginary parts of residues) are real variables and the optimization is done in the real number domain.

Now we consider the phase constraints. Phase essentially is the ratio of the real and imaginary parts of complex number. Normally it will be automatically matched if magnitude is matched when both real and imaginary parts are not small. But this is not the case when both of them are very small numbers. There are two aspects of the ratio: one is the sign of the ratio and the other is the value of the ratio. We first consider the sign constraint. Let's define

$$Y_D = diag(Y_{lin}) \tag{17}$$

where $diag(Y_{lin})$ means generating a diagonal matrix from a vector Y_{lin} and

$$D_{lin} = Y_D A_{lin} \tag{18}$$

then the phase sign constraint becomes

$$D_{lin}x \geq 0 \tag{19}$$

Then we consider the ratio value constrain, which requires that the ratio between real and imaginary parts of the optimized one is the same as the exact one. Let's define

$$Y_I = diag\left(\begin{bmatrix} im(\tilde{Y}) \\ re(\tilde{Y}) \end{bmatrix}\right) \tag{20}$$

and

$$C_{lin} = I_{lin} Y_I A_{lin} \tag{21}$$

where

$$I_{lin} = \begin{bmatrix} 1 & \cdots & 0 & -1 & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 1 & 0 & \cdots & -1 \end{bmatrix} \tag{22}$$

then the phase value constraint becomes

$$C_{lin}x = 0 \tag{23}$$

Finally, we have the following constrained linear least square optimization problem:

$$min(\|A_{lin}x - Y_{lin}\|_2^2) \quad \text{subject to} \quad \begin{matrix} D_{lin}x \geq 0 \\ C_{lin}x = 0 \end{matrix} \tag{24}$$

The resulting problem is solved by MATLAB's Least Square tool package in our work.

4. MULTI-PORT NON-RECIPROCAL CIRCUIT REALIZATION

In this section, we show how to realize a general non-symmetric (non-reciprocal) $n \times n$ admittance matrix into a macro-model in the form of RLC and controlled elements, which can be accepted by general SPICE like simulators in both frequency and time domain simulation.

4.1 Relaxed one-port realization

We start with one-port network realization. For a one-port model with driving-point admittance function, we use a generalized Foster's canonical form [20] to directly synthesize the admittance function.

After optimization, the new element $Y(s)$ in the reduced admittance matrix can be rewritten in Eq.(25).

$$Y(s) = sY_\infty + Y_0 + \sum_{m=1}^{M} \frac{x_m^r}{s - pr_m} + \sum_{n=1}^{N} \left(\frac{x_n^c + x_{n+1}^c j}{s - pc_n} + \frac{x_n^c - x_{n+1}^c j}{s - pc_n^*}\right) \tag{25}$$

The admittance function in Foster's canonical-form can be then

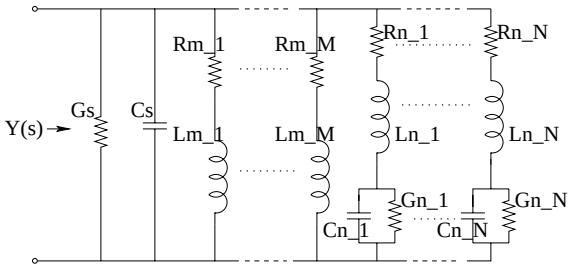

Figure 2: One-port Foster admittance realization.

synthesized by an equivalent circuit shown in Fig. 2 with the following equations to determine values of R, L, C, G elements:

$$\begin{aligned}
&G_s = Y_0, \qquad C_s = Y_\infty;\\
&Rm_m = \frac{1}{x_m^r}, \qquad Lm_m = -\frac{pr_m}{x_m^r};\\
&Ln_n = \frac{1}{2x_n^c}, \qquad Ln_nCn_n|pc_n|^2 = Rn_nGn_n + 1,\\
&\frac{Gn_n}{Cn_n} = -\frac{x_n^c re(pc_n) + x_{n+1}^c im(pc_n)}{x_n^c},\\
&\frac{Rn_n}{Ln_n} = \frac{x_n^c re(pc_n) + x_{n+1}^c im(pc_n)}{x_n^c} - 2re\{pc_n\}.
\end{aligned} \tag{26}$$

In our approach, we *relax* the requirement that all the RLC elements are positive as we do not need to physically realize those circuits. Instead, we allow negative resisters, inductors, and capacitors. As a result, the realization process can be done in straightforward way without any approximation, i.e. the realized circuit and admittance is one-to-one mapping and reversible.

4.2 Multi-port non-reciprocal realization

To realize a general $n \times n$ non-reciprocal admittance matrix, we propose a general complete-graph structure (in case of full admittance matrix) to realize the admittance matrix based on the one-port realization. In the following, we first illustrate how a 2-port network is realized and then we extend this concept for general n-port network realization.

Given a 2×2 non-symmetric admittance matrix as shown as Eq.27,

$$Y_{2\times 2}(s) = \begin{bmatrix} y_{11}(s) & y_{12}(s) \\ y_{21}(s) & y_{22}(s) \end{bmatrix} \tag{27}$$

where $y_{12}(s) \neq y_{21}(s)$, the admittance matrix can be realized ex-

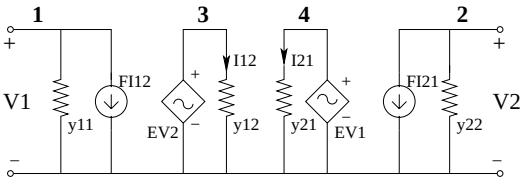

Figure 3: A general two-port nonreciprocal active realization.

actly by using the circuit template shown in Fig. 3, where each branch admittance will be realized by the one-port Foster's expansion method shown in Fig. 2.

Notice that the non-symmetric admittance is realized via two voltage controlled voltage sources (VCVS) EV_1 and EV_2, and two current controlled current sources (CCCS) FI_{12} and FI_{21}. Both VCVS and CCCS have the unit transfer gain. For instance, to realize $y_{12}(s)$, which represents the transconductor that leads to the current injected into node 1 due to voltage at node 2, the VCVS EV_2 first transforms the voltage at node 2 (V_2) into the node 3 ($V_2 = V_3$). Then V_3 drives the admittance y_{12} to generate the current $I12$, which then drives a CCCS FI_{12} to inject the same amount of current into node 1. Realization of $y_{21}(s)$ can be explained in the similar way.

For general $n \times n$ non-symmetric admittance matrix, we can realize each pair of ports using the aforementioned two port realization method until all the pair of ports are realized. The resulting circuits will have a complete graph structure (in case of full admittance matrix). But the non-symmetric property will be preserved during the realization process.

5. EXPERIMENTAL RESULTS

The proposed method has been implemented using C++ and MATLAB. The CPU times are collected on a Linux workstation with 3.0GHz P-IV CPU and 512M memory. We present the results on three examples.

The first example is a folded cascode CMOS OPAMP [6]. Its small-signal model contains 122 resistors, capacitors, and voltage control current source. We perform the multi-point hierarchical model order reduction up to 2MHz, which extracts 4 dominant common poles for admittance matrix. We match the frequency up to 2MHz during the optimization. The synthesized circuit includes 40 RLC, 2 VCVS and 2 CCCS controlled devices, which represents a 63.93% reduction ratio (63.93% circuit elements has been suppressed) for this case.

The resulting waveforms in frequency domain and comparison with the original waveforms are shown in Fig. 4 for $Y_{12}(s)$. As you can see, the synthesized circuit matches the original circuit perfectly up to the 2MHz in all aspects of the frequency responses.

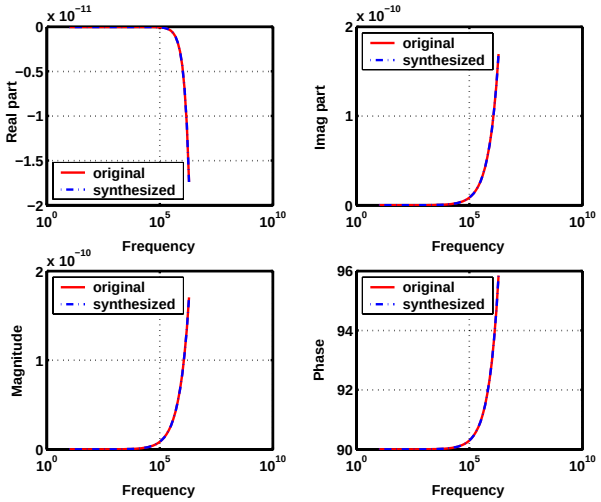

Figure 4: Frequency response of Y_{12} of opamp model

Using this CMOS opamp, we design two low-pass active filters. The first filter example is a tenth-order active Sallen-Key topology low-pass filter shown in Fig. 5. After the reduction and realization, there are 88 RLC elements, 2 VCVS and 2 CCCS dependent

sources in the synthesized circuit compared with 636 devices in the original circuit, which represents 85.53% reduction rate. The re-

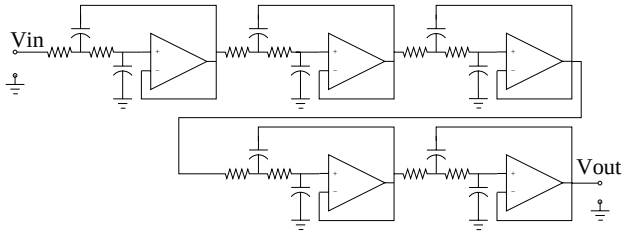

Figure 5: An active Sallen-Key topology low-pass filter

sulting waveforms in frequency domain and comparison with the original waveforms are shown in Fig. 6 for $Y_{21}(s)$. If the phase is not explicitly considered in the optimization process, the results are shown in Fig. 7 for $Y_{21}(s)$. It can be seen that the phase part has noticeable discrepancy compared with the exact response.

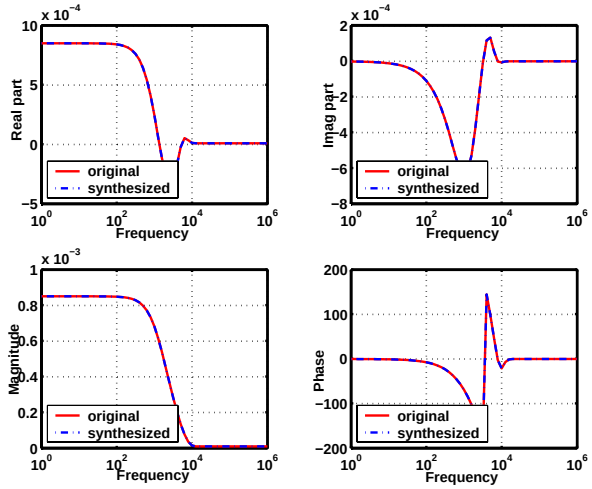

Figure 6: Frequency response of Y_{21} of the Sallen-Key topology low-pass filter

The filter's transfer function response is shown in Fig. 8. Fig 9 shows the simulation in time domain with different excitations. For the left figure, the input signal is a sinusoidal signal with 1KHz frequency. The outputs of the synthesized ones are almost the same of the original circuit and the synthesized circuit. For the right figure, the excite is also a sinusoidal function with 1MHz frequency. The outputs are still very close.

The second filter is shown as Fig. 10. This filter is a fifth-order elliptic filter using the FDNP (frequency-dependent negative resistor) technique. It contains 507 both passive and active elements. The matching frequency is up to 1MHz and we find 8 dominant poles in this range. There are 56 RLC elements, 2 VCVS and 2 CCCS dependent sources in the synthesized circuit, which gives 88.17% reduction rate.

The frequency response of the original circuit and synthesized circuit are shown in Fig. 11. From this figure, we notice that the realized circuit's response is almost the same as the original system form DC to 1MHz, but there are noticeable differences around 100MHz. This is expected as we only match the frequency up to 1MHz.

As a result the original circuit can be replaced by the synthesized model if the filter works in the frequency range from DC to 1MHz(at least) or 100MHz(at most). Over this frequency, the realized cir-

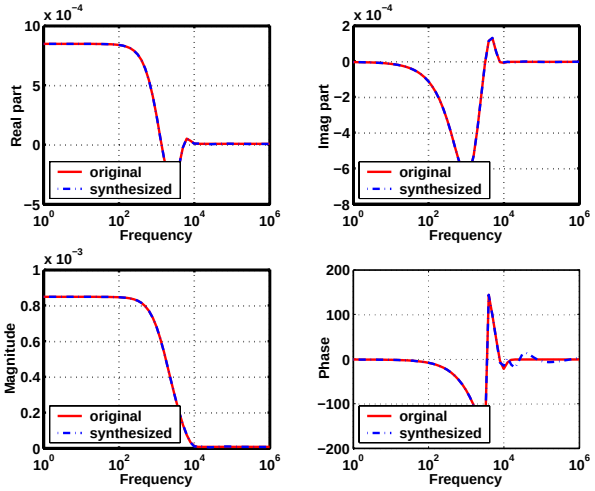

Figure 7: Frequency response of Y_{21} of the Sallen-Key topology low-pass filter without considering phase

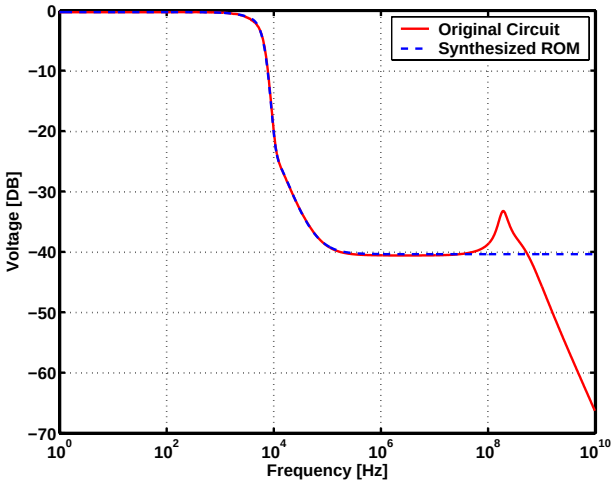

Figure 8: Frequency response of the transfer function of the Sallen-Key topology low-pass filter

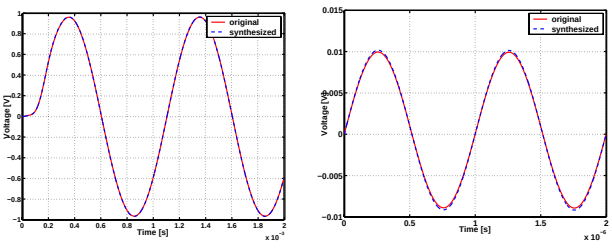

Figure 9: Transient response of the Sallen-Key topology low-pass filter with different excitations

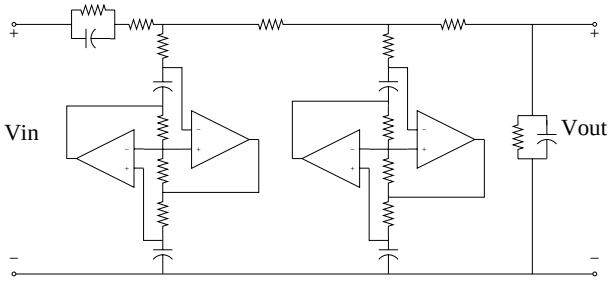

Figure 10: An active low-pass FDNR filter

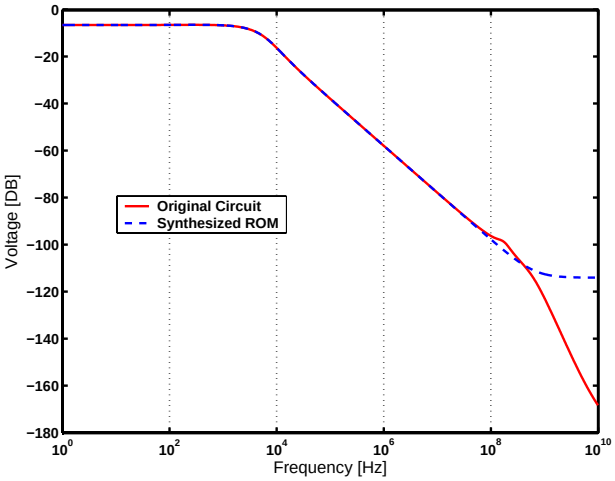

Figure 11: Frequency response of the transfer function of the low-pass FDNR filter

cuit will not match the original circuit well. The resulting transient waveforms are also shown in Fig. 12. We add the same signal to the input of the original filter and the synthesized circuit to view the output waveforms. The left figure is the result from a 1Khz sinusoidal excitation. The outputs are almost same between these two filters. The right figure shows the result from a 2MHz sinusoidal signal. The time domain simulation is still good at this frequency.

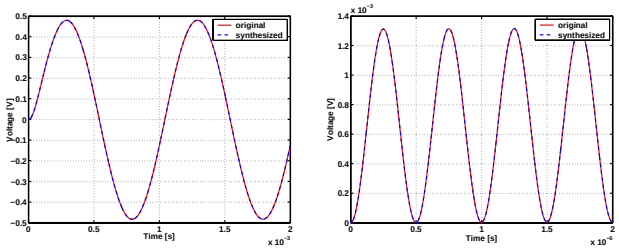

Figure 12: Transient response of the FDNR filter with different excitations

6. CONCLUSION AND FUTURE WORK

In this paper, we have proposed a novel active circuit modeling and realization technique. The proposed method combines the general multi-point *s*-domain hierarchical model order reduction with constrained linear least square based optimization technique to generate high-fidelity order-reduced multi-port admittance matrices in terms of both magnitude and phase responses of all admittance elements in the matrices. To realize the non-symmetric (non-reciprocal) admittance matrices, we have proposed a general multi-port network realization method based on relaxed one-port Foster's canonical form network synthesis technique. The resulting model order reduction flow takes the SPICE netlist of active circuits in and produces the SPICE netlist of macro models out, which makes the generated models very portable and flexible to be incorporated with other simulation tools. The experimental results have shown that the proposed method can generate very high accurate models for a number of active low-pass filters.

Unlike RLCK passive circuits, many analog, mixed-signal and radio-frequency (RF) circuits exhibit non-ideal behaviors such as harmonic distortion, noise phenomena, input/output offset voltage, saturation voltages etc. Our future work will add these non-ideal behaviors to the order-reduced model to capture the non-ideal behaviors of analog circuits.

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