Modeling and Simulation of Jitter in Phase-Locked Loops due to Substrate Noise

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ABSTRACT

This paper presents a methodology to simulate, at the system-level, substrate noise coupling to phase-locked loop (PLL) circuits. Macro models of the noise coupling to the PLL are proposed based on the concept of an impulse sensitivity function (*ISF*). A system-level simulation is implemented using Verilog-A and achieves significant advantage, namely 50 times speed enhancement over circuit-level simulation. Furthermore, a period histogram and its variations are considered as metrics to analyze the substrate noise effects on the PLL and the simulation method is verified by comparison with the measured data of period histogram variation patterns.

1. INTRODUCTION

Mixed signal, system-on-chip (SOC) implementations are of growing importance, compared to multi-chip solutions, due to their area and cost efficiencies. However, these systems also have drawbacks due to the noise coupling between digital and analog circuits through the substrate, which can be quite detrimental to sensitive analog circuits. For this substrate noise, different analysis and simulation methods have been proposed; particularly, for the noise injection into analog circuits, transistor-level or circuit-level simulation has traditionally been used [1] [2].

While circuit-level simulation provides accurate results, it requires extensive computation over extended time periods, especially when performing transient analysis of complex circuits such as those involving phase-locked loop (PLL) circuits. Very often, however, it is necessary to simulate the system in a coarse but fast way in order to gain initial design guidance. For example, speed is more critical than accuracy when simulations need to be repeated in order to identify key parameters in the design. In these cases, a behavioral-level modeling technique can be a powerful option to exploit trade-offs between simulation time and accuracy. In this context, behavioral simulation for PLLs has been studied from several perspectives, including noise considerations [3] [4] [5]. However, a macro model for the substrate noise coupling has not yet been seriously addressed.

This paper will first discuss methods for abstracting the macro model of the substrate noise coupling to PLLs. Then, the implementation of the combined behavioral models in Verilog-A will be explained. This includes the detailed analysis of timing jitter in the PLL output. Finally, the system-level simulation results will be verified by comparison with the measurement results.

2. BEHAVIORAL MODELS FOR PLL

In order to develop behavioral models for substrate noise coupling, the actual coupling mechanisms to the victim circuit need to be identified, first at transistor-level based on a physical representation. Then the identified mechanisms can be abstracted to the system-level, using numerical or empirical analysis. In the case of PLLs, the procedure can be simplified since most sub-blocks are digital and insensitive to substrate noise. By contrast, the VCO is quite vulnerable to substrate noise since its behavior is analog in nature. The substrate noise affects the VCO in two ways: the noise is coupled to the input of the VCO through the loop filter or to the internal oscillating nodes through the pull-up/down transistors in the VCO. In other words, the substrate noise is coupled to the loop filter or the VCO directly.

Although these two coupling mechanisms – loop filter and VCO - are equally significant in contributing to the phase noise of the VCO, there is a basic difference in the approach needed to obtain the respective behavioral models. The substrate noise coupling through the loop filter is linear and time invariant; thus, the transfer function of the loop filter is sufficient for determining the corresponding behavioral model. However, the coupling mechanism through the pull-up/down transistors of the VCO is time variant as well as spatially distributed, since the operating conditions of the transistors change with time. A different approach to model this time variant mechanism is discussed in the following sub-sections.

2.1. Coupling to MOS transistors

At the transistor-level, substrate noise interferes with the charging/discharging process at nodes by causing parasitic currents to flow due to changes in the device bias conditions. The parasitic current in the drain of transistors is attributed to two different mechanisms: the body effect and capacitive coupling of substrate noise to other nodes [6]. For the body effect, a small-signal linear parameter, g_{mb} characterizes the coupling mechanism; the parasitic current is proportional to the amplitude of substrate noise. In addition, fluctuations of the substrate potential results in a displacement current through drain/source junction capacitors of transistors; thus, the current through capacitive coupling is dependent upon the derivative of substrate noise over time. It should be noted while the body effect can be observed only when the transistor is in the active mode, capacitive coupling effects are prevalent even when the transistor is off or used as a

passive component – capacitor, switch, or resistor. In other words, the body effect is more dependent upon the operating environment of the transistor than is the capacitive coupling effect.

2.2. Coupling to VCO

The charge injected due to parasitic currents is only able to temporarily change the voltage at circuit nodes. Whether this temporary voltage variation should affect the basic function of the circuit is determined by the structure of the specific blocks. For oscillators, time dependency of node voltages is most critical; the parasitic current can cause jitter in the period of the oscillator or the phase noise [7]. Since phase deviation of oscillators is a key estimation for substrate noise coupling, a system-level transfer function between the phase deviation and substrate noise can be defined as a behavioral model. This noise coupling model can be derived either empirically or mathematically.

The empirical approach is based on circuit-level simulation of the oscillator, where a voltage impulse is applied to the bulk node of a specific transistor and the resulting phase shift is measured, and a (voltage) impulse sensitivity function (ISF_v) is extracted [8]. Meanwhile, the simulation verifies the linearity between the amplitude of the voltage impulse and the corresponding phase shift within a reasonable range of the amplitude – from -250mV to +250mV ; the typical amplitude of substrate noise is observed to be around 100mV [9], hence justifying the use of g_{mb}.

Figure 1 shows the data of the ISF_v for a ring oscillator, operating at 81MHz with 3 stages of inverters. This ISF_v, which is periodic with 12.345nsec, represents substrate noise coupling to the ring oscillator through the NMOS bulk node of the first stage in the inverter chain. Since the other two NMOS transistors and three PMOS transistors in the chain can also contribute to phase noise, the final phase noise results can be constructed using the superposition of respective sensitivity functions and substrate noise for each transistor.

The analysis of substrate noise coupling to the transistor can present a way to generalize the empirical approach with the voltage sensitivity function. As mentioned above, substrate noise causes a parasitic current; the current yields a phase shift. Thus, these two mechanisms can be represented with respective analytic functions. For the first mechanism, the

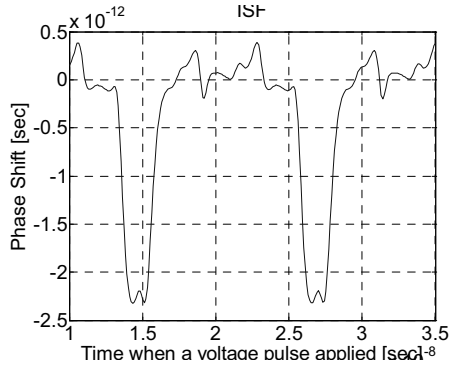

Figure 1. ISF_v of a ring-type oscillator.

parasitic current, $\Delta I(t)$, due to the substrate noise, $V_{sub}(t)$, can be described by:

$$\Delta I(t) = g_{mb}(t)V_{sub}(t) + C_j(t)\frac{dV_{sub}(t)}{dt}$$

where the first term corresponds to the transistor body effect and the second represents the capacitive coupling effect through the drain/source junction capacitors, $C_j(t)$. The second mechanism, representing the relationship between the parasitic current and the phase shift, is characterized as a (current) impulse sensitivity function, $ISF_i(t)$, which can be achieved by applying a current impulse to a node and measuring the phase shift [7]. Based upon the two mechanisms described above, the phase shift, $\Delta\Phi(t)$, can be represented by:

$$\Delta\Phi(t) = \int_0^t \Delta I(\tau) ISF_i(\tau) d\tau$$

$$= \int_0^t (g_{mb}(\tau)V_{sub}(\tau) + C_j(\tau)\frac{dV_{sub}(\tau)}{d\tau}) ISF_i(\tau) d\tau$$

If $V_{sub}(t)$ is a voltage impulse at t_0, $\delta(t-t_0)$, to extract the ISF_v data at t_0, the above equation can be simplified as $\Delta\Phi = g_{mb}(t_0) ISF_i(t_0)$, which indicates that the ISF_v is equal to the multiplication of g_{mb} and the ISF_i. Thus, the phase shift, $\Delta\Phi(t)$, can be reformulated as:

$$\Delta\Phi(t) = \int_0^t ISF_v(\tau)V_{sub}(\tau) + ISF_i(\tau)C_j(\tau)\frac{dV_{sub}(\tau)}{d\tau} d\tau \quad (1)$$

It should be noted that although the ISF_v is an intuitive function that represents the connection between substrate noise and phase shift, it can only represent the phase shift due to the body effect. To include the capacitive coupling effects of substrate noise, the ISF_i term is necessary so that (1) can be implemented for any arbitrary substrate noise. In general, extraction of g_{mb} and ISF_i is more efficient in terms of computation load compared to computing ISF_v and ISF_i, since the procedure of extracting sensitivity functions is computationally expensive.

2.3. Coupling through loop filter

As mentioned before, substrate noise coupling through the loop filter directly affects the control node of the VCO; thus, the effect of this coupling should be considered properly. Even so, unlike the case of the VCO, the coupling process is linear and time invariant and it is rather straightforward to abstract a coupling macro model at the system-level using simulation. This is mainly due to the fact that the transistors in the filter are used as passive devices; the overall transfer function is a passive coupling to first order. All passive devices in the loop filter for noise coupling can be approximated with lumped, equivalent circuit components. With this model simplification, the transfer function between the substrate and the control node can be formulated and implemented as a behavioral model of substrate noise coupling in the system-level simulations.

3. SYSTEM-LEVEL SIMULATION

Once the macro models are determined using the techniques discussed in the previous section, the substrate noise effects

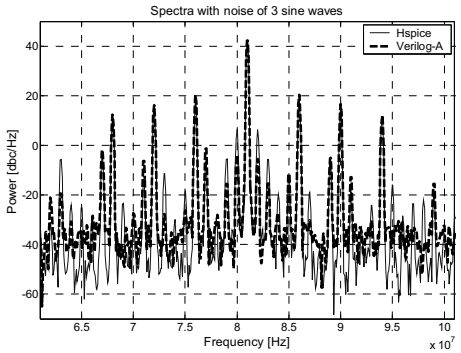

Figure 2. Spectra of simulations with 3 sine waves applied as substrate noise.

on the PLL system can be simulated at the system level. For the system-level languages, two different versions of Verilog-A have been applied: an interpreter-based version from Cadence; and a compiler-based version form Tiburon Design Automation (http://www.tiburon-tda.com).

For an idealized functional simulation of the PLL in Verilog-A, the behavioral models by Kundert [4] have been employed. In addition, the substrate noise coupling mechanisms are implemented by modeling equations and transfer functions as explained in the previous section; the examples of Verilog-A codes are provided on the web (http://www-tcad.stanford.edu/). To validate the advantages of system-level simulation over circuit-level simulation, the Verilog-A simulation results are compared to the results from Hspice simulation with an arbitrarily synthesized noise pattern. In both simulations, the substrate noise is applied to the bulk node of only one NMOS so that a single sensitivity function can be unambiguously examined. In general case, substrate noise is coupled to the bulk node of all the transistors in the VCO as common mode noise as well as in the loop filter. Hence, the entire coupling mechanism can be modeled as the superposition of all these effects.

Figure 2 depicts the spectra from Hspice and Verilog-A simulations when the combination of three sinusoidal signals (50mV 5MHz, 50mV 13MHz, 50mV 90MHz) is applied to the VCO in 81MHz PLL as substrate noise. In addition, the computation times for three simulator implementations are shown in Table 1, with 1,250,000 temporal points sampled in case of Verilog-A.

From Figure 2 and Table 1, it is verified that the system-level simulation in Verilog-A can deliver as good results as the circuit-level simulation, with a speed enhancement of about 50 times; spurs at the fundamental frequencies (5MHz, 9MHz, 13MHz apart from the center frequency) match in amplitude between Hspice and Verilog-A simulation results. The discrepancy of amplitude in minor spurs is attributed to the fact that the behavioral model for substrate noise coupling has limited accuracy in simulating the intermodulation of higher harmonics of substrate noise components. It should be noted that the two different Verilog-A simulations require similar computation time, in spite of the differences between the compiler and the interpreter used to load the Verilog-A code. The system-level simulations of the PLL are based on the top-level structure and include only a few Verilog-A models. Thus, the computation time to load the Verilog-A models is not a primary factor in determining the total simulation time. However, in general, as the number of Verilog-A models increases, the Verilog-A based on compiled implementations is expected to increase in relative efficiency.

Table 1. Simulation times.

Language	Hspice	Cadence Verilog-A	Tiburon Verilog-A
Simulation Time	14 hr. 53min.	19 min.	18min.

4. SUBSTRATE NOISE ANALYSIS

The effects of noise on the PLL can be estimated using two measures: the phase noise in frequency spectrum or the timing jitter in time-domain output. The phase noise provides intuitive comprehension in terms of how noise can affect the PLL performance. However, it involves the conversion from the timing error to the spurs in the frequency domain, which is often too complicated to analyze noise effects. Thus, without the necessity to consider this conversion, the timing error or jitter is a more suitable measure to investigate substrate noise effects. To observe the effects of substrate noise in terms of the jitter, the oscillating period of the steady state PLL output is sampled over a sufficient interval. When these samples are demonstrated in the format of a histogram, i.e., a period histogram, the distribution of the period deviation can be characterized with mode (i.e. the peak of the histogram) and variance (i.e. the cycle jitter). These two properties – the peak location and the cycle jitter – are quite comprehensive measures that estimate substrate noise effects on the PLL. In addition, it should be noted that when investigating jitter and other temporal properties, system-levels simulation are quite powerful. First, the simulation can adopt any arbitrary substrate noise patterns and allow the fundamental analysis of noise and jitter. Also, only the simulation at system-level can efficiently collect sufficient number of samples for the period histogram.

Strictly speaking, since the substrate noise is caused by the combination of all digital gate switching, it is deterministic. However, in practice, the logical structure, with a huge number of the gates, is so complicated that the overall combination of the gate switching signals can be assumed to consist of a periodic base and random components of noise. Thus, when analyzing substrate noise effects, two distinct cases can be considered separately – jitter occurrences caused by the random and the periodic noise contributions respectively. The detail analyses in both cases will be presented in the following sub-sections.

4.1. Period histogram with ideal sine wave noise

First, we analyze the basic situation of the period histogram in the presence of a given periodic substrate noise. Figure 3 shows the situation when a 100MHz sine wave is coupled to the ISF_v as substrate noise. The ISF_v consists of three sub-

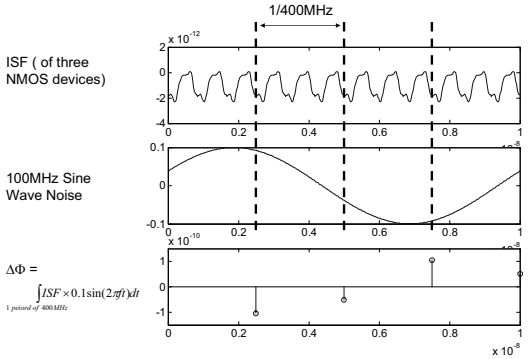

Figure 3. ISF_v of a 400MHz ring-type oscillator and 100MHz sine wave noise.

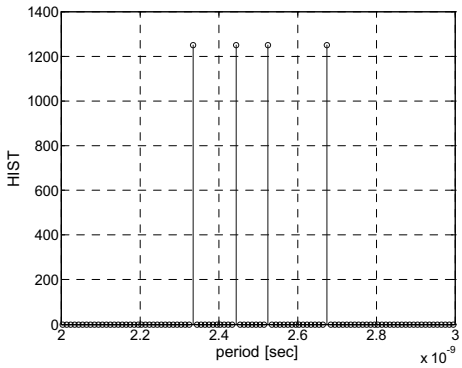

Figure 4. Period histogram with 100MHz sine wave noise.

periods since it is the superposition of three individual ISF_vs of each NMOS device in the three-stage ring-type oscillator. As explained in the previous sections, the phase shift is calculated as the integrated product of the sensitivity functions and the substrate noise. Furthermore, the indication of cycle jitter is just the phase shift evaluated at the end of every period of oscillation (marked as the dashed line in Figure 3). As shown in the bottom graph of Figure 3, four values of the phase shift are possible in this case; the period histogram of Figure 4 displays this fact clearly, showing that the histogram is symmetric and has four peaks. It should be noted that with phase difference between the ISF_v and the noise changing in Figure 3, the number of peaks can vary. Even so, the maximum number of peaks as a function of the sine wave noise (frequency, f_{noise}) is deterministic and can be calculated as:

$$\text{Maximum number of peaks} = \frac{L.C.M.(f_{noise}, f_{osc})}{f_{noise}} \quad (2)$$

where *L.C.M.* means the least common multiple and f_{osc} is the frequency of the VCO. This equation is derived based on the fact that the coupling relationship between noise and the sensitivity functions repeats with the period of $1/L.C.M.(f_{noise}, f_{osc})$. Several issues can be addressed, based on (2). First, the sine wave noise with different frequencies can yield the same number of peaks. For example, 300MHz sine wave noise and a 400MHz center frequency VCO also generate at most four peaks. Second, when f_{noise} is a multiple of f_{osc}, only one peak exists at the center without any jitter, thus showing no jitter even in the presence of substrate noise. Third, all split peaks are equal in amplitude, theoretically. However, the distribution of the peaks is dependant on other factors; thus the histogram with a large number of peaks can show a non-flat shape with some peaks merged to make other peaks higher.

In summary, a single tone sine wave noise yields peak-splitting in the period histogram and the maximum number of the peaks can be determined based on (2).

4.2. Period histogram with random substrate noise

When random noise is coupled through the substrate, the oscillating period of the PLL, *T*, also becomes a random variable and the histogram can be characterized with random properties such as the mean, *E[T]* and the variance, *Var[T]*. Furthermore, with a sufficient number of period samples, the histogram converges to the probability density function of the random period. First, the random variable, *T*, can be represented as:

$$T = T_{ideal} + \Delta T$$

where T_{ideal} is the ideal period of the PLL and ΔT is the period deviation (i.e. the phase sift accumulated over one period of the oscillation). From (1), with substrate noise, *n(t)*, ΔT can be described as:

$$\Delta T = \int_{1\ \text{period of oscillator}} ISF_i(t)(g_{mb}(t)n(t) + C_j(t)\frac{dn(t)}{dt})dt$$

If *n(t)* is a wide sense stationary and white Gaussian random process with zero mean and the variance, σ_n^2, the mean, *E[T]* and the variance, *Var[T]* of the period can be calculated as:

$$\begin{aligned} E[T] &= E[T_{ideal} + \Delta T] = T_{ideal} + E[\Delta T] \\ &= T_{ideal} \\ Var[T] &= Var[\Delta T] \\ &= E[\Delta T^2] - E[\Delta T]^2 \\ &= \sigma_n^2 \{ \int [ISF_v(t)]^2 dt + \int [\frac{d(C_j(t)ISF_i(t)}{dt}]^2 dt \} \end{aligned} \quad (3)$$

From (3), it becomes clear that the white Gaussian random noise introduces a jitter ($= \sqrt{Var[\Delta T]}$) without moving the peak of the histogram. Also, the jitter caused by random noise is proportional to the rms voltage of the noise.

4.3. Variation of period histogram with periodic noise

As discussed above, the shape of the period histogram depends upon the phase difference between substrate noise and the sensitivity function. Figure 5 illustrates the dependence of the histogram shapes on the phase difference when a 100MHz sine wave is applied as substrate noise. The phase of the y axis is based on a period of the sine wave

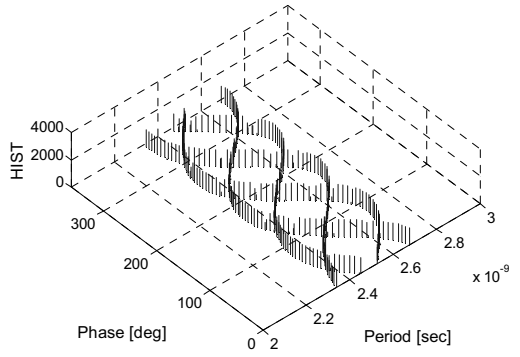

Figure 5. Histogram variation with 100MHz sine wave noise, with varying phase.

noise and, for example, 90° in the figure indicates a 2.5nsec time difference. The dependence of the histogram is depicted within the range of 360° since the shape will repeat periodically. As shown in the figure, four peaks are changing their locations in a sinusoidal manner, with 90° phase difference to to each other and, consequently, those peaks are merged to two at four phase points. In other words, a proper adjustment of the noise phase can decrease its effect in terms of the jitter. Also, the pattern of the histogram variation in the figure consists of four sub-periods. In general, with any periodic noise, the number of these sub-periods is the same value as the maximum number of peaks (as in (2)) since the traces of each peak are combined to make the sub-period pattern. This sub-period pattern becomes a good measure to compare the results between simulation and measurement; an example will be given in the next section.

Also, the shape of each trace can be determined by calculating the period deviation, ΔT, as a function of the phase difference, θ, between the noise and the sensitivity function. Using Fourier Series Expansion, any periodic noise pattern can be represented as:

$$\text{Periodic Noise } p(t) = a_0 + \sum_{k=1} (a_k \cos 2\pi k f_{\text{noise}} t + b_k \sin 2\pi k f_{\text{noise}} t)$$

where a_i and b_i are the Fourier series coefficients. Then, the period deviation at a phase of θ can be represented as follows:

$$\begin{aligned}\Delta T(\theta) &= \int_{\text{1 period of oscillator}} ISF_{\text{v}}(\text{substrate noise}) + C_{\text{j}} ISF_{\text{i}} \frac{d(\text{substrate noise})}{dt} dt \\ &= a_0 \gamma_0 \\ &\quad + \sum_{k=1} [a_k \sqrt{\gamma_{k,1}^2 + \gamma_{k,2}^2} \cos(k\theta + \varphi_k) + b_k \sqrt{\gamma_{k,1}^2 + \gamma_{k,2}^2} \sin(k\theta + \varphi_k)] \\ &\text{, where } \gamma_0 = \int ISF_{\text{v}}(t) dt, \\ &\quad \gamma_{k,1} = \int ISF_{\text{v}}(t) \sin 2\pi k f_{\text{noise}} t + C_{\text{j}}(t) ISF_{\text{i}}(t) 2\pi k f_{\text{noise}} \cos 2\pi k f_{\text{noise}} t dt \\ &\quad \gamma_{k,2} = \int ISF_{\text{v}}(t) \cos 2\pi k f_{\text{noise}} t - C_{\text{j}}(t) ISF_{\text{i}}(t) 2\pi k f_{\text{noise}} \sin 2\pi k f_{\text{noise}} t dt \\ &\quad \varphi_k = \tan^{-1}(\frac{\gamma_{k,1}}{\gamma_{k,2}})\end{aligned} \quad (4)$$

From (4), it is clear that a single trace with any periodic noise pattern is also periodic. Furthermore, its shape is dependent on the shape of the noise pattern; if the noise pattern is known, the shape of the trace can be determined mathematically or vice versa. Thus, the above equation can be applied in both estimating the substrate noise features and adjusting the system to reduce the effects of substrate noise.

4.4. Variation of the period histogram with the combination of periodic and white Gaussian random noises

As discussed above, in practical cases, the substrate noise consists of both random and periodic components. The analysis of this case is just the superposition of the above analyses. If the noise can be presented as:

$$\text{Noise Pattern} = n(t) + p(t)$$

where $n(t)$ is wide sense stationary, zero-mean, white Gaussian noise and $p(t)$ is periodic noise as introduced in the previous sub-sections. Then the mean, $E[T(\theta)]$ and the variance, $Var[T(\theta)]$ of the random period with given θ can be described as:

$$\begin{aligned}E[T(\theta)] &= E[T_{\text{ideal}} + \Delta T(\theta)] = T_{\text{ideal}} + E[\Delta T(\theta)] \\ &= T_{\text{ideal}} + a_0 \gamma_0 \\ &\quad + \sum_{k=1} [a_k \sqrt{\gamma_{k,1}^2 + \gamma_{k,2}^2} \cos(k\theta + \varphi_k) + b_k \sqrt{\gamma_{k,1}^2 + \gamma_{k,2}^2} \sin(k\theta + \varphi_k)] \\ &\quad \text{, where } \gamma_0, \gamma_{k,1}, \gamma_{k,2} \text{ and } \varphi_k \text{ are same as in (4)} \\ Var[T(\theta)] &= Var[\Delta T(\theta)] \\ &= \sigma_n^2 \{ \int [ISF_{\text{v}}(t)]^2 d\tau + \int [\frac{d(C_{\text{j}}(t) ISF_{\text{i}}(t)}{dt}]^2 dt \}\end{aligned} \quad (5)$$

The above equations indicate that while the location of the histogram peak is decided by the periodic noise, the spread of the respective trace is caused by the random noise component. The simulation results for this case will be presented in the next section.

5. COMPARISON WITH MEASUREMENT

As a test vehicle, a Digital Noise Emulator (DNE) and a 400MHz PLL (designed by Barcelona Design Automation Inc.) were fabricated on the same chip, using the TSMC 0.18μm generic logic technology in order to investigate how digital noise impacts the performance of analog/mixed signal blocks. Even though the PLL operates at 400MHz, the output comes through a divide-by-2 block and the ideal period, T_{ideal}, is 5nsec. The DNE takes an external clock input with arbitrary input frequency and generates three different noise patterns: a basic clock pattern with the same frequency as the input; a sub-harmonic clock pattern which is created using a divide-by-16 block; and a pseudo-random noise pattern, generated with logic gates. Thus, the first two patterns are periodic noise and the other is pseudo-random. The DNE can combine two patterns out of three and apply them to the chip through the 20pF coupling capacitors. The effects of substrate noise on the PLL output are measured in terms of the cycle jitter – the time variation of the PLL output period. A Wavecrest Signal Integrity Analyzer, SIA 3000, is used to collect sufficient samples of the output period data and build a period histogram to compare the results from system-level simulation.

Figure 6 shows the measurement results of the period histogram with phase, θ, which varies when 160MHz switching noise is applied through the substrate. In the

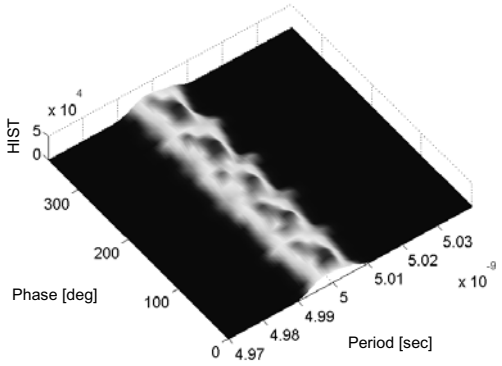

Figure 6. Measurement of period histogram with 160MHz switching noise, with varying phase.

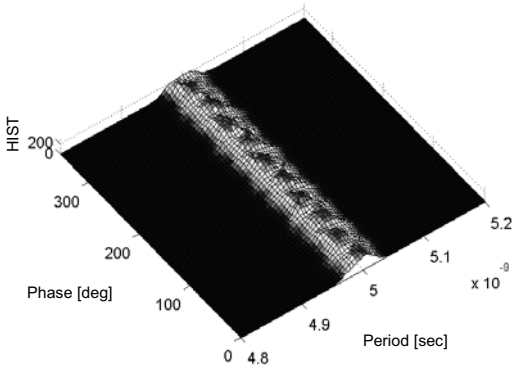

Figure 7. Verilog-A Simulation of period histogram with 160MHz switching noise plus Gaussian white random noise, with varying phase.

histogram variation, the dark spots indicate where the peaks are merged and thus the jitter decreases. The figure shows five repeating patterns and, as stated in the previous section, the number of these sub-periods is determined by (2). Since in the experimental system random noise is unavoidable, system-level simulation needs to include random noise for proper comparison with the measurement results. Figure 7 shows the results of the Verilog-A simulation when both 160MHz switching noise and 70mV-rms Gaussian random noise are applied. Figures 6 and 7 show good agreement between simulations and measurement in terms of the histogram variation pattern. Both figures show five sub-periods and the shape of details for each sub-period are nearly identical. Figure 8 shows the enlarged features of one sub-period from Figures 6 and 7; the relative shape of the dark spot can be observed in both figures. It can be pointed out that the comparison between measurement and simulation is performed in a qualitative way, comparing the histogram variation pattern. With respect to quantitative comparison, histogram spreads from Figures 6 and 7 show some discrepancies. These differences are mainly due to the random noise component applied to the system-level simulation, which is based on an arbitrary input, thus failing to model correctly random noise sources occurring in the test vehicle. However, the substrate noise in the test vehicle is purely periodic, thus the histogram variation due to random noise components is not the primary issue of interest. Hence, the qualitative approach can be justified in this case.

6. CONCLUSION

A system-level simulation methodology for PLLs is proposed, focusing on the behavioral model of substrate noise coupling effects. The simulation model is implemented in Verilog-A and shows good agreement with results of circuit-level simulations, achieving a substantial improvement in the computation speed. Using this methodology, analysis of the substrate noise effects on the period histogram is presented. Results show that: periodic noise splits the peak in the histogram, while random noise increases the deviation around the peak. In addition, it is proposed that phase adjustment between substrate noise and the sensitivity function can change the jitter performance. These analyses are also verified by the comparison with the measurement results using a 400MHz PLL implemented in a 0.18um TSMC process. This work was supported by DARPA under the NeoCAD program.

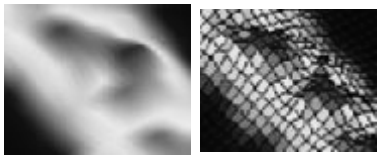

Figure 8. Enlargement of one sub-pattern from Figures 6 (Left) and 7 (Right).

7. REFERENCES

[1] A. Samavedam, A. Sadate, K. Mayaram, and T.S. Fiez, "A Scalable noise coupling model signal IC's," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, June 2000, pp. 895-904.

[2] M. Xu, D.K. Su, D.K. Shaeffer, T.H. Lee, and B.A. Wooley, "Measuring and modeling the effects of substrate noise on the LNA for a CMOS GPS receiver," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, Mar. 2001, pp. 473-485.

[3] A. Demir and A. Sangiovanni-Vincentelli, *Analysis and Simulation of Noise in Nonlinear Electronic Circuits and Systems*, Norwell, MA: Kluwer Academic Publishers, 1998.

[4] K. Kundert, "Modeling and Simulation of Jitter in Phase-Locked Loops," in *Analog Circuit Design*, Norwell, MA: Kluwer Academic Publishers, 1997, pp. 359-379.

[5] M.H. Perrott, "Fast and accurate behavioral simulation of fractional-n frequency synthesizers and other PLL/DLL circuits," in *Proc. of the 39th Design Automation Conf. (DAC)*, Anaheim, Calif., June 2002, pp. 498-503.

[6] E. Charbon et al, *Substrate Noise Analysis and Optimization for IC Design*, Norwell, MA: Kluwer Academic Publishers, 2001.

[7] A. Hajimiri and T.H. Lee, *The Design of Low Noise Oscillators*, Norwell, MA: Kluwer Academic Publishers, 1999.

[8] J.W. Kim, M.H. Perrott, and R.W. Dutton, "Behavioral Simulation Techniques for Substrate Noise Analysis in PLL Circuits," in *Proc. of the 11th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI)*, Hiroshima, Japan, Apr. 2003, pp. 331-337.

[9] L. M. Franca-Neto et al., "Enabling high-performance mixed-signal system on a chip (SoC) in high performance logic CMOS technology," in *IEEE Symp. on VLSI Circuits Digest of Technical Papers*, Honolulu, Hawaii, June 2002, pp. 164-167.