Accurate Behavioral Modeling Approach for PLL Designs with Supply Noise Effects

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Abstract

Using behavioral models to perform system simulation at behavioral level is currently a popular solution to verify mixed-signal systems. However, most of existing approaches only deal with ideal environments or make unrealistic assumptions, which cannot accurately evaluate the performance under supply voltage variation. In this paper, an efficient modeling approach with the effects of supply voltage variation is presented for PLL circuits to build accurate behavioral models in a short time using bottom-up extraction. Only three post-layout simulations are enough to generate accurate behavioral models under different supply voltages. The experimental results have shown that this approach can really have accurate responses under different supply voltages without time-consuming correlation analysis.

1. Introduction

In recent years, analog mixed-signal designs are very popular in ASIC applications. How to integrate digital and analog designs correctly becomes a serious problem. One of the popular ways to solve above issues is building the behavioral models for both digital and analog circuits and performing system simulation at behavioral level. Using those behavioral models, we can finish whole chip simulation in a very short time such that we can verify the integrated system earlier before down to layout level and reduce the design iterations.

In the literature, researches on building behavioral models of analog circuits are very popular [1, 2, 3]. According to the specifications, designers can use Simulink/Matlab or analog HDL to describe the mathematic formulas of analog circuits and simulate the possible results before implementation. Typically, such kind of top-down modeling approach is helpful for circuit designers to estimate the final results much faster when they are building their new designs.

In current SOC era, design reuse or IP-based design methodology is a popular solution to handle complex system. Such kind of verified blocks, especially for analog IPs, often appear as layout form or post-layout netlists, which is hard to understand without designers' help. In addition, some detailed circuit properties, such as timing information and parasitic effects, are hard to be modeled in the top-down approach due to the lack of layout information. Therefore, for IP-based SOC designs, bottom-up extraction approaches [4, 5] that build the behavioral models from post-layout simulation results may be the better way to obtain more accurate models for existing designs.

In our previous work [5], an efficient approach is presented to generate the behavioral models of Phase-Locked Loop (PLL) designs more quickly. The main idea is to use a special "characterization mode" to get required circuit parameters. In the characterization mode, only one input pattern is enough to get circuit properties with parasitic effects and intrinsic noises. No time-consuming correlation analysis is required to build this accurate model. As shown in the experimental results, the behavioral models built by this approach can have accurate results, especially on those non-ideal effects such as output jitters.

In SoC designs, the large portion of digital circuits may require large current to drive. This large current may incur many problems, such as the well-known IR-drop problem, that change the value of supply voltage. This kind of voltage fluctuation may have large impacts on the performance and reliability of designs, especially for analog circuits. Therefore, after the mixed-signal designs are integrated, supply voltage variation must be considered to evaluate the system performance accurately. However, those bottom-up approaches only deal with ideal environments without any variation. In order to have more realistic simulation results, we do need another approach to model the performance changes under non-ideal environments.

Actually, without detailed low-level simulation of the whole design, the possible variation on supply voltage is hard to be predicted. If we are going to estimate the responses under such voltage fluctuation at behavioral level, two primary approaches are often used. One is making an assumption that supply voltage variation is a random distribution and adding a Gaussian or Uniform variation generator into the behavioral models [6]. This is a simpler way to have some responses for observation. However, they may not the real cases while integrated into the system because the drawn current of the digital part may not fit the

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Gaussian distribution very well. Therefore, another approach takes the real supply voltage value as another input of the behavioral model and computes the real responses at this supply voltage immediately [7]. However, building such kind of behavioral models often requires statistical analysis, such as Monte Carlo (MC) analysis [8], to fit a curve of real responses under different supply voltages. Since a lot of simulation results are required in the statistical analysis, the construction time of such behavioral models will become unacceptable if post-layout simulation is used to obtain accurate results.

In this paper, an efficient modeling approach with the effects of supply voltage variation is presented for PLL designs to build accurate behavioral models in a short time using bottom-up extraction. Because all the parameters in the behavioral models proposed in our previous work [5] are obtained from voltage-domain measurement, their changes under supply voltage variation are almost proportional to the value changes of supply voltages in our observation. Therefore, using our modeling approach, we only have to run three post-layout simulations to obtain three behavioral models when the supply voltage has no change, positive change, and negative change. Then, given any supply voltage value, we can determine the parameter values of the behavioral model using interpolation or extrapolation from the parameter values of the three models. And the real responses under this situation can be obtained quickly by simulating the generated behavioral model as shown in Figure 1. According to the experimental results presented in Section 4, this approach can really have accurate responses under different supply voltages without tedious post-layout simulations.

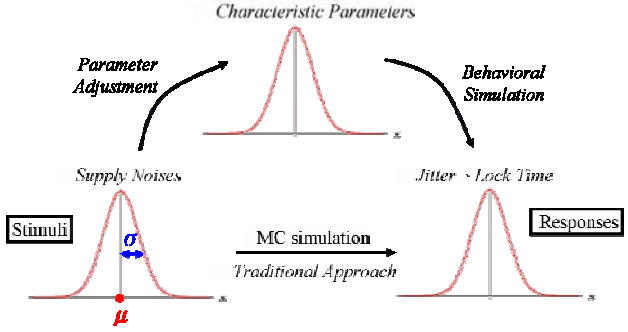


Figure 1. Our Ideas

2. Bottom-Up Extraction Approach for PLL

In this section, we will briefly introduce the bottom-up extraction flow proposed in our previous work [5] to generate an accurate PLL behavioral model. Actually, in the characterization process, the design under extraction does not have to operate in the same manner as in real system. If we can make the design operate in a special mode such that the required parameters can be obtained faster, which is called the "characterization mode", it can save much simulation time for building the behavior model.

For PLL designs, the proposed characterization mode is to break the PLL loop without separating it into independent blocks as shown in Figure 2. The broken connection is also very helpful for us to send special patterns to trigger the PLL into different situations. Therefore, we only need one input pattern to trigger the design and extract all the critical characteristic parameters. In the following subsections, the special input pattern used to trigger the PLL is presented. The relative output responses, the extracted characteristic parameters, and their meanings to our models will also be explained in detail.

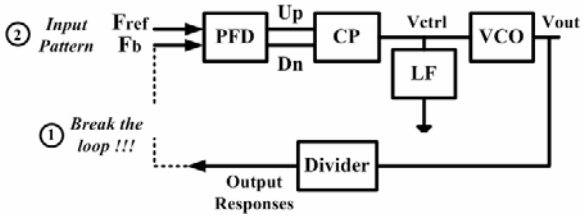


Figure 2. Characterization Mode of PLL

Please note that no exact current values and device sizes are required in the following measurement process. Since voltage-domain behavioral models are used, all parameters can be measured from the simulation results in the special characterization mode. Moreover, because we do not separate the netlist into sub-blocks in the simulation, tedious layout tracing step can be avoided and the interactions between blocks can be automatically considered. We believe that this would be a more suitable approach for existing IPs and flattened netlists.

2.1 Modeling Process

The proposed special extracting pattern is illustrated in Figure 3. The positive edge of F_{ref} will create positive phase error such that the source current of CP can charge V_{ctrl} in stage 1. If we give enough time, we can charge V_{ctrl} until voltage high to observe the entire response. Almost all characteristic parameters can be extracted in stage 1. The other positive edge of F_b will let the PFD operate in the reset state (stage 2). The reset time of PFD and the current mismatch can be observed from the output response. In the following subsections, we will explain how to get the parameters of each block in these two stages.

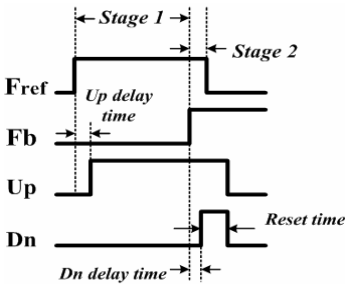


Figure 3. Input Pattern and PFD Response

2.1.1 PFD & Divider

Figure 3 also shows the output responses of PFD (Up and Dn). The parameters of delay time, reset time and output slew-rate can be easily extracted from the output waveforms. Those delay parameters are the primary sources of the non-ideal effects of PFD, such as dead zone. Similarly, the timing information of the frequency divider block can also be observed if we measure the delay time between V_{out} and the output response of divider.

2.1.2 CP & LF

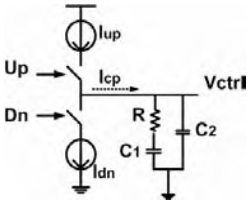


Figure 4. CP and LF

Figure 4 shows the common CP structure with a second-order low pass filter. Because the exact values of internal currents are hard to be observed, we use voltage-domain behavioral models that combine CP and LP together and measure the voltage changes instead of the actual current values. This approach allows us to consider the parasitic effects automatically without the actual values of equivalent RC components or pole/zero positions. The reasons will be explained in the following formulas.

In typical designs, the capacitance C_1 is often much larger than C_2 to obtain a reasonable phase margin. We define a parameter $\boldsymbol{\beta}$ to be C_1/C_2 and assume that $\boldsymbol{\beta}$ is a user-given large enough number. Then, we can get the impedance of the low pass filter (Z_{LF}) as shown in Equation 1. Using the result of Equation 1, we can have the transfer function of I_{cp} and V_{ctrl} as shown in Equation 2 under the assumption that $\boldsymbol{\beta}$ is large enough to be ignored. In this equation, parameter $\boldsymbol{V_{dc}}$ is defined as $I_{cp}R$ and parameter $\boldsymbol{V_{slope}}$ is defined as I_{cp}/C_1. In other words, we change the transfer function from the current form to the voltage form.

$$Z_{LF} = \frac{sRC_1 + 1}{s^2RC_1C_2 + s(C_1 + C_2)} = \frac{sR + \frac{1}{C_1}}{s(\frac{sRC_1}{\beta} + \frac{1+\beta}{\beta})} \quad (1)$$

$$V_{ctrl} = I_{CP}Z_{LF} = \frac{sI_{CP}R + \frac{I_{CP}}{C_1}}{\frac{s^2RC_1}{\beta} + s(\frac{1+\beta}{\beta})} \quad (2)$$

$$\approx \frac{sI_{CP}R + \frac{I_{CP}}{C_1}}{s} = I_{CP}R + \frac{I_{CP}}{sC_1} = V_{dc} + \frac{V_{slope}}{s}$$

In the stage 1 of the proposed input pattern, the "Up" signal of PFD will remain logic high for a long time so that the source current charges V_{ctrl} up to the Vdd gradually. According to equation 3, parameter $\boldsymbol{V_{slope}}$ is the rising slope of V_{ctrl}, as shown in Figure 5.

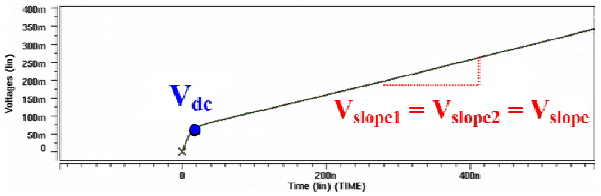


Figure 5. Waveform of V_{ctrl} in Stage 1

$$V_{slope} = \frac{I_{CP}}{C_1} \Rightarrow V_{slope} = \frac{\Delta I}{C_1} = \frac{\Delta V_{ctrl}}{\Delta T} \quad (3)$$

$$V_{dc} = I_{CP}R \Rightarrow V_{dc} = \Delta I \cdot R = \Delta V_{ctrl} \quad (4)$$

In typical designs, capacitances will be implemented by transistors. As shown in Figure 6, there are two different capacitance values with different responses on V_{ctrl} when the transistor is operated in the triode or saturation regions. This effect can be easily handled in our model if we measure two different values $\boldsymbol{V_{slope1}}$ and $\boldsymbol{V_{slope2}}$ for the different regions. If equivalent capacitance components are used, we can just set these two values to be the same one.

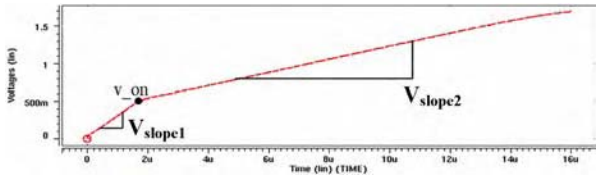


Figure 6. Waveform of V_{ctrl} with MOS Capacitances

About the parameter $\boldsymbol{V_{dc}}$, it can be viewed as the voltage variation of V_{ctrl} in Equation 4. Therefore, we can easily obtain it from the starting value of V_{ctrl}, as shown in Figure 5, because it is the voltage drop when the capacitors are not charged yet.

The other non-ideal effect of CP, current mismatch, can charge or discharge V_{ctrl} a little bit even when the PLL is locked. Therefore, the operation in stage 2 can be used to obtain this mismatch information. We define another parameter $\boldsymbol{e}$, which is the slope of V_{ctrl} waveform in the lock mode as shown in Figure 7, to represent the current mismatch. Using this parameter, we define the mismatch parameter $\boldsymbol{Mis}$ in Equation 5 to modify the output behavior of CP and LF in the reset situation so that the current mismatch effects can be included in our model.

$$Mis = 1 - \frac{V_{slope} - e}{V_{slope}} \quad (5)$$

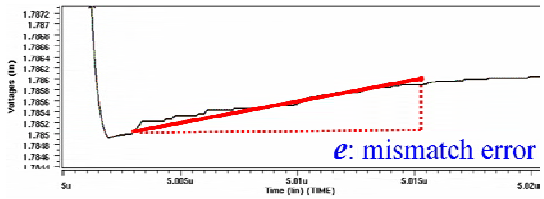


Figure 7. V_{ctrl} Variations in Stage 2

2.1.3 VCO

The critical concerns of VCO circuits are the gain (K_{VCO}), the range of input control voltage and the output

frequency. In the previous approach [4], curve fitting is used to model the behavior of VCO accurately. However, the extracted data must be large enough to have accurate coefficients of the fitting equations, which may increase the required simulation time for building the VCO model.

In fact, rebuilding the completed VCO response is not necessary because designers often prefer to operate VCO in the linear region as possible as they can. For this reason, a simple linear VCO model is accurate enough in the normal situation of PLL. According to the related study [7], linear VCO model can predict more than 90% of real VCO characteristics. Therefore, in our approach, we adopt linear VCO model to avoid long simulation time in traditional curve fitting approach.

In the stage 1 of the proposed input pattern, the output current of CP will charge V_{ctrl} up to the Vdd gradually. During the charging process, we can measure any two voltage values on V_{ctrl} (V_1 and V_2) and measured the corresponding output frequencies (F_1 and F_2) to calculate the gain of VCO (K_{VCO}), as shown in Figure 8. Since the operational range of VCO (V_{min} and V_{max}) is often clearly specified in the data sheet, we can build up the linear VCO model after the K_{VCO} is calculated. If these two values are not specified, we can measure the frequencies at V_{ctrl} = 0 and V_{ctrl} = Vdd to derive the V_{min} and V_{max} of this VCO according to the relationship of the measured K_{VCO}.

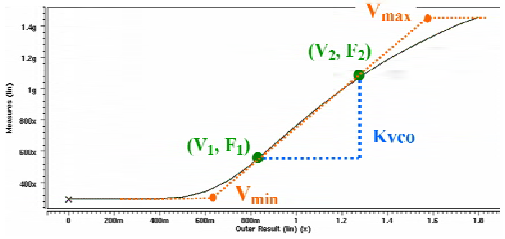


Figure 8. Relationship between V_{ctrl} and F_{out}

3. Modeling the Effects of Vdd Variation

In this section, we will introduce how to use the extraction results from only three post-layout simulations to determine the parameter values of our behavioral model under any given value change of supply voltage. Whatever form of supply voltage variation can be handled in our approach. Traditional Monte Carlo analyses can thus being avoided in this way.

In the proposed behavioral models shown in Section 2, all of parameters are extracted from voltage-domain measurement such that their changes under supply voltage variation are highly related to the variation of supply voltage. Therefore, we make an assumption that the distribution of those internal parameters in our behavioral models will be similar to the distribution of supply voltage variation, as illustrated in Figure 9. In other words, the 1σ values of those internal parameters obtained from MC simulation should be similar to the measurement results when the voltage change is also 1σ.

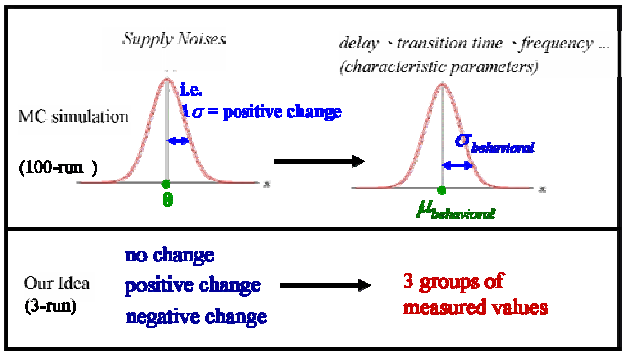


Figure 9. Supply Voltage Variation vs. Internal Parameters

Therefore, we use a Gaussian distribution as stimuli to do 100-run MC analysis and obtain the corresponding distributions of several important parameters of our behavioral models. Their 1σ values are compared in Table 1 with the measurement results when the voltage change is set as 1σ. From the results, we can see that the measured results using our approach are very close to the time-consuming MC simulation. Since the parameters obtained from this assumption are accurate, our behavioral models can still have accurate responses with those parameters.

Table 1. MC simulation (100-run) vs. Our Idea (3-run)

	MC (+1σ)	Measured	Error (%)
up_tr (s)	4.0374E-11	4.1283E-11	*2.25*
vco_tr (s)	3.8137E-11	3.8893E-11	*1.98*
div_tr (s)	3.4495E-11	3.5015E-11	*1.51*
up_tf (s)	3.5067E-11	3.5525E-11	*1.31*
vco_tf (s)	3.1734E-11	3.1958E-11	*0.70*
div_tf (s)	2.8987E-11	2.9328E-11	*1.18*
up_delay (s)	4.4566E-10	4.4624E-10	*0.13*
rst_delay (s)	3.1641E-10	3.1667E-10	*0.08*
vco_delay (s)	1.4448E-09	1.4475E-09	*0.19*
div_delay (s)	3.7085E-09	3.7185E-09	*0.27*
fmin (Hz)	3.1495E+08	3.1564E+08	*0.22*
fmax (Hz)	1.0025E+09	1.0035E+09	*0.10*
Kvco (Hz/V)	1.1590E+09	1.1660E+09	*0.61*
V_{dc} (V)	9.2416E-02	9.2763E-02	*0.38*
V_{slope} (V)	6.1743E+05	6.1539E+05	*-0.33*

Because we cannot predict the distribution of supply voltage variation accurately, we do need several post-layout simulations to have some samples on the real responses. In our approach, we only use three simulations to have three sets of characteristic parameters for the behavioral models when the supply voltage has no change, positive change, and negative change. The amount of supply voltage variation can be chosen arbitrarily. Since the changes of those internal parameters in our behavioral models are almost proportional to the value changes of supply voltage, we can determine the corresponding parameter values of the new behavioral model given any supply voltage changes (***dvdd***) using interpolation or

extrapolation from the measured results of these three simulations, as illustrated in Figure 10. In other words, using Equation 6 is enough to calculate the corresponding changes of characteristic parameters ($d_{behavioral}$). The hundreds or thousands of MC simulations can be avoided in this way and similar results can still be obtained.

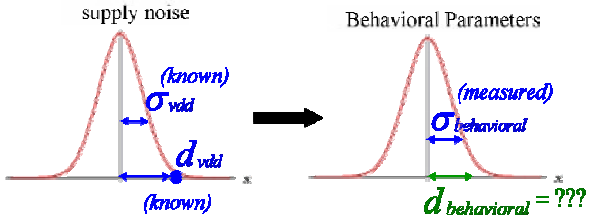


Figure 10. Relationship of the Variations

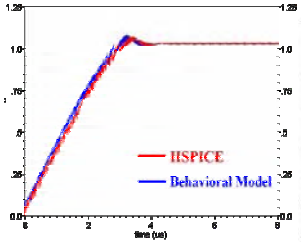
$$\frac{\sigma_{vdd}}{\sigma_{behavioral}} = \frac{d_{vdd}}{d_{behavioral}} \Rightarrow d_{behavioral} = \frac{\sigma_{behavioral}}{\sigma_{vdd}} d_{vdd} \quad (6)$$

In next section, we will demonstrate our idea by a real PLL case and use a Gaussian random generator to produce various values of supply voltage changes. Please note that any variation form can be handled using our approach. A random variation generator is just to produce some unspecified Vdd changes.

4. Experiments and Results

In order to demonstrate the accuracy of our PLL behavioral model under supply voltage variation, we use a PLL designed in TSMC 0.18μm CMOS process as an experiment. The value of F_{ref} is 50MHz and the output frequency (F_{out}) is 800MHz. In our approach, we only have to run three post-layout simulations to obtain three behavioral models when the supply voltage has no change, negative change, and positive change. In the experiment, we arbitrarily choose three values as the variations of supply voltage (dvdd), which are 0, -15mV and 60mV.

At first, we show the modeling results without supply voltage fluctuation. The overall impacts of those non-ideal effects often appear as the jitter form at the PLL outputs, which is also the critical concern of designers. Moreover, variations of V_{ctrl} are the important factor of output jitters such that we will focus on comparing the waveform of V_{ctrl}, output jitters, the lock voltage, and the lock time to the HSPICE results in Figure 11. The traditional behavioral models which are adopted from the Cadence's AHDL library are also compared.



	HSPICE	Tradition	Ours
V_{max} (V)	1.073	0.539	1.083
V_{lock} (V)	1.033	0.469	1.034
T_{lock} (μs)	3.536	1.820	3.366
ΔV_{ctrl} (mV)	7.03	~ 0	6.05
PJ (ps)	< 8	~ 0	< 7

Figure 11. Comparison Results (Ideal supply voltage)

As shown in the right side of Figure 11, the measurement results have demonstrated that the errors of maximum overshoot (V_{max}) and lock voltage (V_{lock}) are less than 1% by using our behavioral model. Compared to the results of HSPICE simulation, the lock time (settling time) and period jitter (PJ) of PLL are also very close. However, if we look at the simulation results of traditional behavioral model, the obtained values are quite different to the real values. In addition, the ΔV_{ctrl} response after locked is much more realistic by using our behavioral model because actual non-ideal effects have been successfully considered. If traditional behavioral model is used, there is almost no variation on V_{ctrl} after locked thus cannot produce any jitters. Those results can demonstrate that our behavioral model has accurate results with intrinsic noises in the ideal environment.

Then, we run the other two simulations when dvdd are -15mV and 60mV to obtain three sets of extracting results such that we can use interpolation or extrapolation to determine the parameter values of our behavioral model under any given value change of supply voltage. We use a random variation generator to produce various voltage variations for demonstrating our approach. In our experiments, 60mV is chosen as the 1σ value and the ideal case is the mean value (μ) for a Gaussian random generator. The worst case sampled near ±3σ is closed to 0.1Vdd, which is a reasonable variation value. As shown in Figure 12, which is the various settling responses on the V_{ctrl} waveform, our noise aware behavioral models are indeed sensitive to Vdd variations.

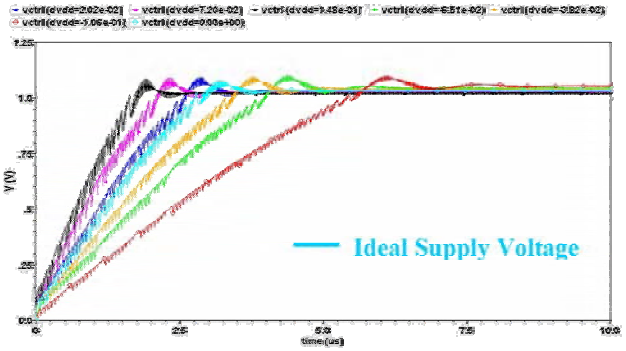
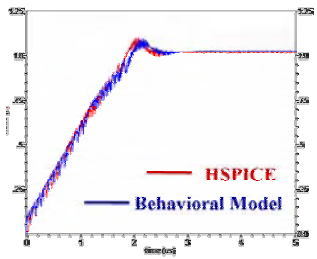


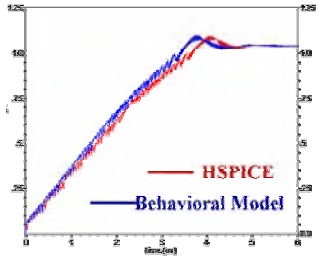
Figure 12. V_{ctrl} Responses with Supply Voltage Variation

In order to check the detailed output responses, we choose two arbitrary variation values (93.1mV and -38.2mV) produced by the random generator and observe their corresponding results. We also compare several critical parameters of PLL designs with the results of HSPICE simulation in Figures 13 and 14. We can see that the results of our behavioral models are still accurate under supply voltage variation. Since the traditional behavioral models cannot produce any output jitters as shown in Figure 11, their results are not compared in the following noisy conditions any more.



	HSPICE	Ours
V_{max} (V)	1.101	1.100
V_{lock} (V)	1.018	1.023
T_{lock} (μs)	2.163	2.263
ΔV_{ctrl} (mV)	8.39	7.84
PJ (ps)	< 9	< 9

Figure 13. Results Comparison when dvdd = 0.0931V



	HSPICE	Ours
V_{max} (V)	1.095	1.100
V_{lock} (V)	1.040	1.039
T_{lock} (μs)	4.107	3.864
ΔV_{ctrl} (mV)	6.57	5.40
PJ (ps)	< 7	< 6

Figure 14. Results Comparison when dvdd = -0.0382V

Finally, more random variation values are considered and the corresponding output responses on period jitter and lock time are shown in Figures 15 and 16. These two parameters are highly sensitive to the supply voltage and they are also the very important concerns of PLL designers. When the supply voltage variation is increasing, our behavioral models can still obtain similar lock time as in the HSPICE simulations. About period jitters, the simulation results of our behavioral models are also close to the HSPICE results with the supply voltage fluctuation. These results can show that we can build accurate behavioral models for PLL designs under any given value change of supply voltage.

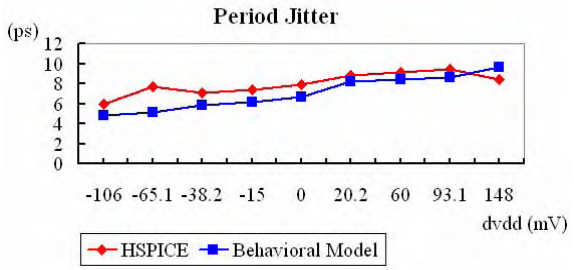


Figure 15. Agreement on Period Jitter

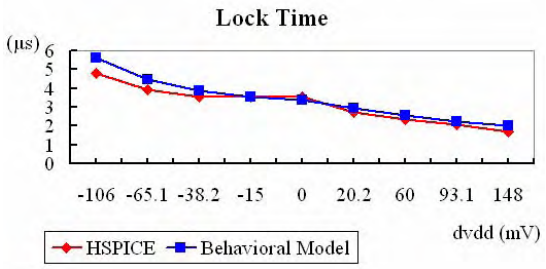


Figure 16. Agreement on Lock Time

5. Conclusions

An efficient modeling approach with the effects of supply voltage variation is presented in this paper to build accurate PLL behavioral models in a short time by using our bottom-up extraction flow. Because all the parameters in our behavioral models are obtained from voltage-domain measurement, their changes under supply voltage fluctuation are almost proportional to the value changes of supply voltage in our observation. Therefore, only three post-layout simulations are enough to generate accurate behavioral models under different supply voltages. This approach can handle any distribution of supply voltage variation and avoid time-consuming MC simulation. Moreover, because no exact current values and device sizes are required in our model, this approach will be more suitable to verify the system performance with the effects of non-ideal supply voltage while using existing IP designs. The experimental results have shown that our behavioral model can have very similar results to the HSPICE simulation but require much less simulation time.

6. References

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