A contribution to a virtual prototyping for a spread spectrum telecommunication system using VHDL-AMS

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Abstract

This paper presents a virtual prototype for a home automation spread spectrum (DS-SS) telecommunication system based on the VHDL-AMS high level language. A specific additive white gaussian noise channel generating a automatic noise level is presented here along with the Box-Muller generation method that allows the user to set the signal to noise ratio parameter (SNR) directly. Simulations and synthesis results dedicated to a FPGA prototype are also presented, in term of size and power consumption.

1.INTRODUCTION

1.1 Context And What The Stakes Are

Today, requirements in system design are extending more and more from electronic design (analogical or digital) to multidiscipline design (analogical and digital, thermal, mechanical ,etc). These current needs imply, as well on industrial as on research laboratories level, the implementation of methodologies to optimize and to make the CAD product reliable. These new methodologies allow to reduce the gap between the linear evolution of designer productivity and the exponential one of hardware circuits complexity. For that, the International Technology Roadmap for Semiconductors (ITRS) [1] recommends the creation and reuse of multidiscipline libraries (analog/mixed-blocks) dedicated to hierarchical design and heterogeneous SOC integration (modeling, simulation, verification, test of components blocks).

Thus, our conception approach of mixed analog and digital circuits is based on a virtual prototyping platform [2] using a high level description language. The aim of the methodology presented in this paper allows to get a flexible, reusable and standard-language-based prototype.

In the article, we are going to present the modelisation of a wireless spread spectrum system allowing the communication on a same broadband of different sensors dedicated to a closed environment. Indeed, communication in a closed environment leads propagation constraints that force us to investigate the technical and technological parameters of the system considered. Therefore we considered a CDMA (Code Division Multiple Access) multiplexing which brings many advantages, as a single carrier for all users with random access to the medium, immunity to interference and multipath effects, or private nature of the information through a code-based addressing. The detailed characteristics of our system have already been presented and validated in literature [2,3]. In addition, by spreading the transmitted signal, data can be transmitted with a power « polluting » less the frequency spectrum and generating less interference for other radio receivers (cordless and mobile phones, modems, TV sets, radio sets, …) .

The modelisation of this system of spread spectrum allowed us to design a prototype of telecommunication as it is shown in figure 1.

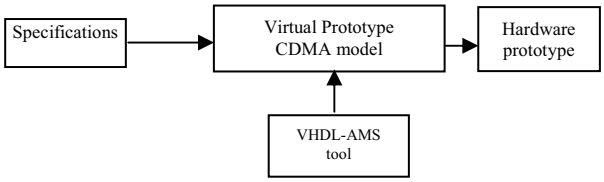

Figure.1. Telecommunication prototype development.

The aim of our approach is to develop a CDMA indoor communication prototype, by offering a virtual VHDL – AMS prototype, based on reusable libraries that we have specifically created.

After presenting the design method for this mixed system, based on high level VHDL-AMS language which enables to describe the analogical and digital unit of the telecom system simultaneously, we will present the spread spectrum telecommunications system in the form of functions as well as its simulation parameters as for example the spreading code, the sample frequency or the noise level in the channel appropriate to our application. Then, we will focus on the elements which need to develop new models as they don't exist in the VHDL-AMS norm, i.e a AWGN (Additive White Gaussian Noise) channel including a BER(Bit Error Rate) self-calculation module. The last part will deal with different simulations based on the principle of the spread spectrum

like the correlation function for example. We will finally present our first synthesis results obtained with Quartus II software in the aim to implanting FPGA stratix II type. We will compare the different functions implanted at the transmitter's and transceiver's level in terms of number cells and consumption.

1.2. Conception Methodology

Today the recent IEEE 1076.1 (VHDL – AMS) [3] standard allows designers to develop analogical and synthesizable digital functions in VHDL-AMS simultaneously. This language has permitted us to code both analogical stages in VHDL-AMS and the digital stage in synthesizable VHDL. In a second step, temporal and frequential analysis prove that our architecture is working and key parameters can be optimized (Constant time, Process Gain…).

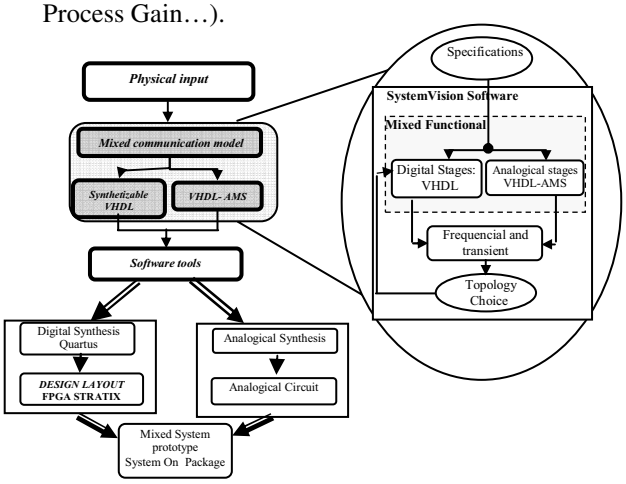

Figure.2 . Virtual prototyping design flow.

The architecture being chosen, the next step is the synthesis of the analogical part (for the stages in VHDL-AMS) and the digital synthesis (for the synthesizable VHDL stages). From each synthesis we will obtain circuits which will be together in the final system of SOP type.(System On Package).
CDMA prototype, which will be presented in the next paragraph is a mixed system whose most significant physical variables will be transferred in the high level parameter i.e for main examples the spread code, the number of branches in the serial acquisition or the noise level in the channel.

2. MIXED MODEL PRESENTATION

2.1. Telecommunication Model

The system that we investigate can assume the communication between the different sensors (Temperature, Position or Video) in a unique frequency band (Bandwith 80 MHz) [4][5]. The architecture of the transceiver is based on spread spectrum technique using a Binary Phase Shift Keying modulation (BPSK) [6]. The data rate is configurable between 19 kbps and 5.7 Mbps by the spreading code length N (7<N<2047) decided by the user. Figure 3 shows the global block diagram of our system.
The transmitter allows to code the signals from the sensors and to spread out the encoded signal with a personal Pseudo-noise code (PN-Code). The radio frequency stage (RF) emits the spreaded signal over a carrying 2.44 GHz frequency.
The multi-user transmission channel is composed of a AWGN noise generator and configurable delays to modelize multipaths effects.

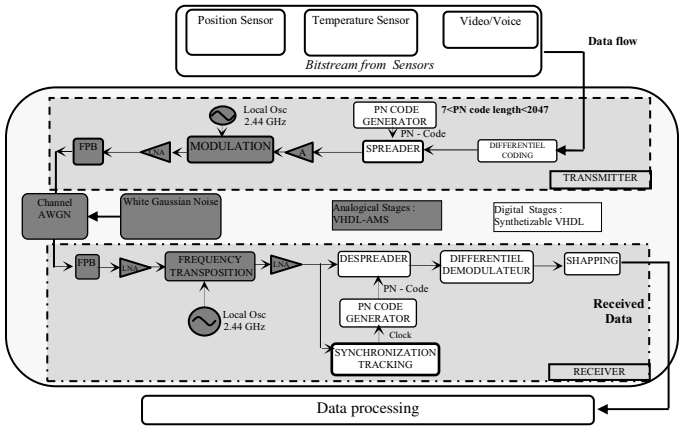

Figure.3. Block Diagram of the transceiver model.

The receiver allows to despread the received data and to recover the emitted frame. It is performed by using digital circuits for Serial synchronization and Delay Locked Loop system (DLL) for the tracking.
To perform this operation properly, the spread spectrum communicative systems require the locally generated spread code to be synchronized, then maintained synchronized (tracking) with the received sequence.
This table below sums up the different simulation parameters presented in our telecommunication system. This mixed system, composed of digital elements (coding, spread….) and analogical (channel, RF layers) is implanted in VHDL-AMS.
The user thus has a complete model at his disposal, in which the majority of the variables appropriate to the physical constants of the analogical and numerical telecommunications circuits are parametrable. The user may change the order of a digital filter as well as modulate the signal noise ratio at the receiver input.

Functions			Signal type (Clock frequency)	Characteristics
TRANSMITTER				
Differential Coding			Digital (40MHz)	Fosc=2.66 MHz Cycle Duty 0.5
Spreader			Digital (40MHz)	X-or Gate
PN Code Generator			Digital (40MHz)	Multi-rate , Galois, M-sequences 7<Spread Factor <2047
Radiofrequency Functions			(Analogical)	2.44 Ghz , 80 Mhz Bandpass
CHANNEL				
AWGN Additive White Gaussian Noise			(Analogical)	Band Path= 40 MHz, Cut off frequency =160MHz
RECEIVER				
Synchronization, Tracking, PN –Code Generator	SERIAL Search	Correlation	Digital (160MHz)	Product , 2nd order filter and square
		Digital Threshold control	Digital (40MHz)	Threshold correlation =1.5V
		Clock	Digital (40MHz ou 160 MHz)	Period = Tc=25ns
	Tracking DLL	Discriminator	Digital (160 MHz)	Product , 2nd order filter
		Loop Filter	Digital (160MHz)	1st Order, $\frac{1}{1+\tau s}$ τ=1µs
		NCO	Digital (640MHz)	K_{NCO} =100kHz/V Fo=160MHz
		PN Code Generator	Digital (40MHz)	M-Sequences
Despreader			Digital (160MHz)	Product , filter

Table.1. Main Parameters defining the transceiver model.

2.2. Additive White Gaussian Noise channel implementation

As the noise libraries are not implemented in VHDL-AMS language, we have developed a channel model based on the Box-Muller noise generation method [7][8][9], allowing the user to set directly the Signal to Noise Ratio parameter (SNR). This AWGN channel is composed of a white Gaussian noise generator added to the emitted signal on the carrier frequency. The white noise is generated by the UNIFORM function [10] from the "math-real" library. This function returns a pseudo-random "x" number with uniform distribution in the open interval [0. 0, 1.0]. In order to get a white Gaussian noise we used the Box-Muller transformation which allows to generate the noise signal :

$$noise = \sqrt{-2\ln x_1} \times \cos(2\pi x_2) \qquad (1)$$

where x_1 and x_2 are two random variables generated by the UNIFORM function.

The noise signal is managed by a normal distribution with a mean equal to zero and a variance σ^2 equal to one.

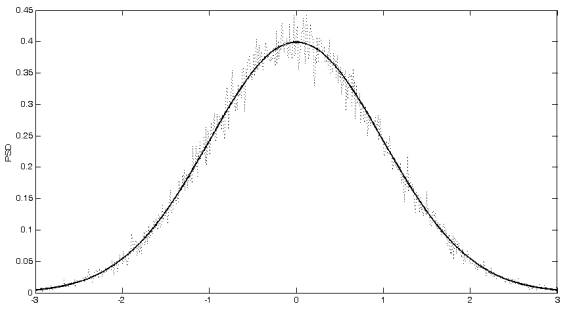

Figure.4. Theoretical (continuous line) and computed PSD of additive white gaussian noise under VHDL-AMS.

Figure 4 represents the Power Spectral Density (PSD) coming from the noise generated in VHDL-AMS, compared to the theory (continuous line) under Matlab™ and that validates the model of noise generation.

By automatically measuring the noiseless signal level "V_input" in the channel (after attenuation and delay), the "level" parameter is adjust to keep up SNR to the desired value.

$$Level\_dB = V\_input\_dB - SNR\_dB \qquad (2)$$

where "level" represents the noise amplitude necessary for desired SNR achieving.

The final amplitude of the noise signal is finally set by the following equation :

$$noise\_generator\_out = 10^{(Level\_dB/20)} \times noise \qquad (3)$$

The figure below shows VHDL-AMS syntax for the global AWGN channel process using the Box-Muller noise generation method.

Listing 1. AWGN channel model.

```
Entity canal is
Generic ( T1: time:=10ns; SNR : real:=10.0 );
Port (terminal transmitter_output, ref, receiver_input: electrical);
End canal;

Architecture arch of canal is
…
Generation_WGN:process
 variable seed11:integer:=2000;
 variable seed12:integer:=10000;
 variable x,y::real;

 begin
    uniform(seed11, seed12, x1);
    uniform(seed11, seed12, x2);
    noise<=sqrt(-2.0*log(x1))*cos(2.0*math_pi*x2);
                    //White Gaussian noise generation
    wait for 1 ns;
    level <= (ve_db –SNR);
    noise_generator_out <= 10.0 **(level/20.0)*noise;

end process Generation_WGN;

break on noise_generator_out;
vo==ve' DELAYED (T1) + noise_generator_out;
                    //vo = receiver input et ve=transmitter_output
end architecture arch;
```

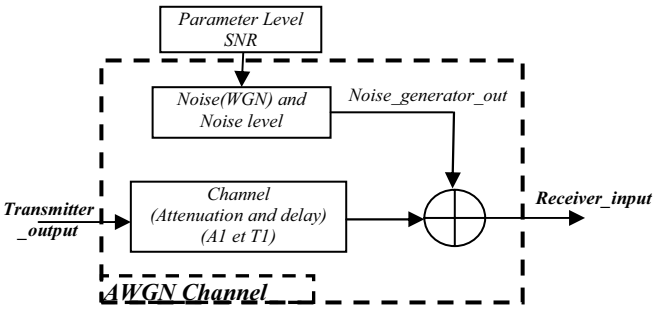

Figure.5.AWGN channel topology.

3. SIMULATION RESULTS

3.1 Functional Validation

3.1.1 Cross-correlation function $R_c(\tau)$

The first step to validate the spread spectrum communication consists to simulate the fundamental function, i.e the cross-correlation function. This function is composed of two elements which are the multiplier and the integrator dump as shown on the next figure (Figure 6).

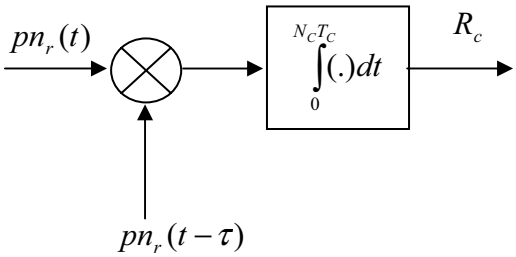

Figure. 6.Receiver cross-correlation topology.

The product block multiplies the signal received $pn_r(t)$ by the delayed local spread code generated in the receiver $pn_r(t-\tau)$.

The Pseudo Noise code is a pseudo-unpredictable sequence, also called PN-CODE, of period N_c and of no average. Ideally, its cross-correlation is maximal for a null delay. Which is why when the code is synchronized with that of the emission at reception we can detect it easily. If on the contrary the code of reception is not synchronized with that of the emission then the correlation signal is low and difficult to detect.

This cross-correlation $R_c(\tau)$ function is mathematically expressed by the following equation [11] where Tc is the chip time, N_c is the number of bits of the spread code, τ the delay between the received signal ($pn_r(t)$) and the local PN-Code ($pn_r(t-\tau)$) and R_c being the cross-correlation function result.

$$R_c(\tau)=\int_0^{N_C T_c} pn(t)pn(t+\tau)dt=\begin{cases}1+\dfrac{\tau}{T_c}\left(1+\dfrac{1}{N_C}\right) & \text{For } 0\le \tau \le Tc\\ -\dfrac{1}{N_C} & \text{For } Tc< \tau<(N_c-1)Tc\\ \dfrac{\tau}{T_c}\left(1+\dfrac{1}{N_C}\right)-\dfrac{1}{N_C} & \text{For } (N_c-1)Tc \le \tau \le N_c\ Tc\end{cases} \quad (4)$$

The simulation results of the cross-correlation function by means of the tool SystemVision at the level of the receiver are presented on the following figure.

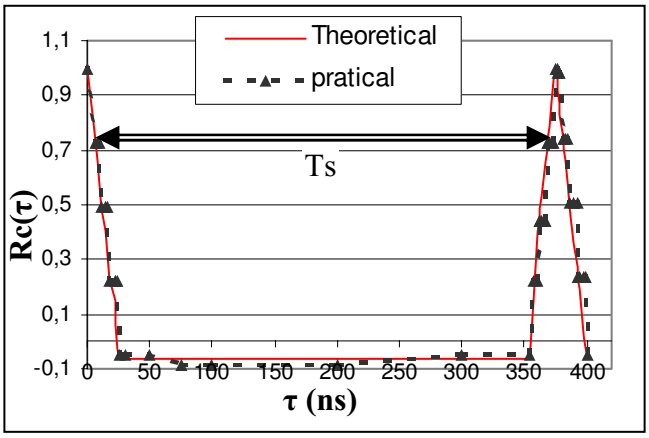

Figure.7. Theoretical (continuous line) and simulated (dotted line) cross-correlation function for N=15 and T_c=25 ns.

The figure 7 shows the result of the cross-correlation function. This function has a periodicity of time Ts (Ts representing the time of a symbol) fixed here to 375 ns (N=15). Compared to equation 4, these results allow to validate our function of correlation, showing a maximum when the correlation is effective.

3.1.2. Noise generation validation

Our study on the channel deals with the level of parametrable signal to noise ratio here fixed to 15dB. The transmitter output signal (Fig. 8-a) is under a 2.44 Ghz carrier frequency. The noise signal is characterized by a mean value equal to zero (Fig. 8-b), and is weighted to achieve the desired Signal to Noise Ratio (Fig. 8-c). Finally the last signal represents the receiver input (Fig 8-d).

Figure 9 presents the power spectrum density of noise signal generated for two signal to noise ratio levels. For each one, the mean value is equal to zero and only the variance is a function of the signal to noise ratio value. These results allow to validate the AWGN channel modelied in VHDL-AMS.

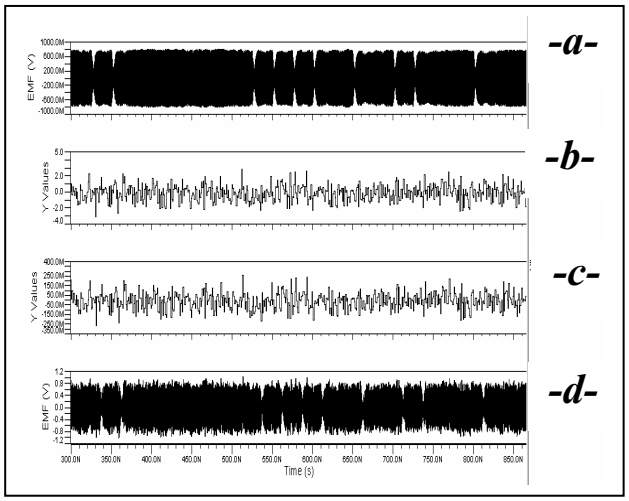

Figure.8 . Computed signals involved in VHDL-AMS channel model : transmitter output (a), noise generator output (b), weighted noise generator output for SNR = 15dB (c) and receiver input (d).

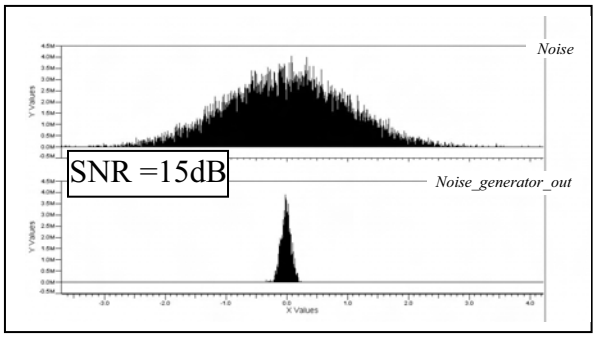

Figure. 9. PSD of noise signal for 15 dB noise level.

3.2. Synthesis Results

We now investigate the implementation of the main transmitter and receiver digital functions. For that, a FPGA (type STRATIX/ALTERA) has been chosen, due to its easily re-computable and low developing time functions. Nevertheless, only the synchronisation organ (Search Serie and Tracking) has not been implemented and the implementation of these functions is in progress. These synthesis has been performed by using Quartus II software tool.

The next figure shows the FPGA synthesis results of the global transceiver in terms of number of digital cells (combinatory and sequential) and power consumption under 3.3 volts voltage supply. We observe that the number of combinatory and sequential cells is practically balanced, with nevertheless a higher digital elementary circuits for the receiver. We can explain this result by the fact that the correlation needs to implement an integrator-and-dump block. Finally, we can notice that the clock control stage consumes 10 times more than the other receiver blocks, which is the most important synthesized function.

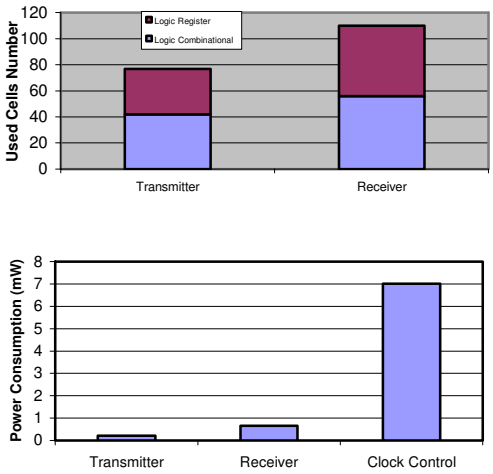

Figure.10. FPGA size (number of cells) and power consumption for global transceiver synthesis.

The last next part of the presented work deals with detailed synthesis results for each main functions of the emitter and the transceiver.

3.2.1. Transmitter unit

Figure 11 shows the detailed circuits topology and associated power consumption for each elementary digital function, that is to say the BPSK differential encoder, the multiplier, and configurable Galois type pseudo-noise code generator adjustable in length by means of a four-bit word (maximal length 2047).

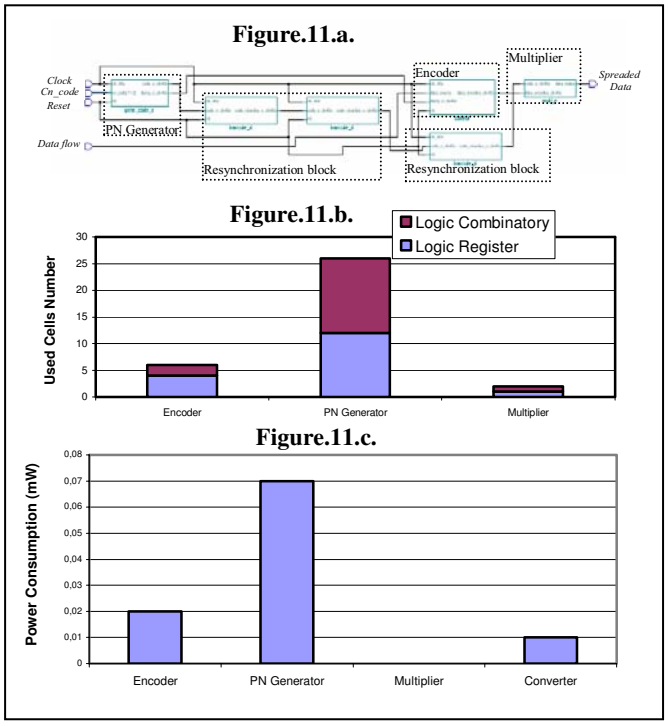

Figure 11. Detailed synthesis results : involved digital functions (a), size results (b) and power consumption under 3.3V power supply (c) for the transmitter.

It will be noticed that the function comprising the greatest number of cells in use is that of the pseudo-noise code generator. Thus is to be expected as it allows generation of both N=7 and N=2047 codes. As for power levels, it will further be noticed that it is this same component which is the highest level consumer at the transmitter stage.

3.2.2.Receiver Unit

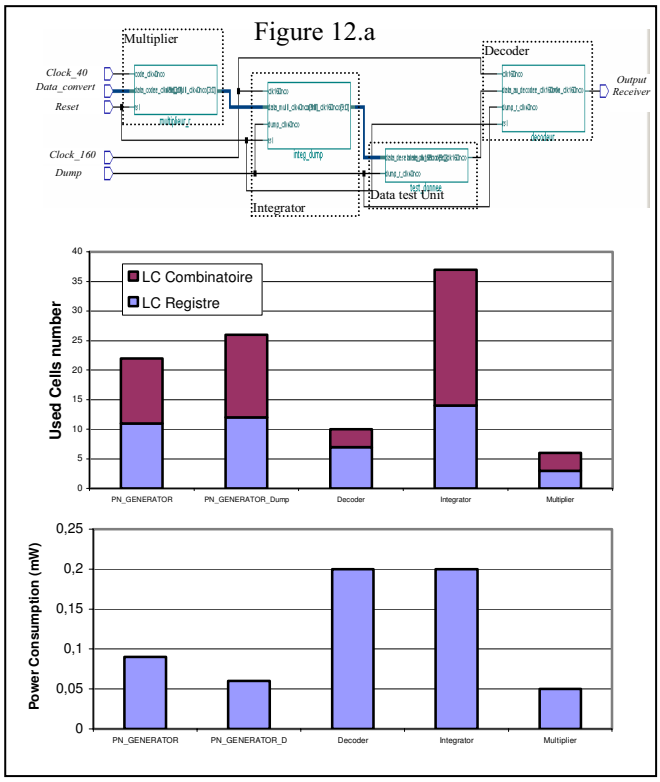

Figure 12 . Detailed synthesis results : involved digital functions (a), size resuls (b) and power consumption under 3.3V power supply (c) for the receiver.

Figure 12 shows the detailed circuits topology and associated power consumption for each elementary digital function, that is to say the pseudo-noise code generator, the differential decoder, the Integrator / Dump block, the multiplier and finally the data test unit.

On the receiver unit, it is the integrator-dump which comprises the greatest number of cells. This component uses one third more than the code generator at reception stage (the same as for the transmitter).

The final parameter examined here following this first attempt at synthesis is the sampling frequency. Quartus II software is used to calculate data propagation time for the worst possible case. The result obtained here is a time of 2.15 ns giving a maximum frequency of 464 MHz. However, this would certainly be a critical frequency once the final VHDL files are integrated, as these are the synchronization and follow-up frequencies.

4. CONCLUSION

We presented this model of a spread spectrum telecommunications system by starting with the description of our design philosophy. This approach was therefore applied to a mixed spread spectrum system. We then expounded the various model simulation parameters, focusing on the additive white Gaussian noise channel. The noise proofed channel was modeled using the BOX-MULLER method, allowing generation of a Gaussian noise factor. In addition, we integrated a parameter allowing self-adjustement for different noise levels. These new developments in channel design were checked by simulation. We then presented the modelisation of two essential parts of a spread spectrum system, i.e the cross-correlation function and the tracking unit, the models being validated by simulation. Following this simulation process on the mixed model, we carried out our first synthesis trial using digital files (VHDL). This stage of the work was effected on a FPGA of the ALTERA group. We then studied the various logical approaches which would allow us to complete synthesis. The final stage was to simulate consumption levels for each function.

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