VHDL-AMS Behavioral Modelling and Simulation of High-Pass Delta-Sigma Modulator

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ABSTRACT

High-pass $\Delta\Sigma$ modulator has the advantage of immunity from the low frequency noise and is thus very effective in the parallel architectures. In this paper, we present the behavioral modelling and simulation of $\Delta\Sigma$ modulators in VHDL-AMS, and in particular of the high-pass modulator. A set of models in VHDL-AMS suitable for time-domain behavioral simulation of SC $\Delta\Sigma$ modulators is developed. The proposed set of models takes into account at the behavioral level most of SC $\Delta\Sigma$ modulator nonidealities, such as jitter noise, kT/C noise, $1/f$ noise, amplifier noise, switch nonidealities, amplifier nonidealities, and capacitor mismatch. We elaborate then a top-down design methodology that is validated by the measurement results.

1. INTRODUCTION

Primarily because of advances in VLSI technologies, among various types of ADC, that based on oversampling and $\Delta\Sigma$ modulation has become more and more attractive in applications requiring high precise A/D conversion with narrow bandwidth [1]. Without considering the inherent internal circuit noise, the oversampling and $\Delta\Sigma$ modulation can perform extremely high resolution ADC without high accuracy device matching. In practical, however, the circuit low frequency noise, such as flicker noise, offset noise and clock feedthrough noise, always exists in the circuit and seriously degrades the performance of the $\Delta\Sigma$ modulators. To overcome this problem, we can use high-pass (HP) modulator combining with chopper-stabilized technique [2, 3]. Moreover this kind of modulator is efficient in the parallel architecture [2, 4].

A significant problem in the design of $\Delta\Sigma$ modulators in general and HP modulators in particular is the estimation of the nonideality effect on their performance, since they are mixed-signal nonlinear circuits. Due to the inherent nonlinearity of the modulator loop, the optimization of the performance has to be carried out with behavioral time domain simulations. Naturally, circuit level simulation is the most accurate. However, the evaluation of the circuit nonidealities effect and the optimization of the building blocks embedded in the modulator are very difficult to handle because of the lengthy simulation time. Indeed, the essence of the traditional circuit simulators is based on complicated element models. If these simulators are used for designing $\Delta\Sigma$ modulators, lengthy simulation time will make the simulator impractical to co-simulate and verify both analog and digital circuits. Moreover, for HP modulator, it is very important to determine the threshold value of the capacitor mismatch and op-amp performance insuring the stability of the modulator. Such a determination is impossible with transistor-level simulations. An intermediate stage of behavioral simulations is necessary. Through multi-level abstraction models, VHDL-AMS is suitable for this task. Moreover, it allows a top-down methodology of design. An efficient behavior model in VHDL-AMS reduces simulation time and reflects phenomena of circuit nonidealities. It allows us to determine possible ranges of circuit specifications with reasonable design margins in view with the circuit implementation.

In this paper, we present a brief overview of HP $\Delta\Sigma$ modulator. Individual blocks building the HP modulator are then modelled in VHDL-AMS. Various nonidealities are described and modelled. The effect of nonidealities on the modulator performance is analyzed to determine the specification for each modulator building block. Finally the simulation results are compared with the measurement results to validate the top-down methodology.

2. HIGH-PASS DELTA-SIGMA MODULATOR

HP $\Delta\Sigma$ modulator is based on the same principle as low-pass modulator i.e. the quantization noise is shaped away from the signal band by the loop filter [1]. The only difference being the position of the signal band, which is now located as $f_s/2$, f_s is the sampling frequency, compared with a pass-band at dc for the low-pass $\Delta\Sigma$ modulator. In the HP modulator, the quantization noise is shaped to low frequency band that covers completely the low frequency noise. The HP modulator is therefore immune to low frequency noise [2]. Hence, it is very efficient in parallel architecture [2] or in a chopper-stabilized configuration as shown in Figure 1(b). For example in the latter case, the immunity of the HP modulator to the low frequency noise is shown by studying the input signal evolution in Figure 1(c).

The HP $\Delta\Sigma$ modulator can be realized by applying the transformation, $z \rightarrow -z$, to a low-pass $\Delta\Sigma$ modulator [2]. The block diagram of the second-order HP $\Delta\Sigma$ modulator is represented in Figure 1(a). The high-pass filter that is a basis component of the HP $\Delta\Sigma$ modulator can be implemented as described in Figure 1(d) which is based on the approach of introducing an extra feedback loop around an integrator [5]. Sign change in the extra feedback loop is obtained thanks to fully differential implementation. To simplify the

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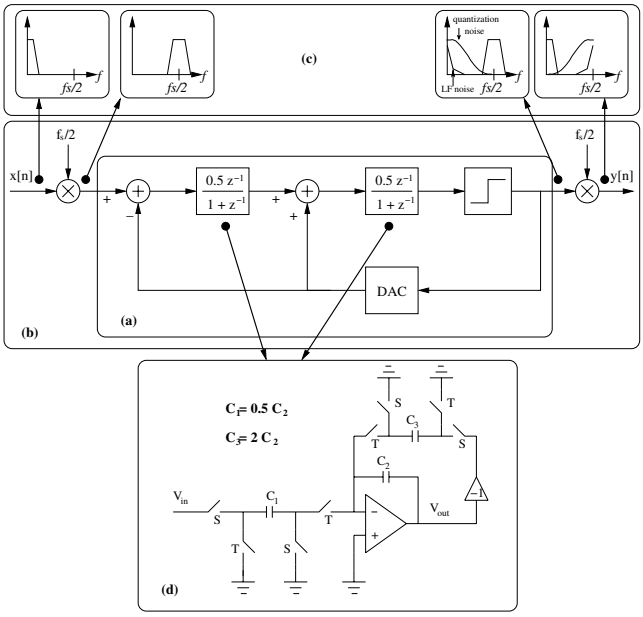

Figure 1: (a) The block diagram of the second-order HP $\Delta\Sigma$ modulator. (b) The chopper-stabilized configuration. (c) The input signal evolution and quantization noise shaping. (d) The implementation of high-pass filter, the basis block of the HP modulator.

analysis, non-differential circuit is presented in this figure.

3. COMPONENT MODELS

Along with the ability to describe multi-abstraction models, the power of VHDL-AMS relies on the fact that it allows the model designer to focus on detailling the constitutive equations of the inner submodels. VHDL-AMS takes advantage of a graph-based conceptual description to automatically compute the equations describing the conservative laws of the global model. The vertices of the graph represent effort nodes (across quantities like voltage) in the circuit, and the edges represent branches of the circuit through which information flows (through quantities like current). Thus, the assembling of complex systems is nothing more than connecting elementary objects through terminals capable of exchanging information, in such a way that the conservative semantics of the generalized Kirchoff laws are preserved. For this reason, instead of presenting complete VHDL-AMS code of complex model, we present how the model is described for each elementary block of the modulator.

Figure 1(a) shows the block representation of the second-order HP $\Delta\Sigma$ modulator. The basis blocks of this modulator are : a high-pass filter, a comparator and a DAC. The high-pass filter is the critical block because its nonidealities affect highly the performance of the HP modulator and even its stability as explained in [2, 5]. This filter is built by switches, capacitors and op-amp as shown in Figure 1(d). The nonidealities degrading the HP modulator performance can be implemented separately by including imperfections in the behavior model of each building block: op-amp, switch, capacitor, comparator and DAC.

The hierarchical representation of VHDL-AMS allows us to select adequate model complexity in order to reduce simulation time. The methodology to model individual blocks is as follows : nonideality parameters of each block are introduced step by step once they have been validated through block simulation. The more complex is the model, the more accurate behavior of the component is obtained, but the longer simulation time is needed. There is therefore a tradeoff to do between the model accuracy and the simulation time. We used for simulation ADVanceMS from Mentor Graphics because ADVanceMS is a multilingual mixed-signal mixed-mode simulator and it simulates, simultaneously, VHDL-AMS and SPICE described circuitry, in any combination.

3.1 Clock Jitter Noise

The operation of a SC circuit depends on complete charge transfer during each of the clock phases [6]. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of the clock jitter on a SC circuit is completely described by computing its effect on the sampling of the input signal.

As in any sampling system, clock jitter in HP $\Delta\Sigma$ modulators results in nonuniform sampling and can introduce errors into the sampled values that increase the total error power at the quantized output. The magnitude of this error depends on both the statistical properties of the jitter and the modulator input signal.

The analysis of jitter begins with the sampling model shown in Figure 2(a). The input signal, $x(t)$, is assumed to be sam-

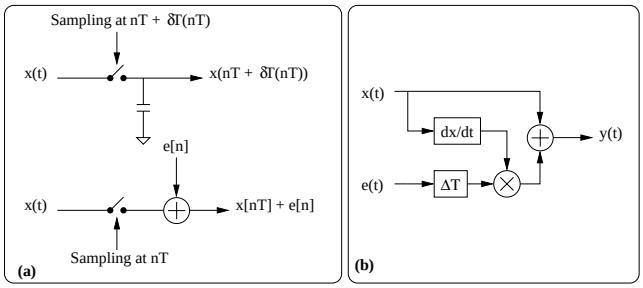

Figure 2: (a) Discrete model of the sampling process when the sampling time nT is perturbed by a random process $\delta T(t)$. (b) Model of a random sampling jitter : x(t) is the input signal, e(t) is white noise with mean value, 0, and standard deviation, 1.

pled at $t = nT + \delta T(nT)$, where $\delta T(t)$ is a random process that models the perturbation of the actual sampling instant from the ideal nT. The error that results from jittered sampling, $e[n]$, is defined as

$$e[n] = x(nT + \delta T(nT)) - x(nT). \quad (1)$$

Because $\delta T(nT) << T$, (1) can be approximated using a first-order Taylor expansion as

$$\begin{aligned} e[n] &\approx x(nT) + \delta T(nT)\, x'(nT) - x(nT) \\ &= \delta T(nT)\, x'(nT), \end{aligned} \quad (2)$$

where $x'(nT)$ is the derivative of $x(t)$ at $t = nT$.

Assuming the sampling clock jitter, δT, to be a Gaussian random process with standard deviation, ΔT, and to be white, the sampling clock jitter model is given by equation (2). The effect of clock jitter then is simulated at behavioral level by using the model shown in Figure 2(b). The modelling of the clock jitter effect leads to modelling white noise in VHDL-AMS that will be presented in Subsection White Noise Model.

3.2 Switch Noise

Two noise sources intrinsic to the MOS switches, thermal noise and flicker noise ($1/f$ noise), can potentially perturb the high-pass filter operation and increases the total error power at the output of the HP $\Delta\Sigma$ modulator. Thermal noise is associated with the random motion of carriers in the resistive channel, and $1/f$ noise is associated with flow of direct current in the device. In the analysis of switch noise below, $1/f$ noise is considered negligible because it is assumed that there is no static current flowing through the switched capacitors, and hence, none through the MOS device [7].

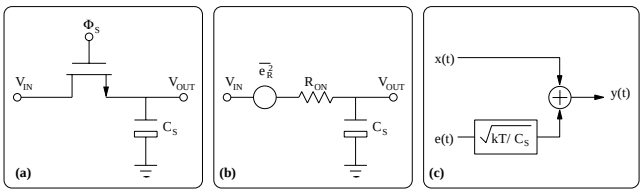

Figure 3: (a) MOS sample-and-hold. (b) Its equivalent noisy circuit when Φ_S is high. (c) Thermal noise model : x(t) is the input signal, e(t) is white noise with mean value, 0, and standard deviation, 1.

The thermal noise contributed by the MOS switches in the high-pass filter can be estimated by modelling each switch with the sample-and-hold circuit shown in Figure 3(a). When Φ_S is high and the MOS switch is on, the channel is modelled as a noiseless resistor, R_{ON}, in series with a noise source, e_R (Figure 3(b)), that has a power spectral density

$$S_R(f) = 4kTR_{ON}, \qquad 0 < f < \infty \tag{3}$$

where k is Boltzmann's constant and T is absolute temperature. The power of the noise sampled onto capacitor C_S is determined by integrating the noise power spectral density, $S_R(f)$, shaped by the transfer function of the low-pass filter formed by R_{ON} and C_S.

$$P_{out} = \int_0^\infty 4kTR_{ON}\frac{df}{1+(2\pi f R_{ON}C_S)^2} = \frac{kT}{C_S}. \tag{4}$$

Since the sampling frequency, f_s, is much lower than the circuit bandwidth set by R_{ON} and C_S, the process of sampling the switch noise results in the concentration of the total noise power kT/C_S into the sampling bandwidth, $-f_s/2$ to $f_s/2$. The switch thermal noise is then modelled as an additive white noise source of variance kT/C_S to the input signal as shown in Figure 3(c). Modelling of thermal noise effect like that of jitter noise, leads to model a white noise source in VHDL-AMS that will be presented in Subsection White Noise Model.

3.3 Operational Amplifier Noise

In addition to kT/C noise from the switches and jitter noise, noise from the op-amp also degrades the performance of the modulator. In the following analysis, it is presumed that all noise sources within the amplifier can be referred to a source at the amplifier's non-inverting input, denoted e_{amp}. The analysis is simplified by using a single-ended representation of the filter (Figure 1(d)), but no error is inherent in this simplification if e_{amp} is defined to be equal to the input-referred noise of the fully differential amplifier used in the fully differential filter. Capacitor C_3 is chosen to be $2 \times C_2$ to yield the desired high-pass transfer function. Capacitor C_1 is unspecified in the following analysis because it only affects the gain of the filter through the ratio C_1/C_2.

The input-referred amplifier noise spectral density, $S_{amp}(f)$, typically consists of a white noise component, characterized by a power spectral density that is constant with frequency, and an $1/f$ noise component that is inversely proportional to frequency. The effect of $1/f$ noise is studied in detail in Subsection Noise Effect. It will be shown that $1/f$ noise can be neglected because it is concentrated in a narrow region around dc, whereas the useful signal is centered at one-half of the sampling frequency, $f_s/2$. The input-referred amplifier noise power, P_{amp}, can be evaluated through a transistor level noise simulation of the complete filter in the proper clock phase, including feedback, sampling and load capacitors. The modelling of amplifier noise like that of jitter noise and thermal noise leads to model a white noise source and $1/f$ noise source in VHDL-AMS, which is presented in Subsections White Noise Model and $1/f$ Noise Model.

3.4 White Noise Model

As explained above, modelling the thermal noise, jitter noise and op-amp noise leads to generate a white noise in VHDL-AMS. The Box-Muller method [8] is used to generate a random value chosen from a normal distribution. This method consists of two steps : Generating independent random values, $v1$ and $v2$, uniformly distributed over (0, 1); and then a random value, $vnoise$, of normal distribution is derived from $v1$ and $v2$ by (5).

$$vnoise = \sqrt{-2\,ln(v1)}\,cos(2\pi v2). \tag{5}$$

To generate a random value uniformly distributed over (0, 1), the function **uniform** provided by the library **math_real** of ADVanceMS, is used. This function returns a pseudo-random number chosen from a uniform distribution on the interval (0, 1). This model is validated by comparing probability density function of the random value obtained to the theoretical one of a white noise.

3.5 $1/f$ Noise Model

An effective method for generating $1/f$ noise in continuous time makes use of the summation of a few Lorentzian spectral. The summation is expressed as in (6) for N spectra in terms of power spectral density as a function of frequency.

$$S(f) = \kappa \sum_{n=1}^{N} \frac{\varphi_n}{f^2+\varphi_n^2} \approx \frac{\kappa}{f} \qquad \text{for } \varphi_1 < f < \varphi_n. \tag{6}$$

The Lorentzian spectrum can be created by filtering white noise with a single-pole low-pass filter. Equation (7) shows

the magnitude response $H_i(j\omega)$ of a single-pole low-pass filter.

$$H_i(j\omega) = \frac{2\pi\sqrt{\varphi_i}}{j\omega + 2\pi\varphi_i}. \quad (7)$$

The power spectral density when white noise of variance κ is filtered is then

$$S_i(f) = \kappa\,|H_i(f)|^2 = \frac{\varphi_i\,\kappa}{f^2 + \varphi_i^2}. \quad (8)$$

Therefore, to generate $1/f$ noise in VHDL-AMS, independent pseudo-white noises with variance of κ generated by white noise model in Subsection 3.4, are filtered by parallel low-pass filters derived from (8). Pole placements are chosen with equal spacing in the log frequency domain, with a density of more than 1 pole per decade. A single-pole low-pass filter is implemented in VHDL-AMS through time domain equation.

$$\varphi\, v_{out} + \frac{1}{2\pi}\frac{dv_{out}}{dt} = \sqrt{\varphi} v_{in}. \quad (9)$$

3.6 Switch Model

Switch can be simply modelled by a variable resistance depending on switch state which is equal to a small resistance, R_{on}, or a big resistance, R_{off}, representing the on-resistance or off-resistance of the switch respectively. In order to increase the convergence speed, the effective resistance of switch is set to be continuous using in addition two parameters presenting the rising time and falling time of the effective switch resistance respectively.

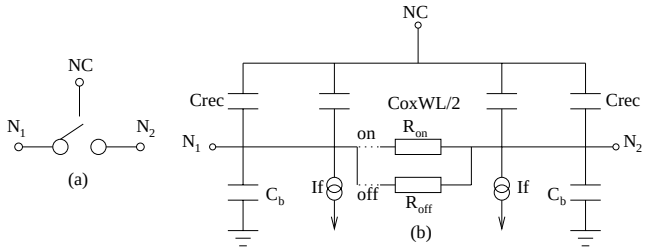

Figure 4: Switch model.

Nonideality parameter such as parasitic capacitances, leakage current may be added to build a very powerful behavioral model as presented in Figure 4. C_b can be considered as the input and output capacitor of the switch, and C_{rec} represents capacitance due to the overlap of gate poly with the source and drain area. Two current sources represent the leakage current from source-body and drain-body junctions. The exact modelling of the charge transfer is a difficult issue because it concerns about load condition of drain and source in the transistor and clock waveforms. However, it is shown that this model is very performing in transient analysis provided that load capacitance area is 50 times greater than the product $W \times L$ of the transistors [9].

3.7 Operational Amplifier Model

The op-amp is a key component in the high-pass filter, the key building block of HP modulator. The performance of the modulator depends mainly on the key op-amp parameters such as slew-rate, finite static gain, bandwidth, and saturation. These parameters are introduced one by one to the VHDL-AMS model of the op-amp to study their effect on the stability and the performance of the HP modulator.

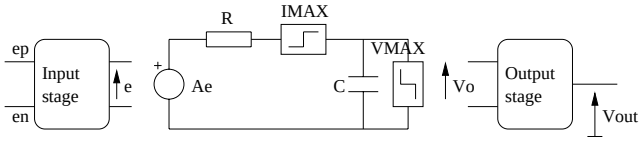

Figure 5: Operational amplifier model.

Figure 5 shows a model of the op-amp. This is a one pole differential or single stage dynamic behavioral model. The model makes it possible to specify finite input and output impedances through the input and output stages, finite gain and finite gain-bandwidth product, slew rate and saturation. The finite gain is defined through parameter A. The finite bandwidth is specified through an R-C network. The slew rate and saturation are accomplished by limiting the output current to $Imax$ and the output voltage by $Vmax$, respectively. The basic equations used to transform the given specifications into internal equations in the model are given by: the -3dB cut-off frequency, f_c is defined as $1/(2\pi RC)$. If R is set to 1Ω then we have $C = 1/(2\pi f_c)$. The output current threshold is then given by $Imax = SR/(2\pi f_c)$.

An even more complete model is presented in [10]. This model is developed by J.B KAMMERER in the Top Behave'sModel'02 contest. In this model, convergence speed is improved and the modelling of various nonideality parameters such as static gain, gain-bandwidth product, saturation and especially slew rate, are validated [10]. This is a quite complete model which is used as our most complex model of op-amp in the simulation of $\Delta\Sigma$ modulator. The modelled parameters of the op-amp is summarized as differential gain; -3dB cut-off frequency; common mode gain; common mode and differential input gain; output impedances; slew rate; and saturation.

3.8 Complete Filter Model

Circuit nonidealities of the high-pass filter are summarized in Figure 6. In the second-order HP $\Delta\Sigma$ modulator, as in the low-pass one, the first filter is the most sensitive component in the modulator. Therefore, all nonidealities are included in the first filter model. Initially, all nonidealities are applied to second filter model. Then, some nonidealities are removed from the second filter model, if the performance of the modulator is not changed.

3.9 Comparator

Single-bit architectures incorporate a simple comparator to perform the internal quantization. A simple DAC is then used in the feedback loop, which does not introduce any nonlinearity error. An ideal behavioral model of comparator is sufficient because the impact of comparator nonlinearities is negligible comparing with those of the amplifier. A more complete version of a comparator that includes hysteresis and an unknown state of the outputs if the input remains in the transition region for more than a specified time can be implemented using a finite state machine. It is a typical example taken for mixed-signal modelling in VHDL-AMS [11].

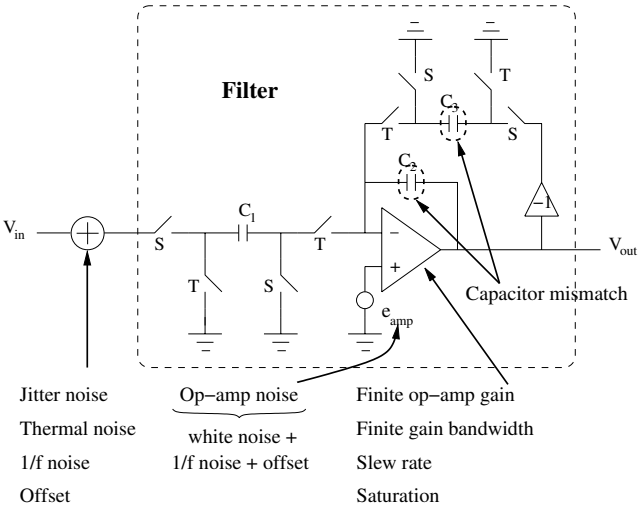

Figure 6: Circuit nonidealities of the high-pass filter building the HP $\Delta\Sigma$ modulator.

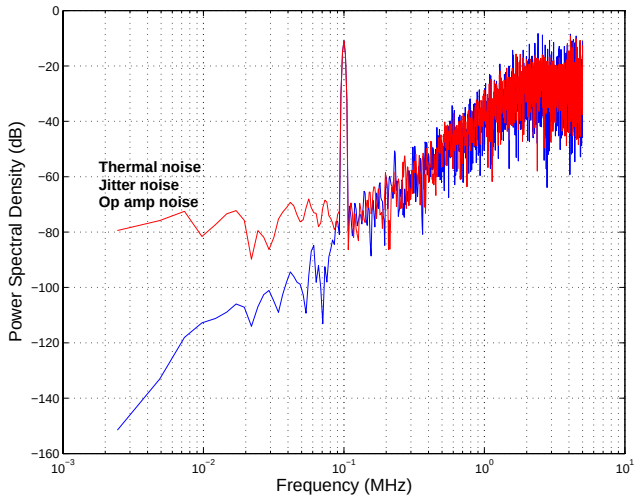

Figure 7: Power spectral density of second-order HP $\Delta\Sigma$ output transformed from HP signal to low frequency signal with ideal modulator and thermal noise, jitter noise and op-amp noise models.

4. SIMULATION RESULTS

Before studying the effect of nonidealities on the stability and performance of the HP modulator, it is necessary to validate the proposed set of models as a whole one even if each individual block has been validated. In order to do this, we perform simulations first on the second-order low-pass modulator and then on the HP modulator. The simulations results in VHDL-AMS are completely as expected and compatible with results from Matlab-Simulink modelling [2]. The summarized simulation results, the effect of different nonidealities, specification on the elementary blocks of the HP second-order $\Delta\Sigma$ modulator are presented hereafter. The simulation parameters used are presented in Table 1.

Parameter	Value
Signal bandwidth	156.25 KHz
Sampling frequency	10 MHz
Oversampling ratio	32
Samples number	45000
Filter gain (C_1/C_2)	0.5
Reference voltages	$\pm$1V

Table 1: Simulation parameters.

4.1 Noise Effect

As expected, thermal noise, jitter noise and amplifier noise increase the inband noise floor, as shown in Figure 7, which degrades the modulator performance. Unlike the effect of amplifier noise in the low-pass modulator, the amplifier noise is amplified at the HP modulator output. The inband noise generated by amplifier noise at the modulator output is about 14 dB higher than the input-referred amplifier noise. This increasing noise at the modulator output is analyzed in [2]. $1/f$ noise has no effect on the modulator performance, because the $1/f$ noise is drowned in the quantization noise which is shaped to low frequency region whereas the useful signal is centered at one-half of the sampling frequency, $f_s/2$. For the same reason, the modulator performance is also insensitive to the offset of the high-pass filter generated from switches and amplifier and comparator offset.

4.2 Nonideality Effect

As in low-pass modulator, the comparator nonideality effect is really negligible in the HP modulator. Simulation results show that the capacitor mismatch and the amplifier nonideality such as static gain, slew rate and bandwidth are critical parameters of the modulator performance. They increase the inband noise floor that degrades the SNR of the modulator. Moreover they lead to harmonic distortion that degrades the SNDR of the modulator and can make the modulator unstable [2]. Other parameters that should be considered are on-resistance, parasitic capacitance, and current leakage of the switch. In order to implement a high-pass HP $\Delta\Sigma$ modulator, we determine elementary block specifications that are summarized in Table 2. With these specifications, the SNDR is 53dB with a 32 oversampling ratio and the sampling rate is 10 MHz.

Nonideality	Parameter	Threshold
Sampling jitter	ΔT	$<$ 0.1ns
Switch (kT/C) noise	C	$>$ 10fF
Amplifier noise	E_{amp}	$<$ 0.2mV_{rms}
Switch on-resistance	Ron	$<$ 1KΩ
Parasitic switch cap	Crec + WLCox	$<$ 30fF
Leakage current	Ifd	$<$ 0.1 μA
Finite gain	$Gain$	$>$ 60 dB
Transition frequency	f_t	$>$ 160 MHz
Slew rate	SR	$>$ 50V/μs
Saturation	Vmax	$>$ 1.4V
Capacitor mismatch		$<$ 0.5%

Table 2: Specification summary.

4.3 Simulation vs. Measurement Results

From the block specifications shown in Table 2, we designed a second-order HP $\Delta\Sigma$ modulator in CMOS process to validate the set of models developed and the concept of high-pass modulator. Figure 8 shows the power spectral density of HP $\Delta\Sigma$ modulator output from behavioral simulation and measurement. Figure 8(b) presents a zoom of the Figure 8(a) in the signal band of interest. The blue and red curves represent the results from behavioral simulation in VHDL-AMS and measurement, respectively. They show a good agreement. The SNR and SNDR obtained from measurement are very close from the results obtained by behavioral simulation in VHDL-AMS. The input signal into the chopper is a 10 kHz sinusoidal whose signal level is -3dB. The sampling rate is 10 MHz, the signal coming into the HP modulator is then at 4.9 MHz. The plot scale is power density (dB) versus frequency (kHz). The SNR is 53 dB with a 32 oversampling ratio, the SNDR is 51 dB. The fall of the SNDR compared to the SNR is because the third harmonic distortion is about 52 dB, much lower than expected (65 dB). This degradation may come from low performance of the op-amp designed. In this sense, a higher op-amp slew-rate is certainly needed in order to weaken the harmonic distortions. Measurement shows that this modulator is completely insensitive to low frequency noise.

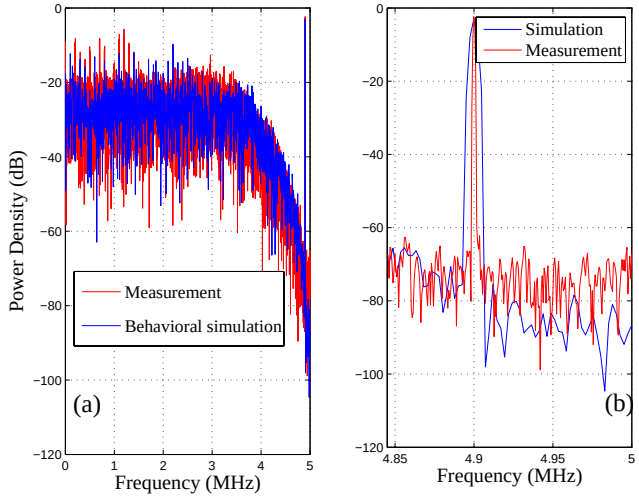

Figure 8: Measured vs. simulated power spectral density of the HP modulator output

The measurement results confirm both the behavioral description and simulation, and the theoretical study of the HP $\Delta\Sigma$ modulator. They demonstrate thus the validation of the set of behavioral models in VHDL-AMS and the top-down design methodology presented in this paper.

5. CONCLUSIONS

In this paper, we present a top-down methodology design with VHDL-AMS. A set of models in VHDL-AMS suitable for time-domain behavioral simulation of SC $\Delta\Sigma$ modulators is developed. The proposed set of models takes into account at the behavioral level most of SC $\Delta\Sigma$ modulator nonidealities, such as jitter noise, kT/C noise, $1/f$ noise, amplifier noise, switch nonidealities, amplifier nonidealities, and capacitor mismatch. This allows us to study the effect of various nonideality parameters on the HP $\Delta\Sigma$ modulator performance, and to define the threshold set of nonideality parameters value ensuring a desired performance of the modulator. This methodology allows us not only to make a specification of each elementary device of the $\Delta\Sigma$ modulator and estimate its performance, but also to optimize various nonideality parameters to obtain a good performance of the modulator. This is really useful for HP $\Delta\Sigma$ modulator design, because unlike the low-pass modulator, a major problem of the HP modulator with the implementation of the high-pass filter we proposed, are the stability and amplified noise of the op-amp noise at the output of the modulator.

6. ACKNOWLEDGMENTS

The authors would like to thank the European Community for the sponsorship of this work through SPRING project.

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